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Novel Offline Switched Mode Power Supplies for Solid State Lighting Applications

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"*Con un sorriso sarà tutto più semplice...*"

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It may sound obvious to keep in mind to always thank the persons to whom we owe all we have, but unfortunately it is not so. Especially when the daily grind leads us to focus on our personal needs, problems and goals.
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Abstract

In recent years, high brightness light emitting diodes (HBLEDs) have increasingly attracted the interest of both industrial manufacturers and academic research community. Among the several aspects that make LED technology so attractive, the most appreciated characteristics are related to their robustness, high efficiency, small size, easy dimming capability, long lifetime, very short switch-on/switch-off times and mercury free manufacturing.

Even if all such qualities would seem to give to solid state lighting a clear advantage over all the other kinds of competing technologies, the issues deriving from the need of LED technology improvement, on one hand, and of the development of suitable electronic ballasts to properly drive such solid state light sources, on the other, have so far hindered the expected practical applications.

The latter problem, in particular, is nowadays considered the main bottleneck in view of a widespread diffusion of solid state technology in the general lighting market, as a suitable replacement of the still dominant solutions, namely halogen and fluorescent lamps.

In fact, if it is true that some aspects of the devices' technology (e.g. temperature dependent performance, light quality, efficiency droop, high price per lumen, etc…) still need further improvements, it is now generally recognized that one of the key requirements, for a large scale spread of solid state lighting, is the optimization of the driver.

In particular, the most important specifications for a LED lamp ballast are: high reliability and efficiency, high power factor, output current regulation, dimming capability, low cost and volume minimization (especially in domestic general lighting applications). From this standpoint, the main goal is, therefore, to find out simple switched mode power converter topologies, characterized by reduced component count and low current/voltage stresses, that avoid the use of short lifetime devices like electrolytic capacitors. Moreover, if compactness is a major issue, also soft switching capability becomes mandatory, in order

to enable volume minimization of the reactive components by increasing the switching frequency in the range of the hundreds of kHz without significantly affecting converter's efficiency.

It is worth mentioning that, in order to optimize HBLED operation, also other matters, like the lamp thermal management concern, should be properly addressed in order to minimize the stress suffered by the light emitting devices and, consequently, the deterioration of the light quality and of the expected lamp lifetime. However, being this work focused on the issues related to the research of innovative driving solutions, the aforementioned thermal management problems, as also all the topics related to the improvement of solid state devices' technology, will be left aside.

The main goal of the work presented in this thesis is, indeed, to find out, analyze and optimize new suitable topologies, capable of matching the previously described specifications and also of successfully facing the many challenges dictated by the future of general lighting.

First of all, a general overview of solid state lighting features, of the state of the art of lighting market and of the main LED driving issues will be provided.

After this first introduction, the offline driving concern will be extensively discussed and different ways of approaching the problem, depending on the specific application considered, will be described.

The first kind of approach investigated is based on the use of a simple structure relying on a single power conversion stage, capable of concurrently ensuring: compliance with the standards limiting the input current harmonics, regulation of the load current and also galvanic isolation. The constraints deriving from the need to fulfil the EN 61000-3-2 harmonics standard requirements, when using such kind of solution for low power (<15W) LED driving purposes, will be extensively discussed.

A low cost, low component count, high switching frequency converter, based on the asymmetrical half bridge flyback topology, has been studied, developed and optimized. The simplicity and high compactness, characterizing this solution, make it a very good option for CFL and bulb replacement applications, in which volume minimization is mandatory in order to reach the goal of placing the whole driving circuitry in the standard E27 sockets. The analysis performed will be presented, together with the design procedure, the simulation outcomes and the different control and optimization techniques that were studied, implemented and tested on the converter's laboratory prototype.

Another interesting approach, that will be considered, is based on the use of integrated topologies in which two different power conversion stages are merged by sharing the same power switch and control circuitry.
In the resulting converter, power factor correction and LED current regulation are thus performed by two combined semi-stages in which both the input power and the output current have to be managed by the same shared switch. Compared with a conventional two-stages configuration, lower circuit complexity and cost, reduced component count and higher compactness can be achieved through integration, at cost of increased stress levels on the power switch and of losing a degree of freedom in converter design. Galvanic isolation can be provided or not depending on the topologies selected for integration. If non-isolated topologies are considered for both semi-stages, the user safety has to be guaranteed by assuring mechanical isolation throughout the LED lamp case.
The issue, deriving from the need of smoothing the pulsating power absorbed from the line while avoiding the use of short lifetime electrolytic capacitors, will be addressed. A set of integrated topologies, used as HBLED lamp power supplies, will be investigated and a generalized analysis will be presented. Their input line voltage ripple attenuation capability will be examined and a general design procedure will be described.
Moreover, a novel integrated solution, based on the use of a double buck converter, for an about 15W rated down-lighting application will be presented. The analysis performed, together with converter design and power factor correction concerns will be carefully discussed and the main outcomes of the tests performed at simulation level will be provided.

The last kind of approach to be discussed is based on a multi-stage structure that results to be a suitable option for medium power applications, like street lighting, in which compactness is not a major concern.
By adopting such kind of solution it is, indeed, possible to optimize converter's behavior both on line and on load side, thereby guaranteeing both an effective power factor correction at the input and proper current regulation and dimming capability at the output.
Galvanic isolation can be provided either by the input or the output stage, resulting in a standard two stage configuration, or by an additional intermediate isolated DC-DC stage (operating in open loop with a constant input/output voltage conversion ratio) that namely turns the AC/DC converter topology into a three stage configuration. The efficiency issue, deriving from the need of multiple energy processing along the path between the utility grid and the LED load, can be effectively addressed thanks to the high flexibility

guaranteed by this structure that, relaxing the design constraint, allows to easily optimize each stage.

A 150W nominal power rated ballast for street solid state lighting applications, based on the latter (three stage) topology, has been investigated. The analysis performed, the design procedure and the simulations outcomes will be carefully described, as well as the experimental results of the tests made on the implemented laboratory prototype.

Abstract

Negli ultimi anni i dispositivi LED di potenza ad elevata luminosità (HBLED) hanno attirato in misura sempre crescente l'interesse della comunità scientifica, sia all'interno del mondo accademico che di quello industriale. Tra le varie caratteristiche, che rendono questo tipo di tecnologia interessante, le qualità più apprezzate sono certamente: la robustezza, l'elevata efficienza, le piccole dimensioni, la facilità di modulazione dell'intensità luminosa, il lungo tempo di vita, l'estrema rapidità di accensione e spegnimento e l'assenza di mercurio.

Nonostante tutti questi aspetti sembrino dare alla tecnologia a stato solido un netto vantaggio rispetto alle tecnologie concorrenti, l'utilizzo dei LED di potenza nel campo dell'illuminazione rimane a tutt'oggi abbastanza limitato. La necessità di ulteriori progressi nella tecnologia dei dispositivi, da un lato, e dello sviluppo di soluzioni in grado di garantirne il corretto ed efficiente pilotaggio, dall'altro, ne hanno, infatti, fino ad ora frenato la diffusione rispetto alle attese.

Quest'ultimo aspetto, in particolare, è al giorno d'oggi considerata il vero "collo di bottiglia" in vista dell'impiego su larga scala della tecnologia a stato solido, in sostituzione delle soluzioni, tutt'ora dominanti nel mercato dell'illuminazione, basate sull'utilizzo di lampade alogene e a fluorescenza.

Se, da un lato, infatti, è vero che alcuni aspetti della tecnologia dei dispositivi (e.g. variabilità delle prestazioni con la temperatura, qualità della luce, calo dell'efficienza luminosa con l'aumentare della corrente, elevato costo per lumen, ecc...) necessitano di essere ulteriormente perfezionati, dall'altro è ormai universalmente riconosciuto che l'elemento chiave per l'ampia diffusione dell'illuminazione a stato solido è proprio l'ottimizzazione dello stadio di alimentazione.

In particolare, le specifiche più importati che un ballast per lampade a LED è tenuto a soddisfare sono: elevata affidabilità ed efficienza, elevato fattore di potenza, capacità di regolazione della corrente di uscita e di modulazione del flusso luminoso, basso costo e

minimo ingombro (soprattutto nell'illuminazione domestica). L'obiettivo principale è, quindi, riuscire ad ideare soluzioni basate sull'utilizzo di topologie semplici, caratterizzate da ridotto numero di componenti e limitati livelli di stress di corrente e tensione, che non prevedano l'impiego di componenti con breve tempo di vita come i condensatori elettrolitici. Inoltre, nelle applicazioni in cui la compattezza è considerata uno degli aspetti di maggior rilievo, anche la capacità di operare in soft-switching diviene una specifica indispensabile. Ciò è infatti necessario al fine di permettere la minimizzazione del volume delle componenti reattive, tramite l'aumento della frequenza di commutazione nel range delle centinaia di kHz, senza compromettere l'efficienza del convertitore.
Per completezza, vale la pena di ricordare che, per ottimizzare il funzionamento dei LED ad elevata luminosità, andrebbero presi in considerazione anche altri aspetti, come ad esempio le problematiche legate alla gestione del calore dissipato dalla lampada, importanti al fine di limitare gli stress termici subiti dai dispositivi e, di conseguenza, migliorare la qualità della luce emessa e massimizzare il tempo di vita della lampada.
Tuttavia, essendo il lavoro presentato in questa tesi centrato sulle questioni relative allo stadio di alimentazione, i suddetti problemi di gestione termica, come anche gli aspetti relativi allo sviluppo della tecnologia dei dispositivi non verranno esaminati.
L'obiettivo principale del lavoro che verrà descritto nel corso dei prossimi capitoli, è, infatti, la ricerca di soluzioni innovative per il pilotaggio da rete elettrica di lampade basate su tecnologia a stato solido. Verranno pertanto approfonditamente trattate le tematiche relative ad analisi, ottimizzazione e sviluppo di topologie che siano in grado di soddisfare i requisiti precedentemente enunciati e di affrontare con successo le sfide proposte dalla continua evoluzione dello scenario del "general lighting".
Per prima cosa, sarà fornita una visione di insieme riguardante lo stato dell'arte del mercato dell'illuminazione, le caratteristiche dei dispositivi di illuminazione a stato solido ed i principali aspetti relativi al loro pilotaggio.
Dopo questa prima sezione introduttiva, la tematica relativa all'alimentazione da rete elettrica di tali dispositivi verrà approfonditamente discussa. Differenti modi di approcciare il problema, a seconda della specifica applicazione considerata, verranno discussi.

Il primo tipo di approccio che verrà esaminato si basa sull'uso di una semplice struttura, formata da un singolo stadio di conversione di potenza. Essa è in grado di fornire al contempo il rispetto degli standard che limitano il contenuto armonico della corrente di ingresso, l'isolamento galvanico e la regolazione della corrente e dell'intensità luminosa in uscita.

ABSTRACT

I vincoli, dettati dall'esigenza di garantire il rispetto della normativa EN 61000-3-2, in applicazioni di bassa potenza (<15W) prive di uno stadio dedicato alla correzione del fattore di potenza, verranno approfonditamente trattati.
Saranno, poi, illustrati i risultati dello studio, sviluppo ed ottimizzazione di un convertitore a singolo stadio, operante ad elevata frequenza di commutazione, basato sulla topologia flyback a mezzo ponte asimmetrico. La semplicità, il ridotto numero di componenti ed il basso costo, che caratterizzano tale tipo di soluzione, la rendono adatta all'alimentazione di lampade per il settore residenziale, in cui la compattezza dello stadio di alimentazione è di fondamentale importanza al fine di consentirne l'alloggiamento nei classici socket E27. L'analisi effettuata, la procedura di progetto ed risultati ottenuti in simulazione ed a livello sperimentale durante lo studio di tale topologia verranno accuratamente descritti e discussi.

Un altro interessante tipo di approccio che verrà considerato si basa sull'utilizzo di topologie integrate, nelle quali due diversi stadi di conversione vengono uniti tramite la condivisione dello stesso interruttore di potenza e della relativa circuiteria di comando.
Nel convertitore che ne risulta, la correzione del fattore di potenza e la regolazione della corrente nei LED saranno dunque garantite dalla combinazione dei due semi-stadi, il cui interruttore comune dovrà essere in grado di gestire sia la potenza di ingresso che la corrente di uscita.
Rispetto alla configurazione a due stadi convenzionale, la soluzione ottenuta tramite l'integrazione consente una minore complessità circuitale, un ridotto numero di componenti e, di conseguenza, una maggiore compattezza ed un minor costo. Tutto ciò viene guadagnato a scapito di un maggiore livello di stress nei componenti e della perdita di un grado di libertà nel progetto del convertitore. L'isolamento galvanico può essere garantito o meno a seconda del tipo di topologie che vengono selezionate per l'integrazione. Se la scelta ricade su topologie non isolate, la sicurezza dell'utente andrà comunque garantita isolando meccanicamente l'involucro della lampada.
I problemi legati alla necessità di smorzare la componente alternata della potenza assorbita dalla rete, evitando al contempo l'utilizzo di componenti con basso tempo di vita, come i condensatori elettrolitici, verranno discussi. A tal proposito si studieranno le caratteristiche di un insieme di topologie integrate, al fine di fornirne un'analisi ed una procedura di design generalizzate. Se ne esaminerà, inoltre, la capacità di attenuare la componente ondulatoria della tensione di ingresso che viene trasferita al carico, dove si traduce in un'oscillazione della corrente di alimentazione fornita ai LED.

Verrà proposta, poi, una soluzione basata su una topologia derivante dall'integrazione di due convertitori di tipo step-down (abbassatori di tensione), per applicazioni di "down-lighting", dimensionata per una potenza di circa 15W. Se ne discuteranno, in particolare, i dettagli di maggiore interesse relativi all'analisi effettuata, alla procedura di progetto ed ai risultati dei test effettuati in ambiente di simulazione.

L'ultimo tipo di approccio considerato prevede, infine, l'utilizzo di una topologia multi-stadio, ritenuta una scelta appropriata soprattutto per applicazioni lighting di potenza elevata (>60W), come l'illuminazione stradale, in cui la compattezza dell'alimentatore non è ritenuta un aspetto di primaria importanza.
Tramite questo tipo di soluzione è, infatti, possibile ottimizzare le prestazioni del convertitore sia dal lato della rete che dal lato del carico. Si riescono a garantire, in tal modo, un'efficace correzione del fattore di potenza, un adeguato controllo della corrente di uscita ed un'appropriata modulazione del flusso luminoso emesso dalla lampada.
L'isolamento galvanico può essere fornito dallo stadio di ingresso o da quello di uscita o da un aggiuntivo stadio DC-DC intermedio, operante a catena aperta con rapporto di conversione di tensione costante. In quest'ultimo caso la struttura del convertitore, si trasforma, dalla classica configurazione a due stadi, in una topologia a triplo stadio.
Il problema che nasce dalla necessità di assicurare un elevato livello di efficienza del sistema, nonostante l'interposizione di ripetuti stadi di conversione dell'energia tra la rete ed il carico a LED, può essere efficacemente risolto grazie alla flessibilità che caratterizza tale tipo di struttura. L'aumento del numero dei gradi di libertà in fase progettuale permette, infatti, di ottimizzare con semplicità ogni singolo stadio.
Per comprovare limiti e potenzialità di tale tipo di approccio, si è deciso di studiare un ballast (dimensionato per una potenza nominale di 150W) basato sulla topologia a triplo stadio precedentemente menzionata, per applicazioni nell'ambito dell'illuminazione stradale. L'analisi condotta, la procedura di progetto ed i risultati delle simulazioni effettuate verranno discussi nel dettaglio, così come i risultati sperimentali dei test di laboratorio effettuati sul prototipo costruito.

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Chapter 1

Solid State Lighting

1.1. Introduction

In the last decades, many issues related to global warming and to the increasing economic and environmental cost of the energy have started gaining a center stage in the public debate.

Every year, indeed, a huge amount of energy is used to support human activities worldwide, as can be noticed by observing the reference picture shown in Fig. 1.1.1. The obvious consequences are the continuous impoverishment of natural resources and the massive emission of CO_2 and other gasses, that actually increase pollution level and favor the greenhouse effect.

Moreover, in order to fully understand the significance of such problem, another fundamental aspect should be taken into account, that is the impressive growth rate of the so-called developing countries.

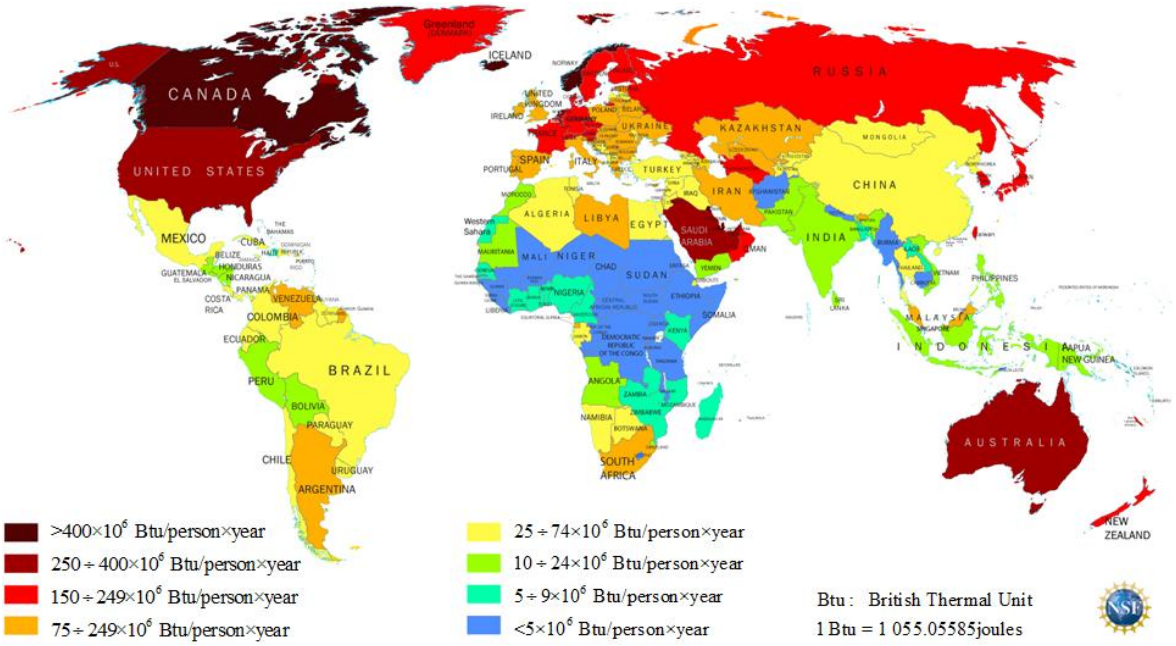


Fig. 1.1.1 – Average annual energy consumption per capita by country (year 2009). Source: United States Central Intelligence Agency.

As a suitable reference of this concern, can be considered the data reported Fig. 1.1.2 (a) and (b), describing the contributions of the different world regions to the global energy consumption, referred to the years 1973 and 2010 ([1], [2]).

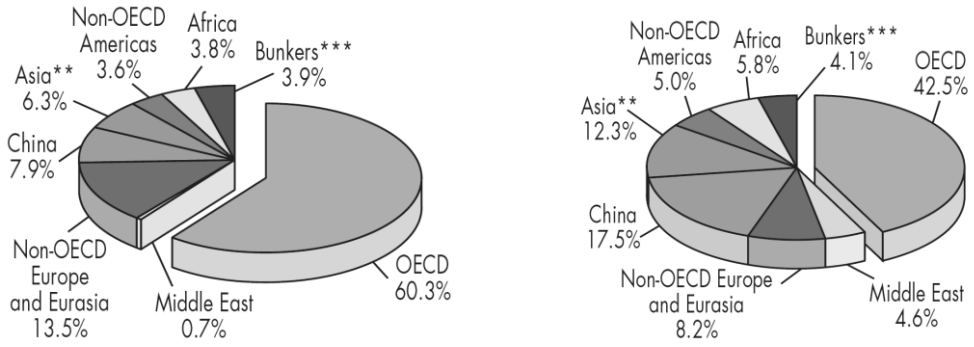
As it can be observed, in the last forty years, the non-OECD member countries (see the notes in Fig. 1.1.2 for details) essentially reversed the course, rising from about 40% to about 60% of the overall energy consumptions.

This clearly forces a substantial rethinking of the way in which energy is generated and used in order to meet the world growing demand for energy.

In an effort to address such problem, concerns like green power, sustainability, and energy saving have become therefore a matter of priority for the international scientific community, with the aim of optimizing the use of available resources and protect the environment.

From this perspective, the main target is to relieve the dependence on fossil fuels, through a larger use of renewable resources, while improving, at the same time, the efficiency of the daily used electrical equipments, thus reducing global consumptions.

In particular, as concerns the latter issue, it may be worth to consider, as a reference, the distribution of the electrical power demand by application, concerning the U.S. commercial buildings, whose relating data, reported in [3] has been summarized in Fig. 1.1.3.



(a) *(b)*

Fig. 1.1.2 – World total energy consumption, by region ,in the years (a)1973 and (b) 2010.

Source: International Energy Agency: "Key World Energy statistics ", released in 2012
Notes:
- the region "Asia" excludes the data relative to the People's Republic of China and Hong Kong;
- the term "Bunkers" includes international aviation and international marine bunkers;
- the countries members of the Organization for Economic Co-Operation and Development (OECD) are: Australia, Austria, Belgium, Canada, Chile, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Israel, Italy, Japan, Korea, Luxembourg, Mexico, the Netherlands, New Zealand, Norway, Poland, Portugal, the Slovak Republic, Slovenia, Spain, Sweden, Switzerland, Turkey, the United Kingdom, the United States (Estonia and Slovenia from 1990).

As it can be observed, about 20% of the electrical energy consumed, is transformed into artificial light. It can be therefore consequently inferred how a strong innovation effort in this field, aimed at improving light sources efficiency, would actually produce substantial benefits in terms of energy saving and reduction of CO_2 emissions.

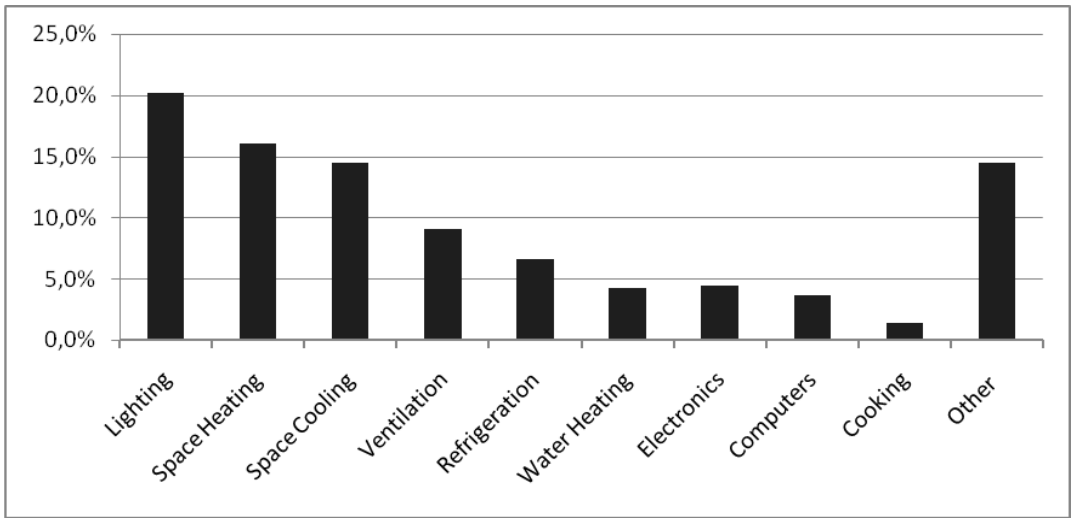


Fig. 1.1.3 – Distribution of electrical energy demand by application in U.S. commercial buildings. Source: U. S. Department of Energy: "Building energy data book" 2011.

As a matter of facts, given the relevance of lighting in the worldwide energetic scenario, it is clearly strategic to move towards the use of more efficient light sources. For this reason the European Union, together with many other countries, in 2009 decided to start the phase-out of incandescent light bulbs [4].

Such light sources, invented in the late nineteenth century, are indeed capable of converting only less than 5% of the supplied energy into visible light, while dissipating the whole remaining amount of energy into heat.

From this perspective, nowadays, the most promising technology is represented by solid state lighting (SSL) in which energy is directly converted into light by manipulating the electrons in a solid, at room temperature. Unlike the case of conventional lighting, namely based on incandescent and fluorescent light sources, in which light is instead generated through an indirect process (electricity is used at first to produce heat and gas discharges) that actually limits conversion efficiency.

The beneficial effects deriving from the replacement of conventional lighting with solid state lighting sources, in terms of energy saving, will be presented in paragraph 1.4.3.

However, besides the higher conversion efficiency, with respect to the other light sources, there are many other advantages actually characterizing the solid state lighting technology.

In particular, among the others it is worth to mention the long lifetime (about 50000 hours), the robustness to shocks and vibrations, the very fast turn-on and turn-off speed, the dimming capability, the very low radiation in the infra-red spectrum, the highly directional light emission, the compactness, etc...

However, despite their many widely recognized positive characteristics, the widespread of LED lamps currently still find it hard to occur.

As an example, it can be considered that, according to the lighting market characterization, released in 2012 by the U.S. Department of Energy, [5]., over the last decade the total number of LED lamps, installed in the U.S.A., has grown from 1.6 million (in 2001) to 67 million lamps (in 2010).

Although this corresponds to an increase equal to 4000%, the actual datum is that, in 2010, LED lamps still represented approximately only 1% of the whole installed lamps.

In order to support a large scale spread of solid state lighting, it is fundamentally important to improve the overall reliability and efficiency of such light sources. Actually the main way to reduce their cost per lumen and compensate for their high initial price, as it that will be better explained in the following paragraphs.

1.2. Lighting

1.2.1. The Long Debate on the Nature of Light

A long lasting debate has permeated the study of light nature along the past centuries, mainly due to the conflict between two main different competing models.

Two contrasting early theories, indeed, were developed since the late seventeenth century, aimed to physical modeling light nature on one hand as a collection of fast-moving particles and on the other hand as a propagating wave.

The first detailed wave theory of light was formally formulated in 1690 in the "Traité de la Lumiere" (i.e. Treatise on Light) by the Duch astronomer Christiaan Huygens. He was the first to describe light as a composition of waves perpendicularly vibrating with respect to light direction, being also able to derive the laws of reflection and refraction.

Almost in the same years, however, another brilliant scientist was carrying out his research activity on light properties, sir Isaac Newton. Differently from Huygens, to explain the phenomena he observed during his studies, Newton theorized that light is composed by a stream of particles ("Optiks", 1704). In order to meet the law of refraction, he made the hypothesis that transparent objects exert an attractive force on such corpuscles, consequently increasing light speed with respect to light transfer in vacuum.

Newton also asserted that particles of different colors have slight mass differences resulting in different speeds in transparent media and therefore in different refraction angles.

Because of the great authority Isaac Newton had in the scientific community, his corpuscular model resisted until the early nineteenth century when the evidences of the wave nature of light became overwhelming.

In particular, Thomas Young experiments on light interference phenomena (1803), then mathematically formalized by Augustin Fresnel in 1815, that significantly bolstered Huygens theory.

However, notwithstanding the many theoretical and experimental proofs, the actual behavior of the light wave remained almost unknown until 1860, when J.C. Maxwell was actually able to described the electromagnetic radiation as a wave of coupled electric and magnetic fields propagating through the space.

He also proposed a careful mathematical formulation of his physical inferences. In its modern form it is expressed through four fundamental equations, that relate the electric and

magnetic fields to their source and still represent the basis of the classical electromagnetism.

Given the highly convincing theoretical and experimental evidences supporting the wave nature of light, at the end of the nineteenth century the conflict between the wave and corpuscular nature of light seemed to have been definitively resolved.

Together with the mechanics and thermodynamics theory of Newton, Maxwell formulation of electromagnetism was adopted as a foundational element of physics.

However in the very early twentieth century, new studies about the blackbody radiation, along with new experimental methods improving the investigation at atomic level, opened the way to quantum physic and led to a substantial departure from classical theories.

In 1900 Planck proposed the idea that the electromagnetic radiation can be emitted and absorbed only in finite packets, called "quanta" whose energy is proportional to the radiation frequency:

$$E = h \cdot f \tag{1.2.1}$$

according to a constant of proportionality ($h = 6.626 \cdot 10^{-34}\ js$) that was experimentally derived and it is worldwide known with the name of Planck's constant.

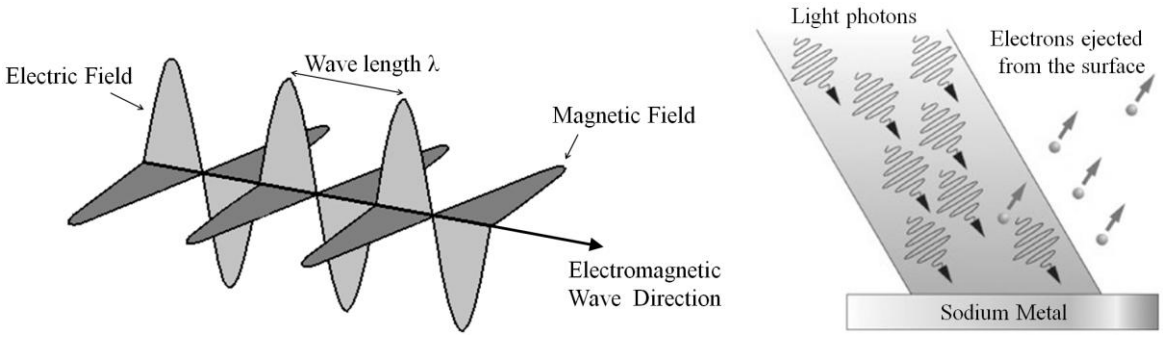
This theory substantially revolutionized physics, however Planck did not provide a physical basis to its proposal, offering essentially only a mathematical construct, aimed at meeting the experimental observations he made on the black body spectrum.

A physical interpretation of such theory was first provided in 1905 by Albert Einstein, that, on the basis of thermodynamic arguments applied to a radiation field obeying to Planck's radiation law, inferred the granular nature of the radiation.

He proposed, in particular, a solution based on the idea that light has both wave and particles characteristic, suggesting that light is composed of energy "quanta", later called "photon", according to the term coined by G. N. Lewis. Each photon has an energy depending on the solely radiation frequency, being independent from light intensity.

Einstein supported his idea through a detailed analysis of the photoelectric effect, an already known process in which electrons are ejected from a metallic surface illuminated by light.

By means of careful experimental measurements, he finally showed that the onset of such process is related to the only frequency of the light and the makeup of the surface, concluding that a only photons with a sufficient amount of energy can induce electron emission.



(a) *(b)*

Fig. 1.2.1 – (a) Maxwell description of the electromagnetic radiation, (b) photoelectric effect.

The basic principles of Einstein theory, claiming the dual nature of electromagnetic radiation, are still universally accepted by modern physic. Light diffracts, reflects off of material surfaces, refracts entering into a material with a different density and can be absorbed by the material. It is, therefore, supposed to both propagate from a place to another as an electromagnetic wave and to interact with matter via absorption and emission as a particle.

1.2.2. The Electromagnetic Spectrum and Visible Light Perception

As previously mentioned, Maxwell research effort, culminated in the formulation of the electromagnetism theory, gave a fundamental contribution to the description of the wave nature of light.

Moreover it is worth to remember that on the basis of Maxwell theory, in 1888 Hertz demonstrated the existence of other electromagnetic waves in addition to those composing visible light. Although characterized by longer wavelengths, such waves resulted, indeed, to be consistent with the properties of light waves, actually demonstrating that light is only a part of a much broader set of phenomena.

Even if there is no theoretical difference between electromagnetic waves with different wavelengths, the electromagnetic spectrum can be divided into different wavelength intervals. Such portions usually take their names from the way the wave are produced or detected, the applications in which they are used, the scientific development that led to their identification, etc.., as shown in Fig. 1.2.2.

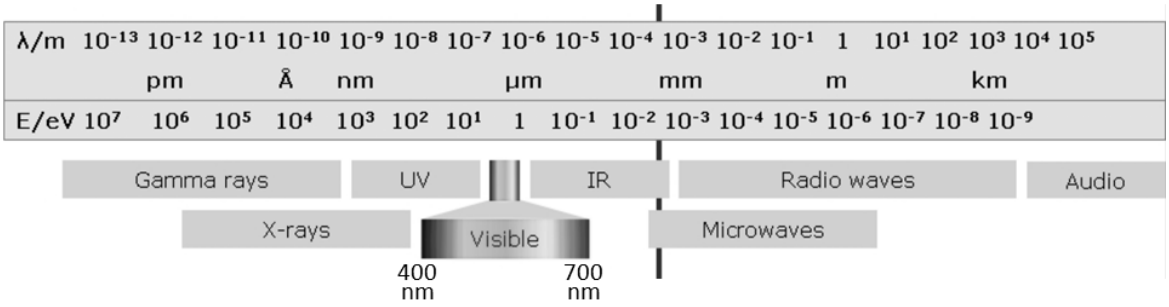


Fig. 1.2.2 – The electromagnetic spectrum.

As it can be noticed, the interval of electromagnetic radiation that is detectable by human eyes, usually referred as visible light or white light, or simply light, is effectively only a small part of the spectrum, including the wavelengths approximately ranging between the 400 and the 700nm.

The human eye is provided of two kinds of receptors named rods and cones, either involved in the visual process depending on the light level. The former contribute to scotopic vision in low light condition, being essentially insensitive to colors. The latter, on the other hand, guarantee color sensitivity contributing to the so-called photopic vision in high luminance conditions. There are three different kinds of cones whose peak sensitivity lie in the violet (blue cones), green (green cones) and yellow (red cones) range, respectively.

Color perception is therefore given by the combination of physical, physiologic and psychic activities, involving the characteristics of electromagnetic radiation and of the human eye and brain, actually resulting in a complex subjective process.

Since the human eye is unable to make spectrum analysis of the radiation, electromagnetic radiations characterized by different spectral contents can be perceived in the same way.

As a consequence, a given perceived color can be the effect of light sources emitting a mixtures of different wavelengths, known as the phenomenon of metamerism. From this perspective a fundamental role is played by colorimetry, a science aimed at quantifying and physically describing the colorimetric stimulus that determines human color perception.

In order to provide suitable tools to enable a standard color evaluation and reproduction, proper standard scales and reference quantities have been established by the "Commission International de l'Eclairage" (CIE) and the "Optical Society of America" (OSA).

The basic idea is to conceptualize the parameters describing color sensation, the so-called "tristimulus values", related to the stimulation of the human eye cone photoreceptors, as the amount of three primary colors in a tri-chromatic additive color model ([6]).

To eliminate the dependence on the observer, due to its particular eye receptors distribution, a standard colorimetric observer has also been defined.

In the CIE color space, such tristimulus values (usually indicated with the capital letters X, Y and Z) are associated with colors by means of color-matching function, that numerically describe the chromatic response of such standard observer.

As a result, a complete plot of the whole visible color set, should be three dimensional.

However, in order to derive a practical reference to specify the different colors, two different concepts, namely brightness and chromaticity, can be distinguished.

The latter, in particular, can be specified by two of the normalized parameters, also called chromaticity coordinates:

$$x = \frac{X}{X+Y+Z} \qquad y = \frac{Y}{X+Y+Z} \qquad z = \frac{Z}{X+Y+Z} \tag{1.2.2}$$

being the third one linearly dependent from the others according to the relation:

$$x + y + z = 1 \tag{1.2.3}$$

The corresponding CIExy bi dimensional diagram, commonly used to specify the chromaticity of a color is shown in Fig. 1.2.3.

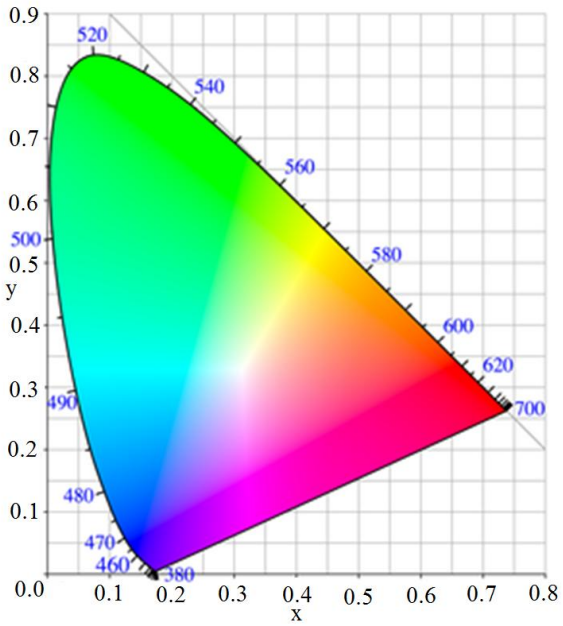


Fig. 1.2.3 – Chromaticity diagram.

Moreover, since the CIE XYZ color space was deliberately designed so that the Y parameter was a measure of the brightness, the resulting color space CIE xyY, (specified by the chromaticity parameters x, y and the brightness parameter Y) can be practically used as a reference to exhaustively specify each different color.

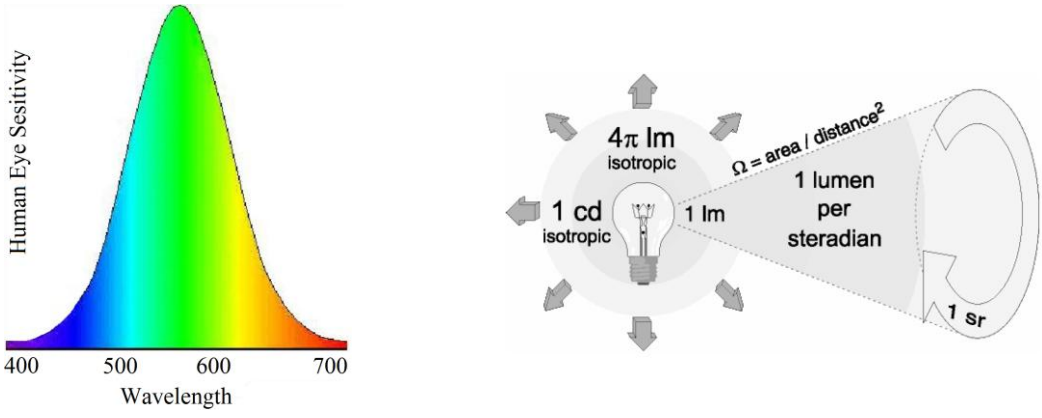
Once briefly summarized the underlying ideas of electromagnetic spectrum and color, it is worth to spend a few words on some basic light measurement parameters, that are widely used to describe light sources [7]. Namely: luminous flux, luminous intensity, illuminance, luminous efficiency and luminous efficacy.

Luminous Flux

The luminous flux accounts for the portion of power emitted by a light source that is actually perceived by the human eye and is measured in "lumens" (lm). It is therefore significantly different from the concept of radiant flux, that corresponds, instead, to the measure of the total power of the emitted light, despite human eye sensitivity to the different radiation wavelengths.

The luminous flux can be computed as the integral, over the visible spectrum wavelengths (λ), of the product between the radiant power P(λ) and the CIE spectral luminosity function V(λ) (Fig. 1.2.4 (a)) scaled by the lumens per watt conversion factor for CIE curve (k=683 lumen/W):

$$\phi = k \cdot \int_{380\text{nm}}^{730\text{nm}} P(\lambda) \cdot V(\lambda)\, d\lambda \quad [\text{lumen}] \tag{1.2.4}$$



(a) *(b)*

Fig. 1.2.4 – (a) Relative eye sensitivity (b) isotropic light source: luminous flux and luminous intensity.

Luminous Intensity

Since many sources are not isotropic, the luminous intensity accounts for the amount of luminous flux emitted in a specific direction into a solid angle, called steradian. The SI unit of luminous intensity is the "candela" (cd), which is defined as lumens over steradians (sr). As it can be observed from Fig. 1.2.4 (b), an isotropic light source will emit uniformly in a total volume of 4π sr. As a result, in such case a luminous intensity of one candela will correspond to a luminous flux of 4π lumens.

Illuminance

Such parameter is measured in "Lux" and expresses the photometrically corrected power (lumens) falling upon a given unity of surface area (m^2)

Each luminaire can be considered a point source if the observation distance is at least five time greater than light source diameter. Now, from a point source, light will spread out, so that the illuminated surface will increase (and consequently the illuminance value will decrease) according to the inverse square law (Fig. 1.2.5 (a))

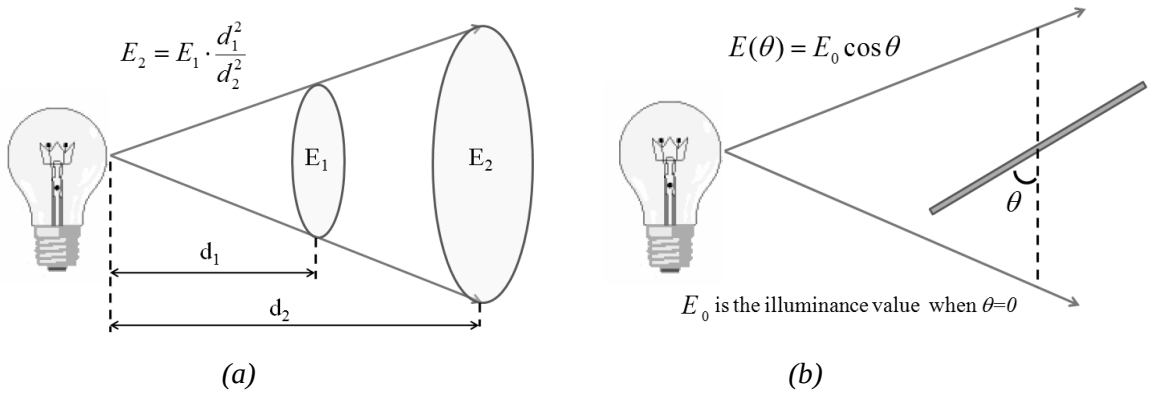


Fig. 1.2.5 – Illuminance decrease according to the (a) inverse square law, (b) cosine law.

Moreover, the illuminance also decrease according to the cosine of the angle of incidence (θ), as shown in Fig. 1.2.5 (b), where E_0 is the illuminance corresponding to a surface normal to the incident light direction.

Luminous Efficacy and Efficiency

The luminous efficacy is defined as the ratio between the total luminous flux and the total radiant flux of an emitting source. In the SI, luminous efficacy has units of lumens per watt (lm/W). A related concept is that of luminous efficiency, that is usually used to evaluate the lighting efficiency of an artificial light source and is defined as the luminous flux emitted by a specific light source over the total energy it consumes in a time unit.

1.2.3. The "Quality" of Light

Light plays a fundamental role in people's everyday life. Eyesight is actually considered the most important sense for the human being, since about 80% of information is acquired at visual level.

As a matter of fact darkness typically somehow causes a feeling of fear, consequently increasing our stress level; moreover, the persistence of a low light condition can influence people mood and cause some discomfort.

There are a lot of scientific evidence of the close relationship between lighting and a multitude of biological, physiological and psychological effects, that are relevant for human performance and well being. Light affects our biological clock, however there is a threshold below which light is incapable to correctly regulate human circadian system.

Nowadays people usually spend the most of their time indoor, under artificial lights, in chronobiological darkness conditions, that can cause physical disturbances of various kinds. However, it is fundamental to understand that it is not a matter of quantity, but rather of quality of lighting.

Indeed, if providing a proper light level is clearly a necessary condition to achieve a good enlightenment, it is still not sufficient, since many other characteristics like light uniformity, spectral power, glare, etc... contributes to the actual lighting quality.

So, providing "good" lighting quality is much more than just guaranteeing an appropriate quantity of light. Therefore, it cannot simply expressed in terms of photometric measurements, since light perception is influenced by a number of different physical, physiological and psychological factors.

Moreover, the idea of "good" lighting usually varies depending on the specific place, its setting, its function, the characteristics of the people it is supposed to house, etc...

As a result, provide general criteria suitable for light quality analysis and find out prediction parameters to evaluate it is not a simple concern. However, some qualitative aspects, to be considered when estimating the suitability of lighting conditions, can be easily identified, as discussed also in [8]-[11].

Visual Performance

It is determined by the speed and accuracy in performing visual tasks, such as writing, reading, typing, interacting with other people, view image and videos, work with specific objects, etc... Visual performance is improved with increasing luminance, until reaching a

plateau above which any further illuminance increase does not actually produce any practical improvement.

Visual Comfort

To realize visually comfortable environments it is actually not a straightforward task, due to the several interrelated factors that can produce visual disturbances. Visual comfort, however, can be provided through a multitude of aspects, such as: a proper lighting distribution and light level, reduced glare and veiling reflections, the absence of excessive shadows and flickering effects, etc..

Color Characteristics

Light color characteristics are determined by light source emission spectrum, on one hand, and by the reflectance properties of the objects' surfaces on the other hand.
Light designer action field is clearly mainly aimed at addressing the former aspect, which is usually described by two different parameters, the so-called color temperature and the color rendering index. The first one is defined as the temperature of an ideal black body radiator that radiates light of comparable hue to that of the considered light source.
The second one is, instead, a quantitative measure of the ability of a light source to faithfully reproduce a set of test colors, compared to an ideal reference source of the same color temperature.

Psychological Aspects

Luminance can act at psychological level triggering emotions, affecting people's mood, increasing objects attractiveness. Therefore a lighting set-up that does not meet user expectations and does not produce positive feelings can be considered inappropriate, although it provides proper visual properties.
Moreover, lighting conditions can affect on productivity performance through motivation as shown in Fig. 1.2.6. So, lighting installations should be realized so as to allow people to work efficiently, safely and comfortably while trying to improve their productivity exploiting the non-visual aspects of light.

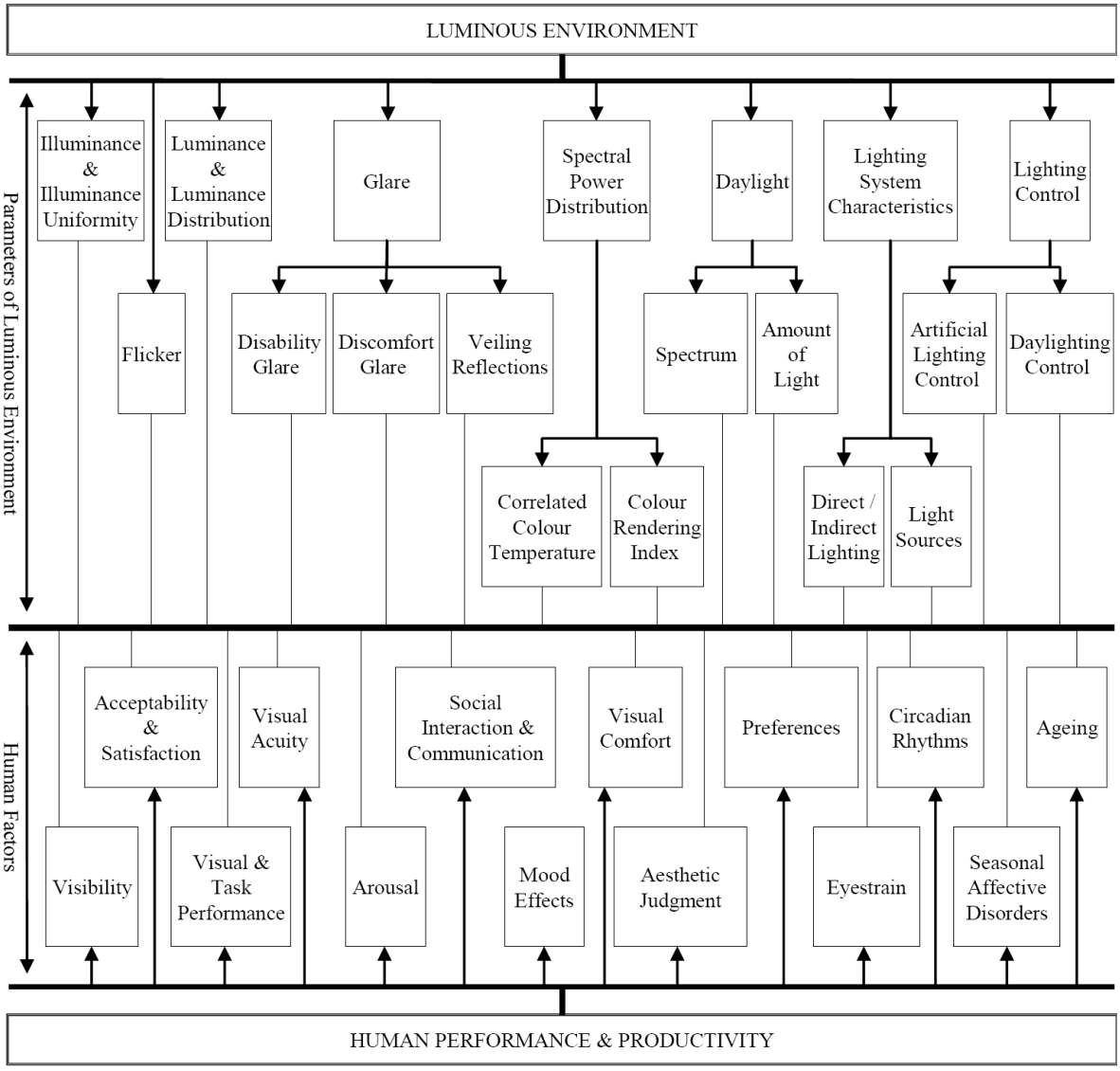


Fig. 1.2.6 – Interaction between human performance and luminous environment.

1.3. The Lighting Market

1.3.1. Lighting Applications

The world of lighting is characterized by a multitude of different kinds of applications, each of which has its peculiar properties and requirements that must be understood, studied and addressed. Only in this way it is, indeed, possible to meet the current market needs, enhance lighting systems and consequently improve people life quality.
As a reference, the most common lighting applications categories, are briefly reviewed here in the following, with the aim of pointing out their peculiar features.

Commercial Lighting
Lighting systems for commercial areas are usually aimed at creating a pleasant environment, capable of promoting positive customers feelings encouraging them to shop. In such situation light pays a fundamental role in enhancing product qualities, allowing to easily recognize the value of the brands on sale.
The most common luminaries involved in such kind of application are usually indoor spotlights, which allow the maximum positioning and set-up modification flexibility, and recessed luminaries [12], in order to hide lighting fixture and improve the aesthetics of the light source.

Industrial Lighting
Lighting in warehouses and industrial plants can improve safety, create flexible spaces, enhance working quality and productivity.
Due to the peculiar structure of such places, namely very large areas and high ceilings, however, the main required features in this kind of lighting application, are: long lifetime, minimum maintenance needs and high luminous efficiency, with the aim of minimizing costs. It is worth also to note that, in general, in this contest uniform lighting is not required. The typical lighting technique is indeed characterized by the use of a general low illuminance enlightenment, together with supplemental, more intense lighting concentrated in areas of specific interest such as the workstations.

Residential Lighting
In residential environments a multitude of different kinds of light sources are usually used, due to the huge variety of multidisciplinary activities that usually take place in such spaces.

A house, indeed, is a place where people can socialize, eat, sleep, play, study, work, relax, indulge in their hobbies, etc... For this reason, specific solutions, to match the requirements of each kind of activity, need to be adopted. As a result, in residential applications, the lighting conditions required in each particular case will be therefore achieved, from time to time, through the combined use of standard bulbs and more technical products.

Outdoor lighting

Outdoor lighting systems are intended to improve people safety, guaranteeing the visibility of obstacles and of potential dangerous situations, helping both vehicles and pedestrians and providing an effective contribution to the prevention of micro-criminality.

Common requirements for outdoor lighting typically call for the use of high efficiency and low maintenance cost street lamps. However, the specific needs of some urban elements (squares, monuments, parks, crossroads, etc...) must be obviously taken into account. In such cases the use of particular products like: pathway luminaries, floor-recessed luminaries, outdoor floodlights, etc... is actually recommended.

1.3.2. State of Art of Lighting Market

The launching of new energy programs by the European Community and the U.S. government, together with the release of new international efficiency standards and the advent of new technologies, herald a change in the lighting market in the upcoming years.

In order to better understand where the market is headed, it is worth to indentify the main characteristics of the current lighting market. A useful reference in this perspective is provided by the U.S. Department of Energy lighting market characterization report [5], released in January 2012 (DOE -LMC 2012), that illustrates the state of the art in this regard.

Such report, indeed, actually provides a snapshot of U.S. present situation making the inventory of all "lighting installed in the U.S. in stationary applications" in 2010. To this end, the market data have been split into four different sectors related to: residential, commercial, industrial buildings, and outdoor.

As it can be noticed, by observing the outcomes summarized in Table 1.3.1, about half of the electricity used for lighting is consumed in commercial buildings, while being the residential sector the second largest lighting energy consumer.

	Lamps	Average Daily Operating Hours	Wattage per Lamp	Annual Electricity Use (TWh)
Residential	5,811,769,000	1.8	46	175
Commercial	2,069,306,000	11.2	42	349
Industrial	144,251,000	13.0	75	58
Outdoor	178,374,000	11.7	151	118
Total	**8,203,700,000**	**4.7**	**48**	**700**

Table 1.3.1– Summary of U.S. lighting market characteristics in 2010. Source: DOE - LMC 2012.

It is worth to observe that the latter datum is given by the combination of the large base of installed lamps and their typically low efficiency, being incandescent lamp still the most broadly used in residential sector.

As a reference of the U.S. electricity consumption and lumen production by market segment and lamp type, the data reported Fig. 1.3.1 and Fig. 1.3.2 can be considered, respectively. Light sources have been grouped in six different lamp technology categories, that is: incandescent, halogen, compact fluorescent, linear fluorescent, high intensity discharge, and solid state/other.

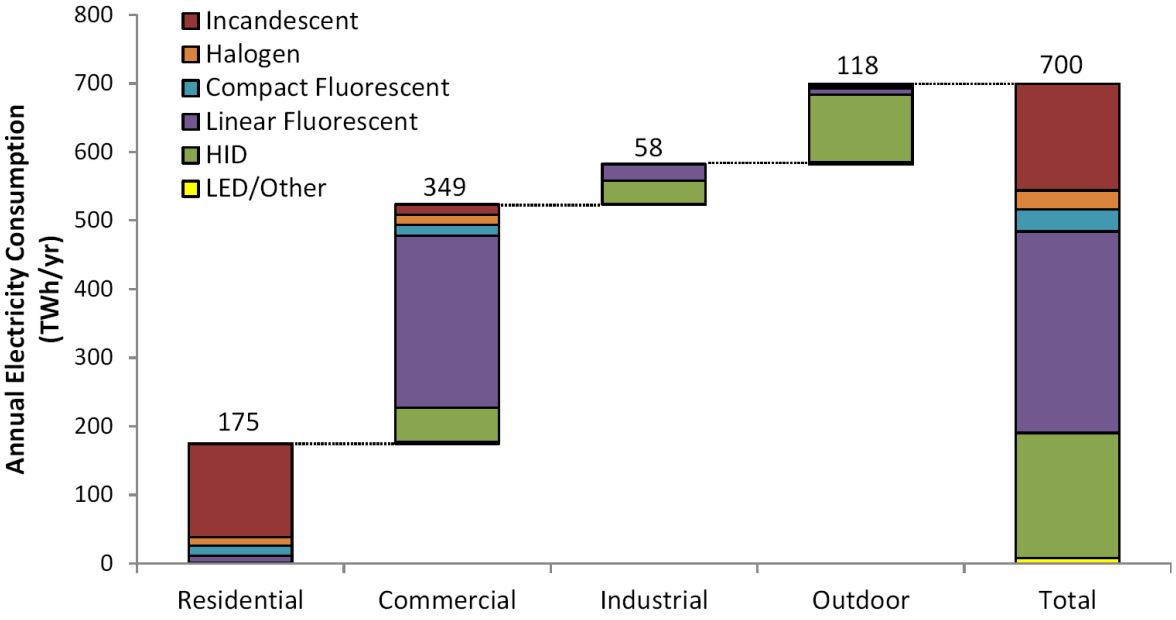


Fig. 1.3.1 – U.S. lighting electricity consumption by sector and lamp type in 2010. Source: DOE - LMC 2012.

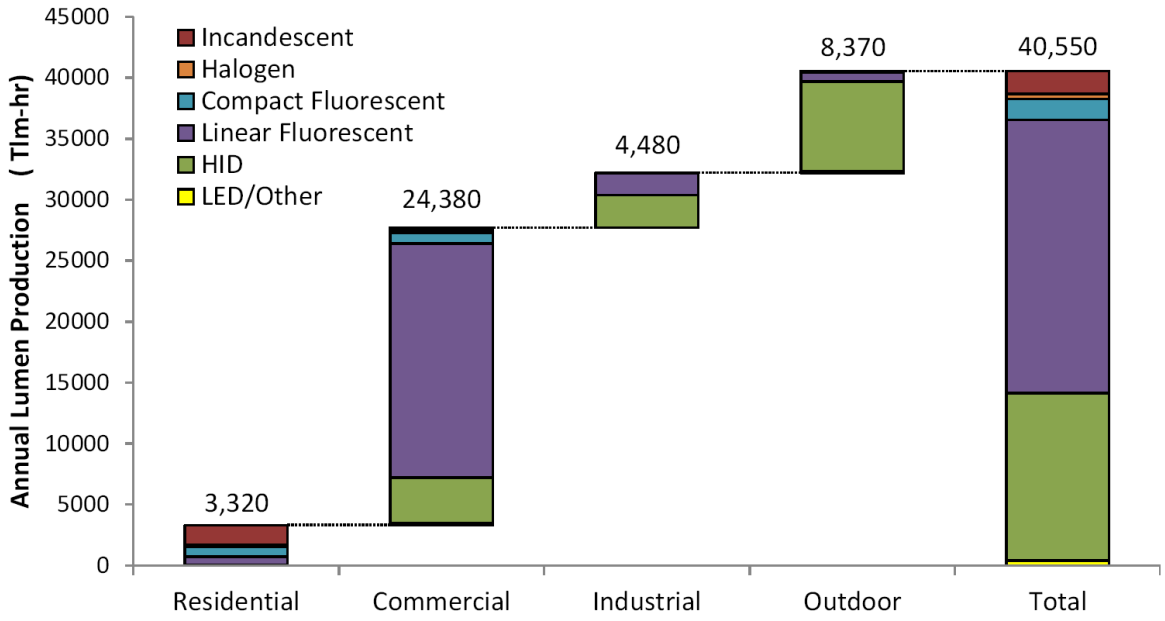


Fig. 1.3.2 – U.S. lumen production by sector and lamp type in 2010. Source: DOE - LMC 2012.

As it can be noticed, the relation between the energy consumed and the produced lumen is clearly unfavorable for incandescent lighting, while being highly beneficial in the case of efficient light sources, like HID, linear fluorescent and compact fluorescent lamps.

Another interesting reference is provided in Fig. 1.3.3, which shows the percentage of market share of each sector according to three different perspectives: the number of installed lamps, the energy consumption and the lumen production.

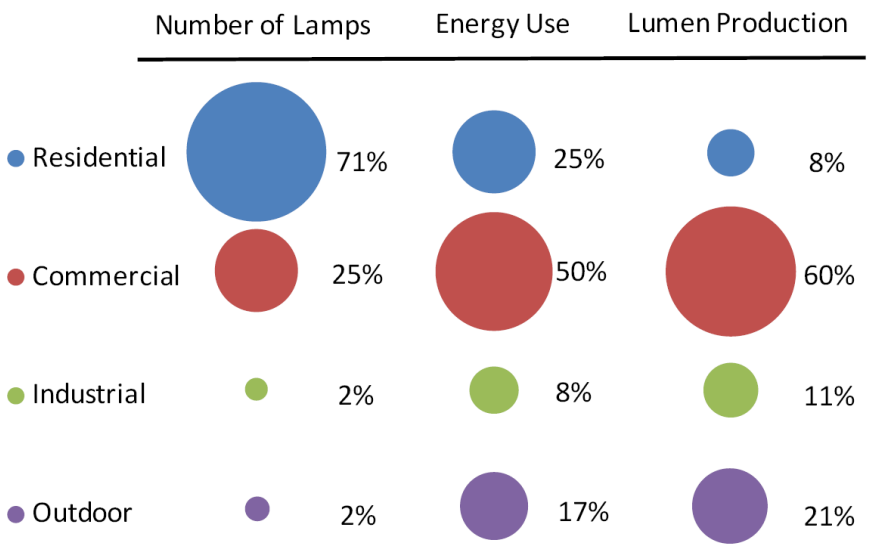


Fig. 1.3.3 – U.S. Lighting Lamp Inventory, Electricity Consumption and Lumen Production in 2010. Source: DOE - LMC 2012.

As can be seen, the lighting of commercial building clearly turns out to be the main sector as concerns energy use and lumen production, while being the most of lamps actually installed in the residential environment, because of the many multidisciplinary applications characterizing such segment.

Further details concerning the current U.S. lighting market can be derived also from the analysis, of Table 1.3.2.

	Residential	Commercial	Industrial	Outdoor	All Sectors
Incandescent	**62.0%**	**3.7%**	**0.3%**	**10.0%**	**45.1%**
General Service - A-type	34.9%	2.1%	0.3%		25.3%
General Service - Decorative	16.9%				11.9%
Reflector	7.5%	0.9%	0.0%		5.5%
Miscellaneous	2.8%	0.7%		10.0%	2.4%
Halogen	**4.4%**	**2.3%**	**0.0%**	**2.3%**	**3.8%**
General Service	0.5%	0.0%	0.0%		0.3%
Reflector	2.9%	0.9%	0.0%		2.3%
Low Voltage Display	0.3%	1.2%			0.5%
Miscellaneous	0.7%	0.1%	0.0%	2.3%	0.6%
Compact Fluorescent	**22.8%**	**10.4%**	**0.3%**	**6.8%**	**18.9%**
General Service - Screw	19.3%	2.0%	0.1%		14.2%
General Service - Pin	0.1%	6.6%	0.1%		1.7%
Reflector	2.0%	1.9%	0.1%		1.9%
Miscellaneous	1.4%			6.8%	1.1%
Linear Fluorescent	**9.9%**	**80.0%**	**89.2%**	**16.3%**	**29.1%**
T5	0.1%	5.2%	6.4%		1.5%
T8 Less than 4ft	0.1%	0.7%	0.5%		0.2%
T8 4ft	1.1%	43.9%	54.4%		12.8%
T8 Greater than 4ft	0.0%	1.3%	2.3%		0.4%
T12 Less than 4ft	0.1%	0.4%	0.0%		0.2%
T12 4ft	5.7%	19.8%	16.6%		9.3%
T12 Greater than 4ft	0.5%	5.3%	7.5%		1.8%
T8 U-Shaped	0.0%	2.2%	0.4%		0.6%
T12 U-Shaped	0.0%	0.5%	0.7%		0.1%
Miscellaneous	2.3%	0.6%	0.3%	16.3%	2.1%
High Intensity Discharge	**0.0%**	**1.7%**	**9.8%**	**52.2%**	**1.7%**
Mercury Vapor	0.0%	0.0%	1.0%	2.3%	0.1%
Metal Halide	0.0%	1.5%	6.5%	16.5%	0.8%
High Pressure Sodium	0.0%	0.2%	2.3%	32.5%	0.8%
Low Pressure Sodium		0.0%		0.8%	0.0%
Other	**0.9%**	**1.9%**	**0.4%**	**12.5%**	**1.4%**
LED	0.2%	1.8%	0.4%	10.8%	0.8%
Miscellaneous	0.8%	0.0%		1.7%	0.6%
TOTAL	**100%**	**100%**	**100%**	**100%**	**100%**

Table 1.3.2 – U.S. lighting market: distribution of lamps (percent of the total) by end-use Sector in 2010. Source: DOE - LMC 2012.

The data reported therein match the information accounting for the light sources distribution among the different sectors, with those related to the market shares of the different lighting technologies.

As it can be noticed, very interesting hints are provided about the strong variations in the distribution of the various lighting technologies according to the specific sector of application.

However, beside a static snapshot of present situation, it may be worth to catch also market trends. In this perspective, a suitable information, about lighting market evolution over the last decade, can be derived by comparing current data with the outcomes of the analogous DOE's report relative to the year 2001 [13].

The net result is a general decrease of average lamp wattages against an increment of lamp quantities, thanks to the use of more efficient lighting technologies.

A detailed description of such matter can be easily derived by observing Table 1.3.3 and Fig. 1.3.4, reporting the comparison between the data of the years 2001 and 2010 concerning the number of lamps and the average light sources efficacy for the different sectors.

	Lamps (million)		Average Daily Operating Hours		Wattage per Lamp		Electricity Use (TWh)	
	2001	2010	2001	2010	2001	2010	2001	2010
Residential	4,611	5,812	2.0	1.8	63	46	208	175
Commercial	1,966	2,069	9.9	11.2	56	42	391	349
Industrial	327	144	13.5	13.0	65	75	108	58
Outdoor	73	178	10.5	11.7	205	151	58	118
Total	**6,977**	**8,203**	**4.8**	**4.7**	**62**	**48**	**765**	**700**

Table 1.3.3 – Number of installed lamps by application sector. Comparison between the data collected in 2001and in 2010. Source: DOE - LMC 2012.

As it can be noticed, indeed, from 2001 to 2010 a general increment of the average light sources efficiency, in terms of the ratio between the emitted luminous flux and the dissipated power, actually involved all market sectors.

However, it is worth to observe that such improvement has been particularly noticeable in commercial building and outdoor applications, while the residential sector, despite the widespread of compact fluorescent lamps, still keeps suffering the large reliance upon incandescent light sources.

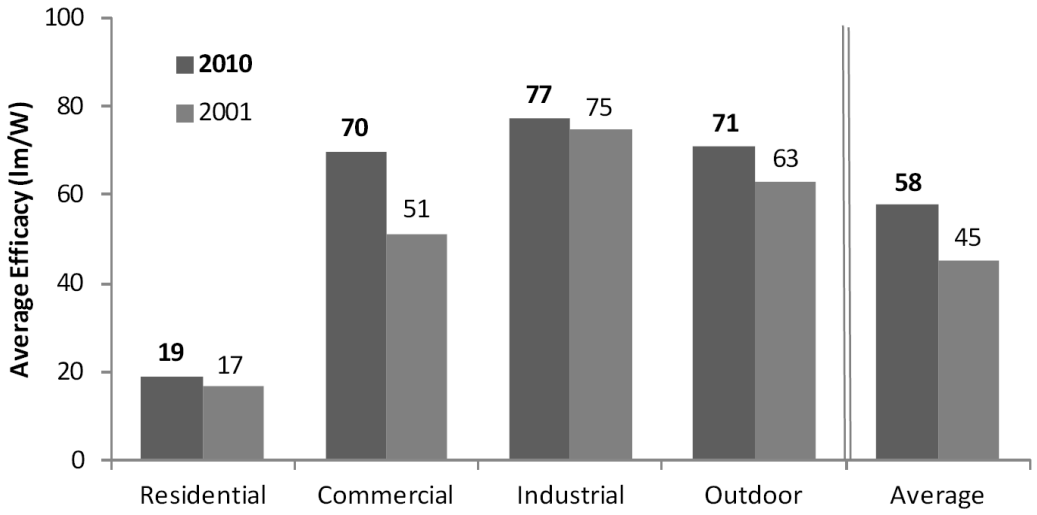


Fig. 1.3.4 – Average light sources efficacy by sector. . Comparison between the data collected in 2001and in 2010. Source: DOE - LMC 2012.

The actual result is that the average efficacy of the entire U.S. lighting stock has increased from 45 lm/W in 2001 to 58 lm/W in 2010, considering the overall lumen production over the whole energy consumed for lighting purposes.

It is interesting to observe that, although there has been a considerable migration towards energy efficient lighting technologies, solid state lighting is still limited to niche applications.

As can be inferred from Table 1.3.2, LED lamps diffusion is, indeed, currently relevant only for the outdoor use (10.8%), being employed most of all for traffic light signals as shown in Fig. 1.3.5. Nevertheless, solid state lighting market share is still negligible (<1%) as concerns the cumulative lighting market datum.

In many cases, the high initial price is the major responsible in deterring the consumer from buying energy efficient lighting products, despite the perspective of lower lifecycle costs.

It is therefore evident that solid state lighting technology still need a further research commitment to improve devices performances and decrease manufacturing costs. On the other hand, international governments can play a fundamental role in supporting investments in energy efficient lighting, also through more stringent lighting regulations, and public awareness campaigns.

Only in this way, it will indeed be possible to promote a further improvement of average lighting sources efficacy and realize potential energy saving, through a massive LEDs lighting market penetration in the upcoming years.

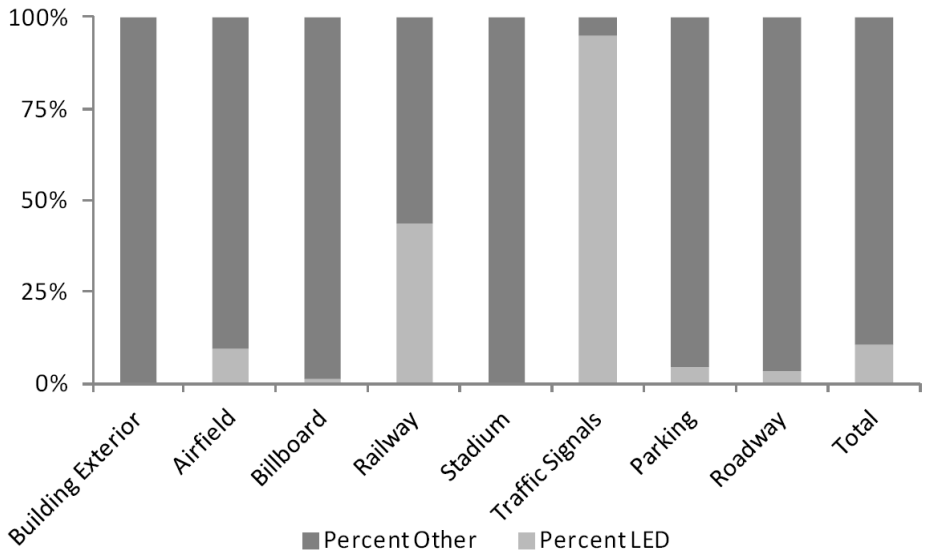


Fig. 1.3.5 – LED prevalence in the outdoor sector. Source: DOE - LMC 2012.

1.4. Solid State Lighting

1.4.1. The History of Lighting - a Brief Review

The relationship between human life and artificial lighting is a very ancient history, started about half million of years ago with the construction of the first torches built with coniferous tree branches.

The next step was the creation of primitive lamps made of hollow rocks initially filled with moss soaked in animal fat and then with fish, olive and other vegetal oils. However, only in 3000 BC became the construction of the first candles, although very different from those commonly known nowadays.

A significant step forward was then made about four thousand years later, in the tenth century AD, with the invention of the first kerosene lamp by Zakariya al-Razi and the consequent introduction of the first street lamps.

However, only with the Industrial Revolution the lighting sector actually received a major boost. The need to extend the work activity during the night hours, indeed, strongly encouraged the research of ever more effective light sources.

In 1780 the Swiss physicist Aimé Argand patented the Argand lamp, an oil lamp capable of emitting from 6 to 10 candela, then improved also with the addition of a glass chimney, Fig. 1.4.1 (32-34).

In the same years were carried out many studies on gas lamps, culminated with the invention of the first gas lamp by the Scottish engineer William Murdoch, in 1792.

The advent of the nineteenth and twentieth century finally brought a real lighting revolution, with a huge amount of significant advances in lighting technology. Among the many inventions, the most relevant ones are listed here in the following as useful reference.

- 1800 Carcel lamp, by Bernard Guillaume Carcel,
- 1802 Carbon arc lighting, first electric lamp, by Humphry Davy,
- 1835 first bulb based electric lighting system, demonstrated by James Bowman Lindsay,
- 1853 modern kerosene lamp, by Ignacy Lukasiewicz,
- 1867 first fluorescent lamp, demonstrated by A. E. Becquerel,
- 1875 first patented electric light bulb, by Henry Woodward,
- 1876 Yablochkov candle, the first practical carbon arc lamp for public street lighting, by Pavel Yablochkov,

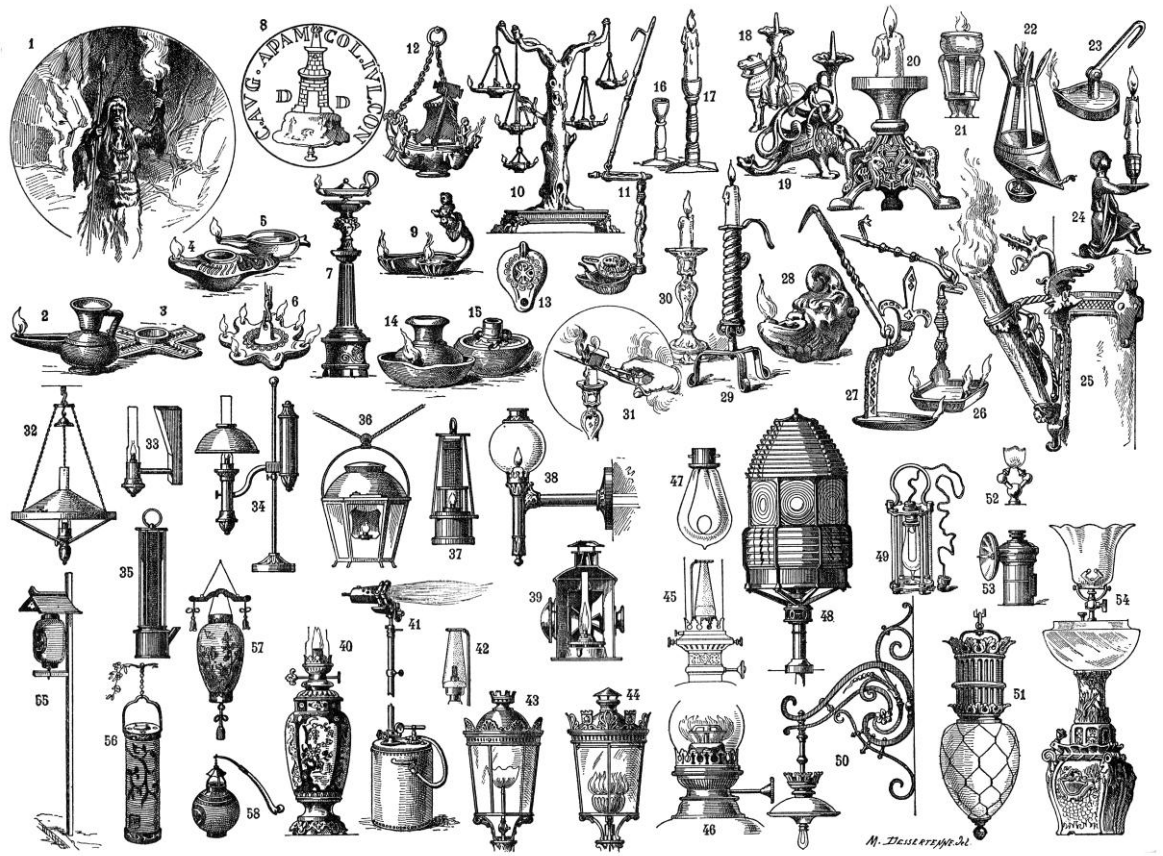


Fig. 1.4.1 – Lighting through the ages, illustration by Maurice Dessertenne .

Antiquity: 1. Prehistory. - 2-3. Egyptian - 4-5. Assyrian. 6-13. Roman. - 14-15. Carthaginian. - 16-17. Merovingian period. - Middle age and modern times: 19-20. 11th century. - 21. 12th century. - 22. 13th century. - 23-24. 14th century. - 25-26-27. 15th century. - 28. 16th century. - 29. 17th century. - 30-31. 18th century. - Contemporary period: 32. (original) Argand lamp. - 33-34. (Antoine Quinquet's improved) Argand lamp- 35. Stephenson (Geordie) lamp (mines). - 36. Street light. - 37. Davy lamp. - 38. Air-fed wick lamp (theatre). - 39. Railway lamp. - 40. Carcel lamp. - 41. Gasifier. - 42. Auer (gas) lamp with gas mantle. - 43. Gas street lighting (regular burner). - 44. Gas street lighting (high intensity burner). - 45. Auer (petrol) lamp. - 46. (Air-fed) petrol lamp. - 47. Incandescent (electricity). - 48. Lighthouse (electricity). - 49. Mine lamp (electricity). - 50. Incandescent (electricity) [street light]. - 51. Arc light (electricity). - 52. Acetylene lamp (burner). - 53. Acetylene lamp (bycicle). - 54. Acetylene lamp (lamp). - Japan: 55. Street light. - 56. Transportation (rickshaw). - 57. Lantern for funerals. - 58. Portable lantern.

- 1879 first patented carbon-thread incandescent lamp, by Thomas Edison and Joseph Wilson Swan (lasted 40 hours),
- 1880 first long lasting lightbulb (1500 hours), by Thomas Edison,
- 1893 introduction of the first commercial fully enclosed carbon arc lamp, by General Electric,
- 1894 creation of the Moore tube, precursor of electric gas discharge lamps, by D. McFarlane Moore,

- 1897 incandescent lamp with solid state electrolytes, by Walther Nernst,
- 1901 mercury-vapor lamp, demonstrated by Peter Cooper Hewitt,
- 1910 neon lighting, demonstrated by Georges Claude,
- 1926 first patented fluorescent lamp, by Edmund Germer,
- 1962 first practical visible-spectrum LED, developed by Nick Holonyak Jr.,
- 1981 first Compact Fluorescent Energy Saving Lamps with integrated ballast,
- sold by Philips,
- 1991 first fluorescent light bulb using magnetic induction, invented by Philips
- 1994 first commercial sulfur lamp,
- 1995 first white LED, with blue chip and additional phosphors, invented by Shuji Nakamura at Nichia labs.

The Origins of Solid State Lighting

As it can be noticed, in the 19th and 20th century lighting timeline previously described, solid state lighting has been taken into account twice, namely in correspondence of the development of the first visible-spectrum LED device, in 1962, and of the invention of the first white LED in 1995.

The origins of solid state lighting history, however, are much older, dating back to the experiments of Henry J. Round, one of Marconi's assistant in England, at the beginning of the twentieth century.

In February 1907 Round published a note to the editors of the "Electrical World" to describe a curious phenomenon, resulting in a bright glow from a carborundum diode (Fig. 1.4 2) however there was not follow up publications, so that more than the inventor of the LED, Round should be actually considered the discoverer of the electroluminescence.

A Note on Carborundum.

To the Editors of Electrical World:

SIRS:—During an investigation of the unsymmetrical passage of current through a contact of carborundum and other substances a curious phenomenon was noted. On applying a potential of 10 volts between two points on a crystal of carborundum, the crystal gave out a yellowish light. Only one or two specimens could be found which gave a bright glow on such a low voltage, but with 110 volts a large number could be found to glow. In some crystals only edges gave the light and others gave instead of a yellow light green, orange or blue. In all cases tested the glow appears to come from the negative pole, a bright blue-green spark appearing at the positive pole. In a single crystal, if contact is made near the center with the negative pole, and the positive pole is put in contact at any other place, only one section of the crystal will glow and that the same section wherever the positive pole is placed.

There seems to be some connection between the above effect and the e.m.f. produced by a junction of carborundum and another conductor when heated by a direct or alternating current; but the connection may be only secondary as an obvious explanation of the e.m.f. effect is the thermoelectric one. The writer would be glad of references to any published account of an investigation of this or any allied phenomena.

NEW YORK, N. Y. H. J. ROUND.

Fig. 1.4 2 - .A note on carborundum, Henry J. Round 1907.

In the issue of Nature Photonics of April 2007, Nikolay Zheludev actually gave credit to Oleg Vladimirovich Losev for being the real inventor of LED. However, despite the debate on paternity of solid state lighting, Losev is undoubtedly one of the leading figure in the history of LEDs [14].

He was born in 1903,from a high-ranking family in Imperial Russia and, although without receiving any formal education, during his short research carrier he published a number of papers and was granted of many patents of which he was the only author.

In particular, in the 1920s Losev studied light emission from forward biased zinc oxide and silicon carbide crystal rectifier diodes. His first paper on this topic, entitled "Luminous carborundum detector and detection with crystals", published in 1927 on a Russian journal of wireless telegraphy and telephony, essentially constitutes the official discovery of solid state lighting.

During his studies, Losev was able to establish the current threshold for the onset of light emission, to record the spectrum of the emitted light and to actually provide a comprehensive study of LEDs and their applications in a total of sixteen paper published between 1925 and 1930.

Such new devices had immediately a considerable success, however, because of their low power rating, for many years their application was limited to the fields of communications and electronics. It was only in the 1990s, with the introduction of the first high brightness white light emitting diodes, designed for higher power levels, that started the use in lighting applications.

1.4.2. LEDs: Operating Principles and White Light

An LED is essentially a junction of semiconductor materials doped with impurities with opposite sign charge. Typically the two doped regions are indicated with the letter "*n*" or "*p*" depending on the kind of majority carriers, namely electrons or holes, respectively.

In order to reach the thermodynamic equilibrium, a charge transfer will initially occur between the two regions, with the electrons flowing from the region *n* (or cathode) to the region *p* (or anode).

When the equilibrium is reached the junction interface will be characterized by the presence of a depletion region, devoid of carrier, and of a potential barrier, hindering the charge flowing from one region to the other (Fig. 1.4.3 (a)).

If a forward biasing voltage is applied to the junction ($v_P>0$ in Fig. 1.4.3 (b)), the potential barrier is reduced and the depletion region will be strengthened.

So, under forward bias, majority carriers from both sides of the junction are enabled to cross the depletion region, under the action of the electric field, and entering the other side of the junction, resulting in a net transfer of majority carriers between the two regions.
This process of charge injection actually produces an excess of electrons in the conduction band of the *p* doped region and of holes in the valence band of the *n* doped region, as shown in Fig. 1.4.3 (b).
This, consequently, highly improves the probability of recombination between such careers. The process according to which an electron falls across the energy gap towards a lower energy level actually matching a hole.
Two different kind of recombination can occur, namely radiative o non radiative, depending on whether it results in the emission of a photon or of a phonon.
When the potential energy is converted into a phonon, namely a vibration of the lattice, instead that into a photon, the actual result is heat production, rather than light emission.
For an optoelectronic device, that is intended to operate as a light source, radiative recombination is therefore actually desired. The ratio of the number of photons, emitted from the active region of the semiconductor chip, to the number of electrons, injected into the active region, is called "*internal quantum efficiency*".

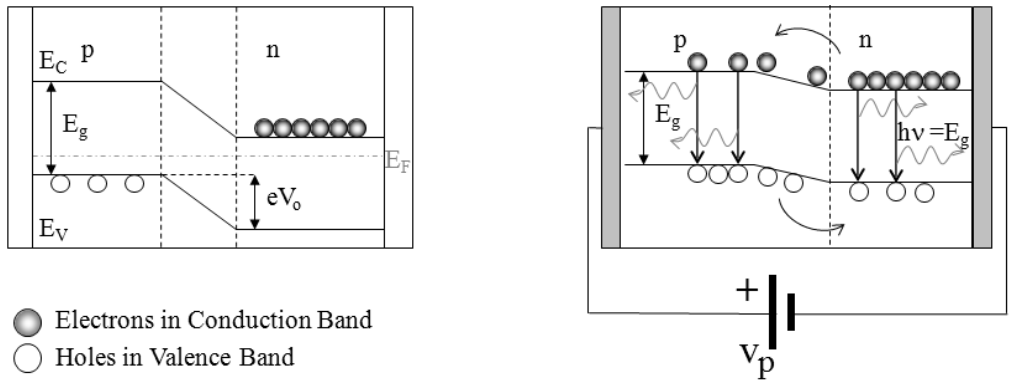


Fig. 1.4.3 – Band diagram of a pn junction at the equilibrium (a) null biasing, (b) forward biasing.

However this is not the only parameter concurring to the determination of device conversion efficiency, since a number of other power losses characterize the actual conversion process. In order to clarify this issue, the other two main contributors, to the overall LED chip efficiency, are briefly described here in the following.
The first one is the "*electrical efficiency*", that accounts for device ohmic losses associated with the semiconductor layers and the LED package materials. It essentially represents the

rate of the electrical charge carriers injected into the LED package that actually reach the active region of the LED.

The other important parameter is, instead, the "*light extraction efficiency*" which corresponds to the number of photons emitted from the semiconductor chip into the encapsulant, over the total number of photons generated in the active region. The product between the latter parameter and the internal quantum efficiency is called "*external quantum efficiency"*.

Additional efficiency losses will then occur within the LED package (whose typical structure is shown in Fig. 1.4.4) some of them will be briefly described as reference in the following.

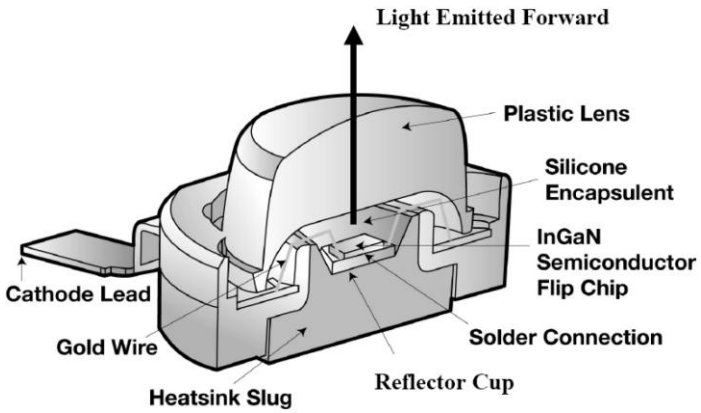


Fig. 1.4.4 – Typical structure of a LED device.

White Light LEDs

As previously explained, the light emitted by a solid state source is the result of radiative recombinations between majority and a minority free carriers within the semiconductor.

If such transitions take place between states in the conduction (E_c) and in the valence band (E_v), the energy of the emitted photons will correspond to the chip material band gap energy $E_g=E_c-E_v$.

As a result, the wavelength (λ) of the light emitted, and thus its color, will also depend on the band gap energy, according to the law:

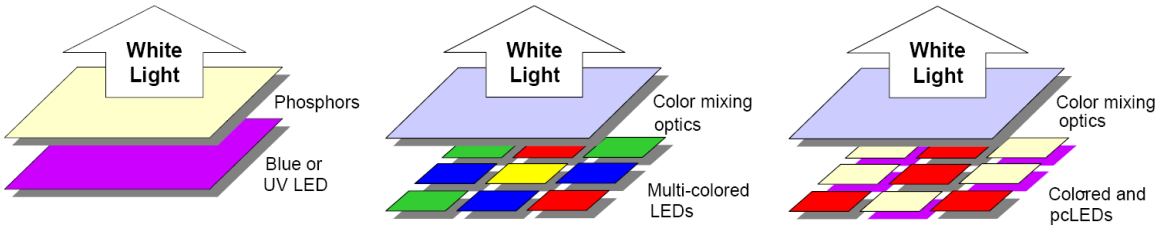
$$\lambda = \frac{h \cdot c}{E_g} \tag{1.4.1}$$

where h is the Planck's constant and c is the speed of light.

So, LEDs actually result to be devices with a narrow band optical emission. Advances in materials science and manufacturing have nowadays enabled making devices emitting in different regions of the spectrum.

However, for general lighting purposes, white light emission is actually necessary ([15]-[17]), so that multiple colors will have to be controllably mixed in order to achieve this goal.

To this end, three main kinds of approach can be considered, as shown in Fig. 1.4.5, namely: phosphor-conversion, discrete color mixing and a hybrid approach given by the combination of both previous approaches.



(a) *(b)* *(c)*

Fig. 1.4.5 – Approaches for the realization of a white light emitting LED: (a) Phosphor-Converted LED, (b) Color-Mixed LED, (c) Hybrid Method LED.

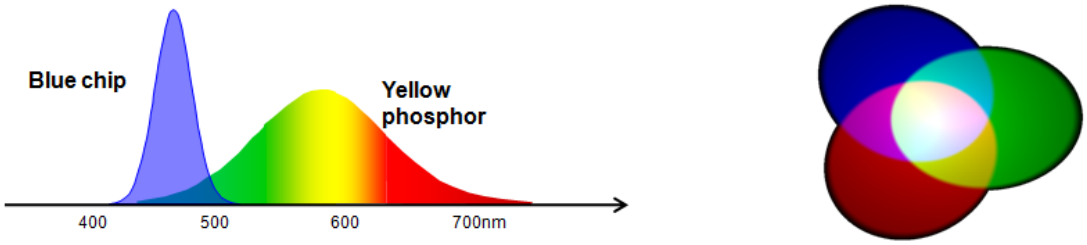
According to the first approach, white light is generated by mixing the blue light directly emitted by the chip with the down-converted yellow light emitted by the phosphors (Fig. 1.4.6 (a)), usually placed on the LED emission surface. Although currently the most used, such approach suffers the efficacy limitations deriving by the fact that chip emitted light has to be absorbed, converted and re-emitted by the phosphors.

The efficiency with which phosphors convert the wavelength of the absorbed light is referred as "*phosphor conversion efficiency*" and includes quantum efficiency of the phosphor and the Stokes loss of the conversion process.

As a reference, it can be considered that the typical values of the overall source efficiency and nominal efficacy of such devices are currently equal to 26% and 98lm/W, with a projected potential improvement allowing the achievement of an overall source efficiency equal to 54% and a nominal efficacy of 199lm/W.

Conversion issues can be avoided with the discrete color mixed approach, according to which white light is obtained by the additive mix of multiple LED monochromatic sources, Fig. 1.4.6 (b). Unfortunately, green and amber LEDs, needed to reach this aim, suffer from

poor internal quantum efficiency. So, even if color mixed approach theoretically offers better efficacy, currently phosphor-converted LEDs are still typically capable of achieving higher efficiency levels.



(a) *(b)*

Fig. 1.4.6 – Creating white light:(a) phosphor conversion, (b) additive mixing of monochromatic sources.

With reference to the optical losses incurred while creating white light through color mixing, the "*color-mixing/scattering efficiency*" is defined as the ratio of the photons exiting the encapsulant to the photons injected into the encapsulant.
The current overall source efficiency and nominal efficacy of such devices are typically equal to 15% and 97lm/W, respectively. However, according to the expected improvements of green and amber emitters, their values are estimated to increase until reaching about 67% and 266lm/W, respectively.

Finally, as concerns the hybrid approach, based on the use of both phosphor converted and monochromatic LEDs, the idea is to combine the benefit of both previous approaches to achieve higher efficiency and enhanced color quality.

1.4.3. Solid State Lighting: Issues and Benefits

In order to understand the potential of solid state technology for lighting applications, it is worth to analyze its current performance and projected improvement, with reference to the present performance of other widespread technologies and their evolution over the last decades.
The chart reported in Fig. 1.4.7, presented in the "*Solid-State Lighting Research and Development: Multi-Year Program Plan*" [18], of the U.S. Department of Energy released in April 2012 (DOE-MYPP 2012), shows exactly these trends, and can be therefore taken into account as a suitable reference.

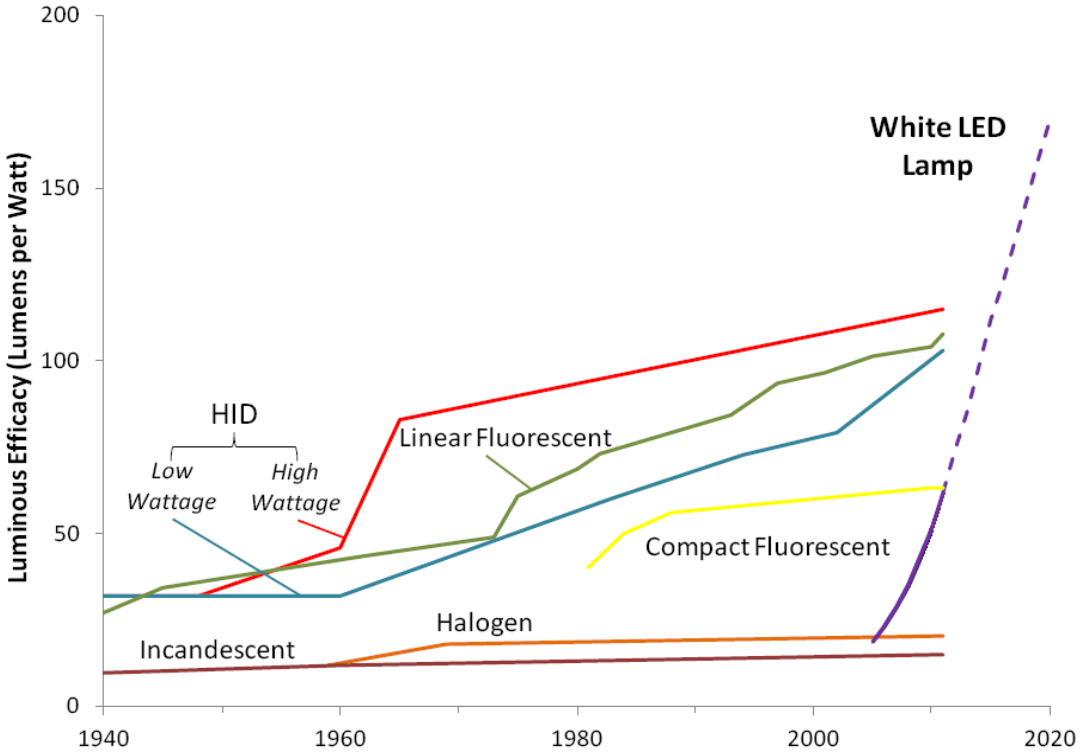


Fig. 1.4.7 – Historical and predicted efficacy of light sources. Source: Navigant Consulting, Inc - Updated Lumileds chart with data from product catalogues and press releases. Source: DOE - MYPP 2012.

As it can be noticed, the considerable improvement of other conventional high efficiency lighting technologies still hinders market penetration of solid state lighting.

Indeed, although LEDs are nowadays accredited to be the most efficient light source, overall commercial LED lamps efficacy (i.e. including LED driver circuitry and other optical, thermal and mechanical components effects, besides the LED package) still need some further improvements.

As a matter of facts, even if the luminous efficacy of LED luminaires has surpassed that of the incandescent and compact fluorescent lamps, it still lags behind other conventional efficient lighting solutions, like HID and linear fluorescent lamps.

Fortunately, commercial LEDs are still far from the estimated limit efficacy of this technology and still have therefore a considerable headroom for improvement ([19], [20]).

Reports on prototype lamps with efficacy exceeding 150 lm/W have already been presented, so that future commercial LED-based light sources have the potential to overcome the efficacy of the most efficient conventional light sources.

It is worth to note that improving luminous efficacy is not actually only a matter of energy saving.

Higher LED efficiency values will, indeed, consequently reduce the number of devices necessary for a given lighting application and relax also thermal management requirements of LED luminaires.

The net result will be therefore a significant reduction of the cost of solid state lighting sources, fostering their market penetration and allowing LEDs to outperform the competition from other technologies.

A closer inspection, indeed, reveals a considerable gap between the current cost of LEDs compared to that of their major competitors.

As a reference the data listed in Table 1.4.1 can be considered. As it can be noticed, on a base unit of dollars per kilo-lumen, LED lamps results to be about twelve times more expansive than halogen bulbs and about three times compared to equivalent dimmable compact fluorescent lamps.

TABLE 1.4.1 - COST PER KILO-LUMEN OF THE MOST WIDESPREAD LAMP REPLACEMENTS

Halogen Lamp (A19 43W; 750 lumens)	$2.5 per kilolumen
CFL (13W; 800 lumens)	$2 per kilolumen
CFL (13W; 800 lumens dimmable)	$10 per kilolumen
Fluorescent Lamp and Ballast System (F32T8)	$4 per kilolumen
LED Lamp (A19 60W; 800 lumens dimmable)	$30 per kilolumen

It is therefore evident that a substantial cost reduction is desirable besides an overall performance improvement. If indeed it is true that, rather than the initial price, the actual cost of a lamp is its lifecycle cost, a reduced first cost barrier will shorten the payback time, that is the parameter that ultimately influences the choice of most of the costumers.

As a further reference of LED technology real potentialities, a comparison between the current cost of an integrated white light LED replacement lamp and of a 13W compact fluorescent lamp, according to the DOE - MYPP 2012 projection, is shown in Fig. 1.4.8.

So, by matching the projection data, describing the expected advances in solid state lighting technology performance and costs, reported in Fig. 1.4.7 and Fig. 1.4.8, LED based lamps seem actually destined to definitely succeed within the next decades.

In order to demonstrate the importance of solid state lighting technology, the projected energy savings, deriving from the widespread of LED based lighting source has been computed in a study of the lighting market characterization, [5] (DOE - LMC 2012).

As can be observed from the corresponding graph, here shown in Fig. 1.4.9, the effects of a continued market penetration of LED lighting through the year 2030 have been estimated, using an econometric model of the U.S. lighting market.

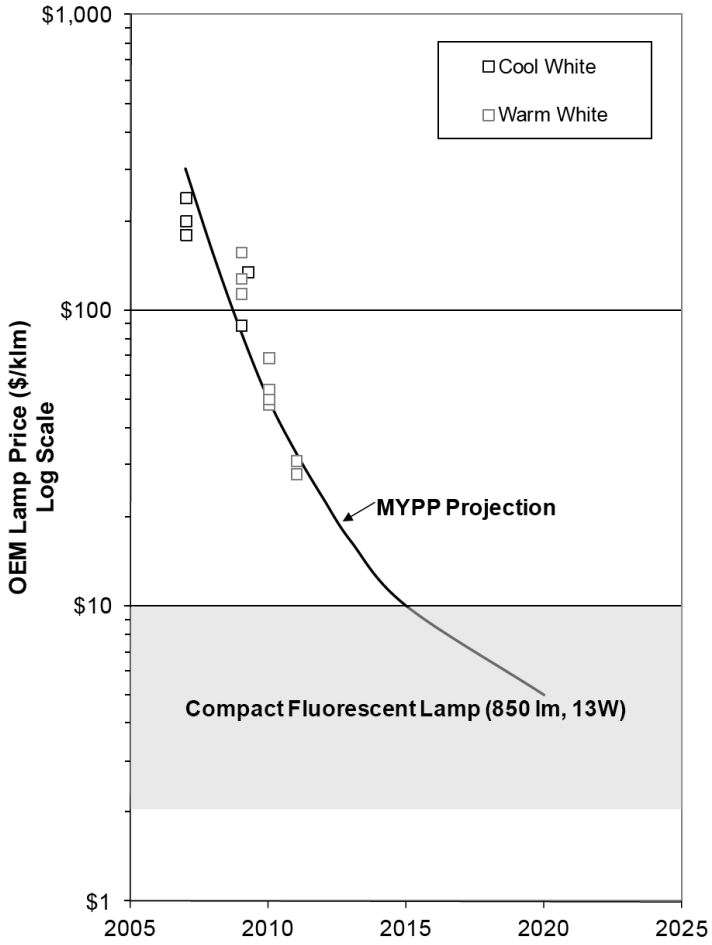


Fig. 1.4.8 – White Light Integrated LED Lamp Price Projection (Logarithmic Scale).
Source: DOE - MYPP 2012.

In particular, it has been investigated the potential decrease of the electricity consumed for lighting purposes, resulting from the projected growing presence of LED based luminaires in the lighting market.

The actual result is that, if LED lighting technology will meet its expected efficacy, lifetime and cost targets, its projected adoption will produce considerable electricity savings.

In particular, a decrease equal to 46% of the total electricity used for lighting has been forecasted, by the year 2030, with respect to a scenario assuming no additional market penetration of LED lighting.

To have a practical reference, this would actually mean an U.S. energy saving of approximately 300 terawatt-hours, roughly equivalent to about 30 billion dollars saved in 2030 alone.

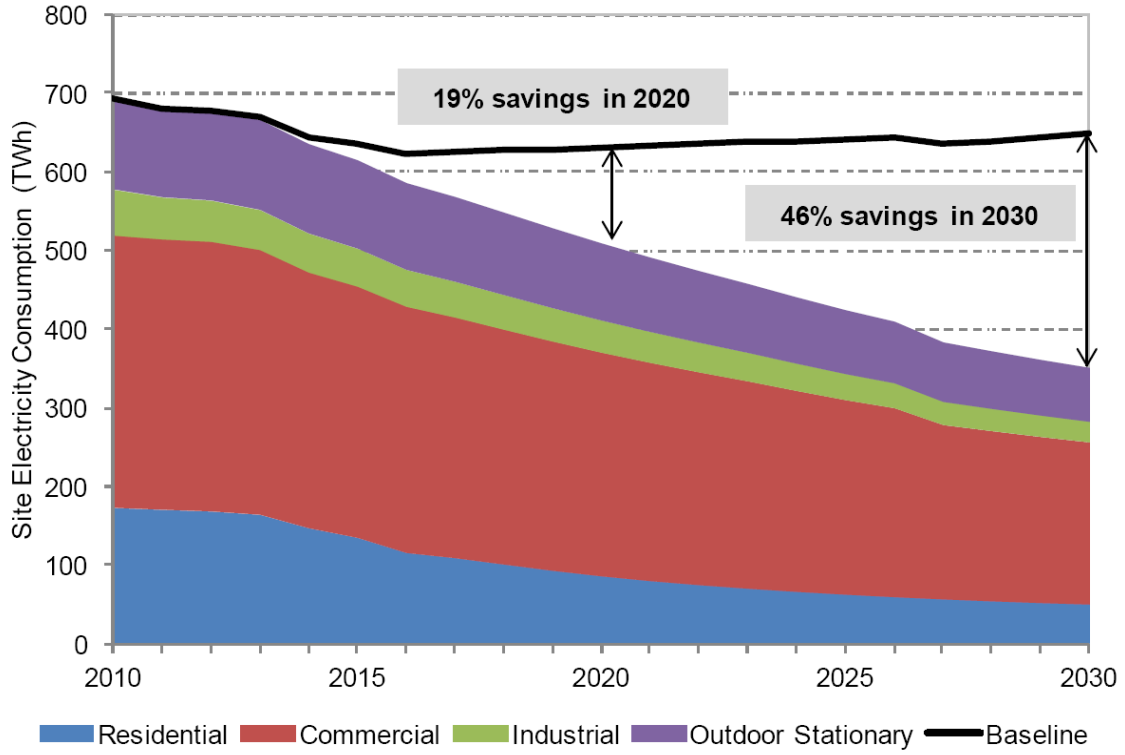


Fig. 1.4.9 – Forecasted U.S. Lighting Energy Consumption and Savings, from 2010 to 2030.
Source: Energy Savings Potential of Solid-State Lighting in General Illumination Applications. Prepared by Navigant Consulting, Inc. for the Department of Energy. Washington D.C. January 2012.

1.5. Solid State Lighting Driving

1.5.1. LED Driving Issues

When approaching solid state lighting, the light source should be treated as a complex system, in which a number of different issues have to be properly addressed along the conversion path within the input power and the white emitted light.

Most lighting systems, indeed include power conversion stage, current regulation and control circuitry, thermal management and secondary optics, as shown in the basic scheme of Fig. 1.5.1.

In the description proposed so far, the attention has been focused mainly on LEDs operation and white light emission issues.

However, besides these concerns, also the other mentioned aspects will have to be properly addressed, in order to minimize possible negative effects on the overall lighting fixture performance thus improving its efficiency and reliability.

As a matter of facts, thermal issue plays a really relevant role in minimizing thermal stresses, stabilizing the characteristics of the emitted light and consequently preventing the early ageing of the light source, as shown in Fig. 1.5.2.

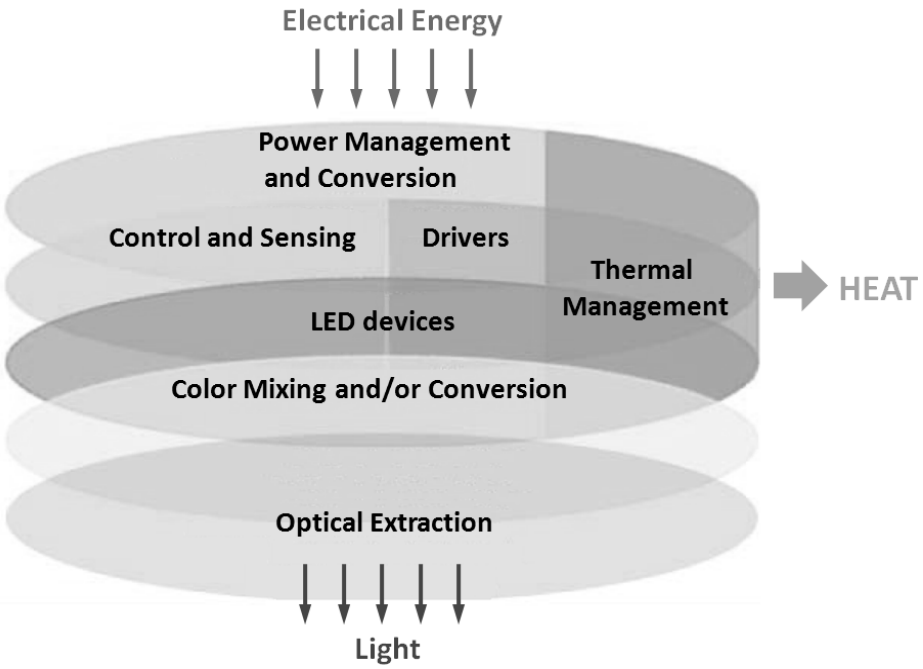
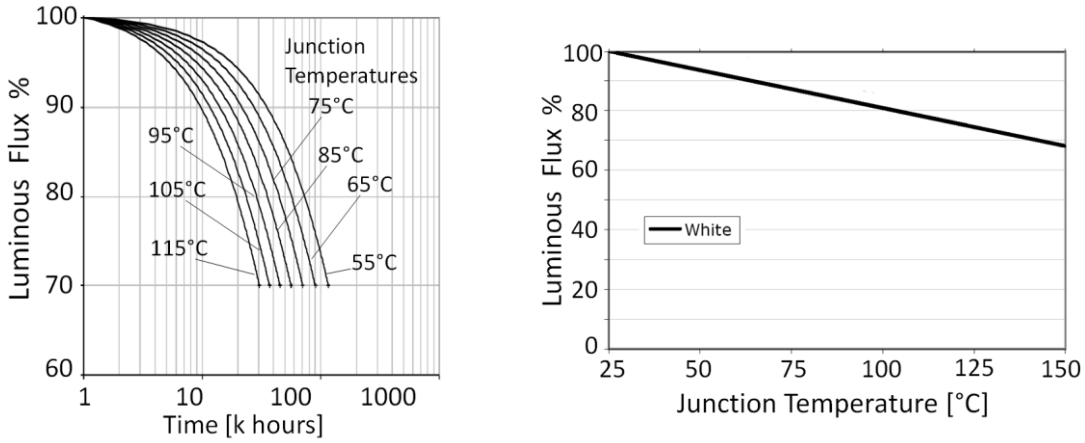


Fig. 1.5.1 – Equivalent scheme of the overall solid state lighting system..



(a) *(b)*

Fig. 1.5.2 – Examples of (a) LED ageing for different junction temperatures and (b) Luminous flux variation as a function of LED junction temperature.

Such matter, actually calls for a proper lamp design, aimed at dissipating the heat produced by non radiative recombination, ohmic losses and a number of other inefficiencies, with obvious consequences on lamp compactness and cost.

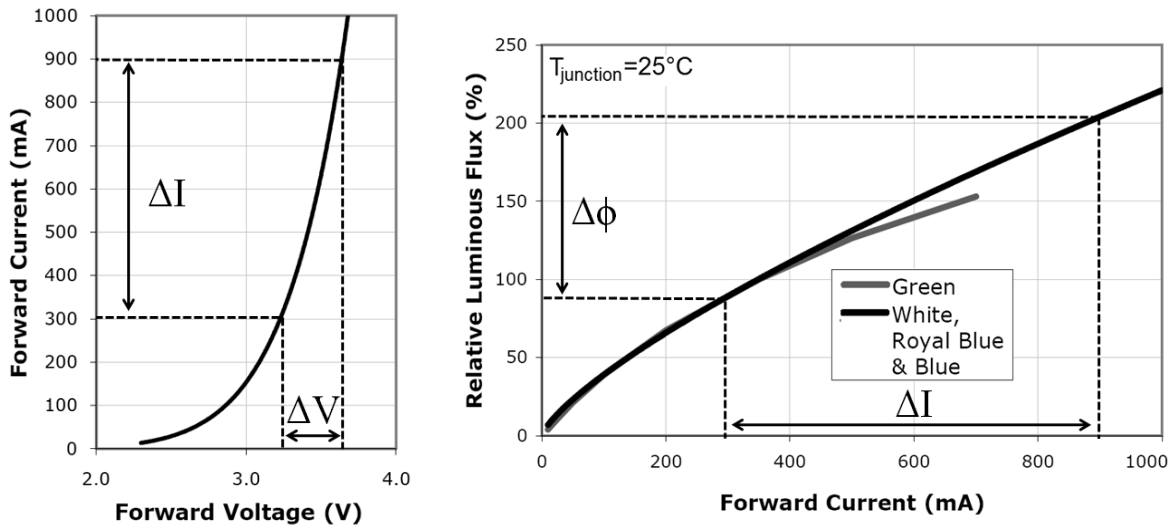
On the other hand, as concerns power conversion and LED current regulation and control circuitry, many different solutions can be employed depending on the type and on the power rating of the target application.

Besides the obvious differences between the various applications, however, it is important to clarify what are the basic challenges deriving from LED driving, so as to identify the actual functions that the power conversion and control stage is called to perform.

In this perspective, it is worth to remember that, being an LED basically a diode, it will be characterized by a specific threshold bias voltage, over which it will exhibit a steep voltage- current curve, as shown in Fig. 1.5.3 (a).

Since the emitted luminous flux actually depends on LED forward current Fig. 1.5.3 (b), it can be easily inferred that LEDs current has to be properly regulated in order to achieve the desired light emission.

The first way of approaching such issue is to use LED current-voltage characteristic to derive the forward voltage necessary to get the desired current level and consequently voltage biasing the device according to such value. However, as it can be noticed, with this solution even slight variations of the bias voltage will produce large current changes, with evident effects on the emitted luminous flux.



(a) *(b)*

Fig. 1.5.3 – (a)Voltage-current and (b) Flux-current characteristics of a Cree XR-E HBLED.

The main function of a LED driver will be therefore to limit the forward current variation, regardless of input and output varying conditions, in order to meet the design specifications.

The easiest way to reach this goal, commonly used in the past with low power devices, is to place a ballast resistor in series with the LEDs, in order to get a rough current limitation.

However, with modern high power devices, such technique has clearly become unusable, in order to avoid affecting the overall system efficiency, because of the resulting high conduction losses.

A smarter approach is to drive LED forward current, rather than its voltage. In practice this actually turns in sensing LED current and consequently regulating the resulting sensing signal, so as to control lamp brightness.

To this end, "passive" regulation, although very simple and cheap, would be nowadays impractical, due to the considerable associated losses, as already observed, and to the need of some kind of LED current control in order to allow light brightness control.

However, also "active" solutions, relying on the use of linear regulators will not suit the typical applications involving the use of HBLEDs. In such cases, indeed, due to the typical voltage and current levels, linear regulators would suffer from a very poor operating efficiency, especially in correspondence of high input voltage levels.

In order to overcome this problem switched mode regulators can be employed, even if at cost of a higher component count and therefore of a higher complexity and higher costs.

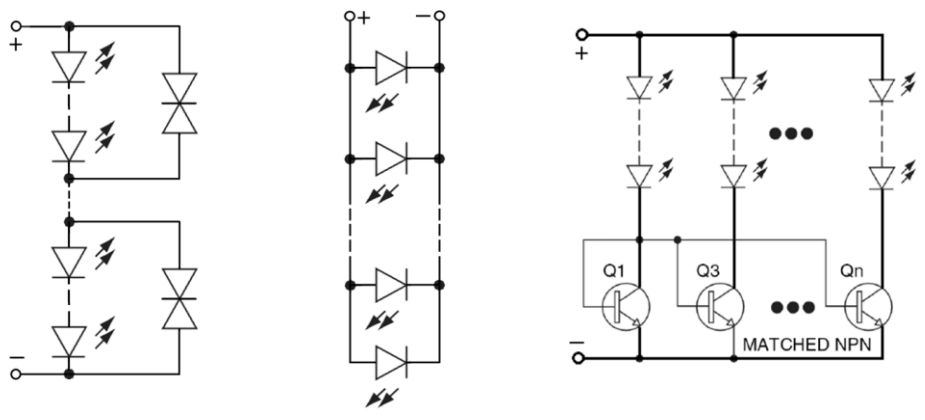
Besides the higher efficiency, switched mode power converters also offer the capability of adjusting the input voltage level, that is to step-up or to step-down its value, in order to meet load requirements.

It is worth to note that the latter will be clearly strongly dependent on the arrangement of LEDs as well as on the characteristics of the devices used.

Among the many different possible configurations, three main kinds of LEDs connection can be identified, namely: series, parallel and series/parallel arrangements.

In the first case all LED devices are polarized by the same current. This favors an homogeneous light emission and results in a higher series resistance, actually reducing current dependence on the variations of the voltage applied at the terminals of the LED string. The main drawback of such kind of approach is the low reliability, due to the fact that, in case of failure of a single device causing an open circuit, the whole LED string would be actually affected. In order to prevent such eventuality, usually the LEDs are subdivided in groups of few units. Each group is paralleled with a bypass element, that starts conducting in event of a failure within the corresponding group, as shown in Fig. 1.5.4 (a). This adjustment allows to limit the damage to the only devices belonging to the group that is involved in the failure.

The opposite approach is to connect all the LEDs in parallel (Fig. 1.5.4 (b)). This technique offers a high reliability, because although a device would fail and open, the other LEDs composing the lamp could keep working and enlightening. However, since according to such configuration all devices are biased by the same voltage level, possible differences in devices threshold voltage will consequently turn into different forward LED currents, actually resulting in non-homogeneous light emission.



(a) *(b)* *(c)*

Fig. 1.5.4 – LED connections:(a) series (with bypass), (b) parallel and (c) series/parallel (with current sharing network)

Finally, an intermediate solution can be realized by combining series and parallel connection of LEDs. In this case the devices belonging to the same string will be driven by the same current, while the different paralleled string will be uniformly voltage biased. Also in this case, current differences can eventually occur, depending on the characteristics of the devices composing each LED string, calling for the introduction of current sharing techniques (Fig. 1.5.4 (c)).

Depending on the specific requirements of each application, different topologies can be selected to implement switching mode regulators. Some basic examples of non isolated configurations, namely buck, boost and buck-boost topologies, are reported in Fig. 1.5.5.

For LED driving purposes, such regulators can be conveniently configured as constant current sources, through a feedback control of LED current, that allows a tight output regulation.

Another drawback of switched mode regulators, that is worth to mention, is the generation of electromagnetic interferences, due to the high frequency variation of current and voltage levels. This consequently forces to the use of proper filters, in order to comply with the requirements of the EMI standards, further increasing the driving stage complexity, volume and cost.

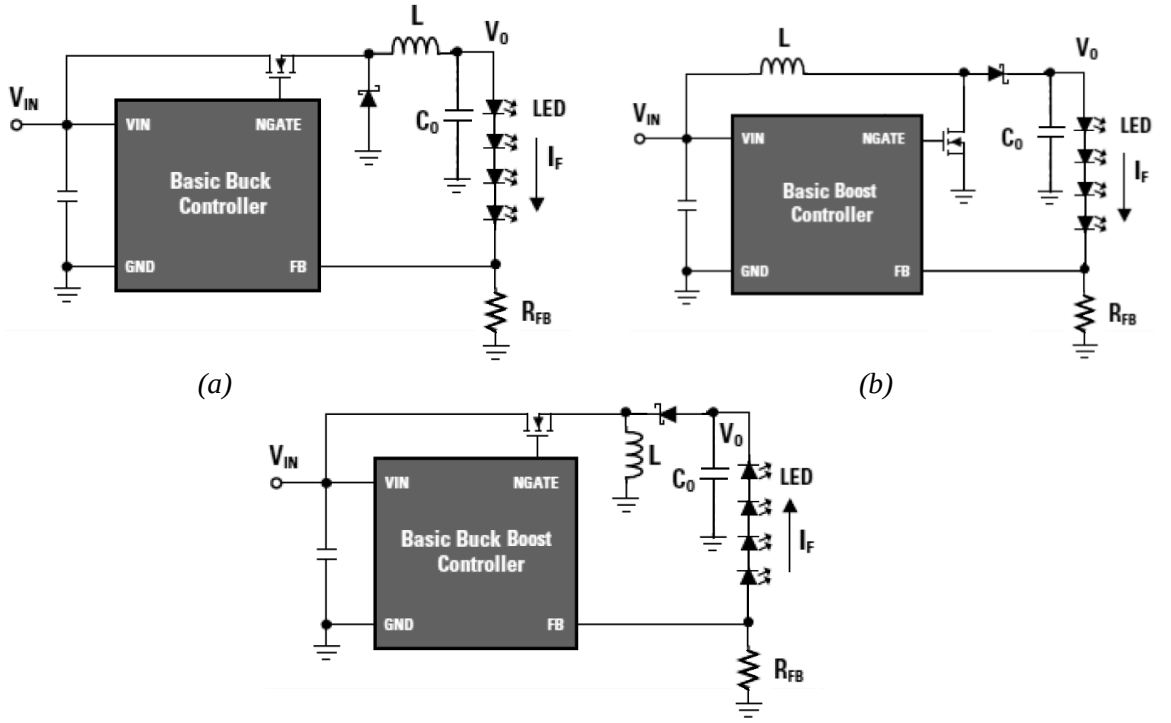


Fig. 1.5.5 – Examples of switching mode regulators: (a) buck, (b) boost and (c) buck-boost configurations

A particular sector in which the use of switching mode power supplies is considered almost essential is that concerning the offline driving of HBLED based light source, that is actually the topic of the research activity described in the following in this thesis.

1.5.2. Offline LED Driving Solutions

In offline applications LED lamps are fed directly from the mains, thanks to the use of properly controlled power converters. The actual configuration of such power conversion and regulation stages strongly varies, depending on the specific requirements of the considered application, the power level and the luminaire specifications.
Anyway, despite the specific implementation, the design of offline HBLED ballast will actually force to tackle, at least, three main issues, namely: circuit complexity, step down capability and line side converter spectral performance.

As concerns the last aspect, AC/DC HBLED driver has to be designed so as to comply with harmonic and efficiency standards [21], [21]. Although the situation, as regards LED driver legislation, is continuously evolving, the main harmonic standards currently considered as reference are the IEC 61000-3-2 for the European market and the ANSI C82.77-2002 harmonic emission limits for the U.S.A. Moreover, in recent years, energy quality and efficiency standards, such as Energy Star and allied indications, actually calling for improved power factor and efficiency levels, began to be taken into account, with the aim of developing better and better lighting fixtures.

As regards, instead, the need to lower the input voltage, it should be observed that step-down feature can be effectively provided through a number of different isolated or non isolated buck or buck-boost based topologies. The actual step-down requirements will depend on the input line voltage characteristics (i.e. RMS value and relative tolerance) as well as on load specifications, that is: the type of LED used, the number of devices and their arrangement.

Finally, as concerns ballast complexity, it may be worth to make some considerations about AC/DC HBLED driver structure. First of all, it is worth to keep in mind that circuit complexity minimization is mainly aimed at increasing ballast power density, improving its efficiency and reducing its costs, so as to favor solid state lighting widespread, as discussed in the previous paragraphs.

From this perspective, many different ways of approaching the offline driving issue can be identified. Anyway, in an effort to provide a general description of such matter, three main kinds of solution can be identified, that are briefly discussed here in the following.

The Single Stage Approach

The simplest configuration, that actually minimize converter complexity, relies on the use of a single conversion stage. According to this solution, the multiple tasks, concerning the achievement of proper line side performance, output regulation and possibly also the galvanic isolation, are performed by the same power stage. In such configuration an energy storage element can be placed in parallel to the LED load, as shown in Fig. 1.5.6, so as to compensate for the pulsating input power absorbed from the mains.

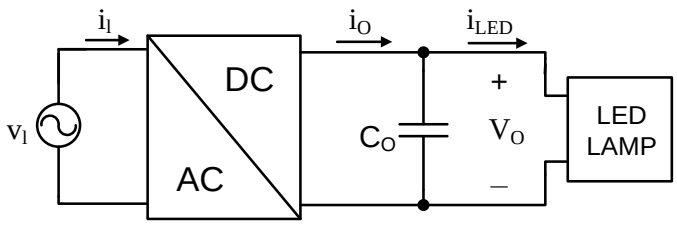


Fig. 1.5.6 – Simplified scheme of the offline single stage driving approach.

Although very simple, cost-effective and compact, this kind of configuration suffers, however, some drawbacks. The main disadvantages derive essentially from the large variability of driver operating conditions, that complicates design optimization. Being the AC/DC converter devoid of low frequency energy storage elements, indeed, the input power ripple will be entirely delivered to the output filter capacitor.
As a result the converter will have to be capable of properly managing the large input variation, actually forcing to an oversizing of its components. Moreover, it is also worth to note that the residual output voltage ripple will actually result in a LED current harmonic at twice the line frequency, negatively affecting lamp performance.
Such kind of solution results to be particularly suitable in low power applications (<12W), such as bulb replacement, desk and cabinet lamps, etc..., in which cost minimization and high compactness are considered a must.

The Double Integrated Stage Approach

In medium power applications, like for example down lighting, decorative lighting fixtures, ceiling fans etc..., usually characterized by power levels roughly ranging between 12W and 60W, the previous solution could be unsuitable.

In such cases, indeed, an optimized converter operation actually becomes a major requirement in order to prevent detrimental effects on ballast efficiency. Moreover also line side performance actually become a relevant concern, calling for some kind of input power factor correction in order to guarantee the compliance with harmonics and energy saving standards.

The optimal solution, in this case, in order to achieve the best performance levels for both the above mentioned tasks, would clearly be the selection of a two stage configuration.

However, being high compactness and low cost still applicable requirements, a suitable trade off could be the use of an integrated configuration.

Such solution is essentially given by the combination of two different conversion stages sharing the same main controlled switch.

In this way it is possible to retain most of the two stage configuration beneficial effects, while saving one active switch and the whole related driving and control circuitry.

Moreover, such kind of integrated configuration gives the possibility to move the twice the line frequency energy storage element away from the load. As a matter of facts it can be actually shifted upstream between the two semi-stages, as shown in Fig. 1.5.7, so that the input energy will be first stored in the BUS capacitor (C_B) and then delivered to the load.

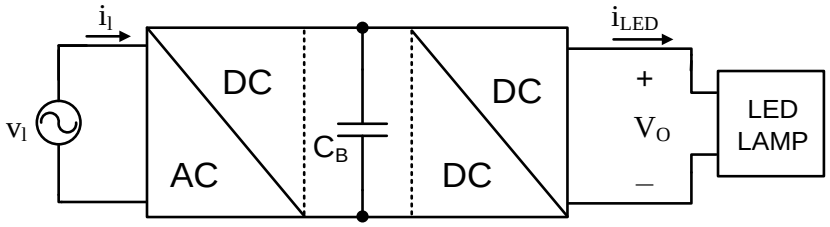


Fig. 1.5.7 – Simplified scheme of the offline double integrated stage driving approach.

The Multiple Stage Approach

Finally, as concerns high power applications the multiple stage configuration approach usually results to be the most suitable solution. This is the case, for instance, of the so called "area lighting" fixtures, namely: street lighting, fluorescent and HID lamps replacements, etc..., in which the power level is generally higher than 60W.

In this lighting sector, indeed, ballast compactness is usually a minor constraint, while good line side performance are strongly recommended as well as high efficiency levels. Moreover, it is worth to note that in such appliances the actual influence of the driving stage on the overall lighting fixture cost is significantly lower, if compared to low and medium power applications, such as bulb replacement or down lighting.

Therefore, the use of an even complex structure (Fig. 1.5.8), capable of guaranteeing high performance both on line and on load side, is usually easily justified. Furthermore, thanks to the use of highly optimized stages, also high efficiency levels can be reached, despite the multiple energy conversion process.

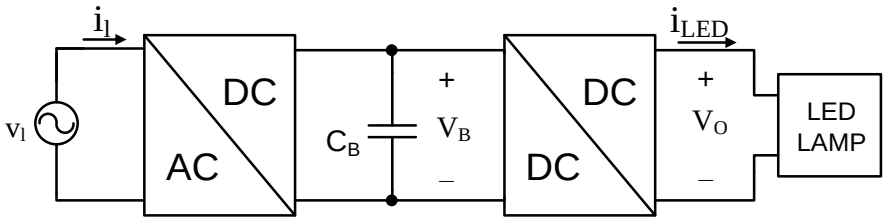


Fig. 1.5.8 – Simplified scheme of the offline multiple stage driving approach.

Since each conversion stage is intended to perform at best a given specific task, such a solution also guarantees the maximum flexibility, significantly simplifying converter design. The line voltage can be initially bucked or boosted, getting DC-link voltage levels lower or higher than the line peak, depending on the selected topologies. Galvanic isolation can be provided by the input stage, by the output stage or even by an additional intermediate DC-DC conversion stage, that is operated in a fixed working point, so as to optimize transformer design and maximize its efficiency.

Some novel solutions, aimed at matching specific solid state lighting requirements while improving the overall lighting fixture performance, will be presented in the following chapters.

Each one of the just described different offline LED driving approaches will be deeply investigated. All the deriving issues will be carefully discussed and addressed, throughout the description of the results of the research activity performed, that actually constitutes the core of this thesis.

Chapter 2

The Single Stage Approach

2.1 Introduction

In this chapter a thorough analysis of a LED lamp ballast solution, based on the use of the single stage approach, is presented. As already remarked, the main challenge of this kind of approach to the solid state driving issue is to be able of guaranteeing proper performance both on line and on load side, through the use of a single power conversion stage. Thanks to its simplicity and low component count, this solution is considered a suitable option mainly in low power applications in which compactness and low cost are considered major goals. As concerns solid state lighting market, the typical area of interest, characterized by such kind of specifications is that of bulb replacement applications. In this regard, LED lamp drivers currently available usually replicate the typical structure of compact fluorescent lamp ballasts, whose volume, however, are typically too large to be widely acceptable.

In order to achieve a substantial driver miniaturization, so as to give the possibility to put the whole ballast circuitry it in the typical E27 standard sockets, passive and, in particular, magnetic component volume minimization is a fundamental concern. Therefore, a significant increase of the operating frequency towards the range of, at least, some

hundreds kHz is required. This calls for the use of converters that, thanks to their easy scalability toward high switching frequency operation, like in the case of resonant topologies, can properly suit this purpose. In particular, the conventional series resonant converter could be considered, as the simplest implementation of the concept, as in [23]. However, in order to be able of guaranteeing soft switching operation, independently from the load level, so as to limit the detrimental effects of high switching frequency on converter efficiency, different kinds of solution, such as those based on the LLC resonant topology, have been investigated in recent years [24]-[28].
In order to retain all the advantages of the LLC structure, while enabling also load regulation at constant switching frequency, through a proper control of the power switches duty cycle, a solution based on the use of the asymmetrical half bridge (AHB) topology ([29]-[37]) has been considered.

As it will be carefully discussed in the following, the considered converter, actually an AHB flyback topology ([38]-[48]), through a proper design, optimization and control techniques, is also capable of managing significant input DC-link voltage ripple levels, while guaranteeing optimized operating conditions for the resonant circuit.

The latter, in particular, is a really interesting feature that gives the possibility to comply with the EN61000-3-2 without implementing any kind of power factor correction technique, simply by means of full wave rectifier cascaded with a small input non electrolytic filter capacitor.
In this regards, it is worth to note that the EN61000-3-2 standard offers, as concerns lighting equipments with a maximum power lower than 25W, the possibility of choosing between two different kinds of requirements.

The first one is to comply with the class D limits (normalized over the nominal power of the application) regarding all odd harmonics up to 39^{th}, as reported in Table 2.1.1.

The other one is to satisfy two different constraints, namely:

1) the 3^{rd} harmonic must be lower than 86% of the fundamental harmonic while the 5^{th} harmonic must be lower than 61% of the fundamental harmonic;
2) the input current waveform must start at an angle lower or equal than 60°, present the last peak at an angle lower or equal than 65° and end at an angle greater or equal than 90°, where the line voltage zero-crossing is assumed to be at 0°.

TABLE 2.1.1 - EN61000-3-2 CLASS D SPECIFICATIONS

HARMONIC ORDER "n"	MAXIMUM PERMISSIBLE HARMONIC CURRENT (mA/W)
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13	0.269
2n+1 where: 7<n<19	3.85/n

So, in this regard, the main concern to be addressed will be the identification of the less demanding requirement, between the two given options, and the set up of a proper design procedure, in order to determine the maximum value of the input filter capacitor that guarantees the compliance with standard for a given load power.

2.1.1 Line Side Harmonic Injection

In solid state lighting fixtures, the load is typically regulated so as to guarantee a constant current level through the LEDs. Consequently, keeping in mind LEDs voltage-current characteristic and assuming steady thermal conditions, also the power absorbed from the line will be constant in such kind of applications.

Therefore, in order to perform the analysis of the input rectification and filtering stage, a model like that shown in Fig. 2.1.1 can be reasonably considered.

As it can be noticed, the input rectification stage has been modeled with a diode and a voltage source, generating the rectified line voltage:

$$\left|v_l(\theta)\right| = V_l \cdot \left|\sin(\theta)\right|, \qquad \theta = \omega_l t \tag{2.1.1}$$

where V_l is the line voltage peak and ω_l is the angular frequency.

On the other hand, as concerns the power conversion stage and the LED load, they have been replaced with a variable current source, whose value varies as a function of the

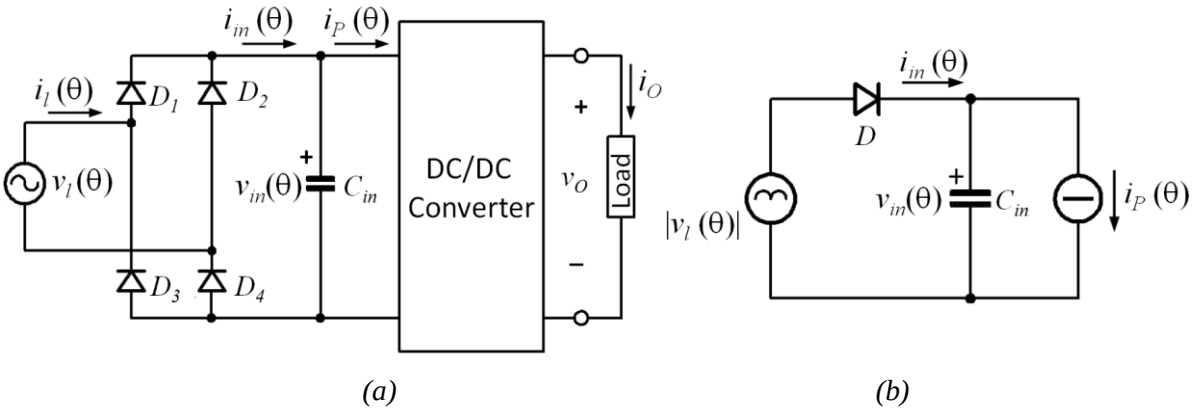


Fig. 2.1.1 – (a) Full wave rectifier feeding a constant power load, (b) equivalent scheme.

voltage across the input filter capacitor ($v_{in}(\theta)$), so as to model an input constant power (P_{DC}) absorption:

$$i_P(\theta) = \frac{P_{DC}}{v_{in}(\theta)} \tag{2.1.2}$$

In order simplify the notation used throughout the analysis, voltage and current expressions will be normalized. To this end the following base quantities has been conveniently chosen:

$$V_N = V_l, \qquad I_N = \frac{P_{DC}}{V_l} \tag{2.1.3}$$

Now, keeping in mind the assumptions made and the quantities defined, the expression of normalized diode current, during the diode bridge conduction interval, can be written as follows:

$$i_{inN}(\theta) = \frac{i_{in}(\theta)}{I_N} = \omega_l C_{in} \frac{V_l^2}{P_{DC}} \cos(\theta) + \frac{1}{\sin(\theta)} = 2k\cos(\theta) + \frac{1}{\sin(\theta)} \tag{2.1.4}$$

where k is an adimensional parameter defined as:

$$k = \omega_l C_{in} \frac{V_l^2}{2P_{DC}} \tag{2.1.5}$$

and C_{in} is the value of the input filter capacitance cascaded to the diode bridge.

If |k|>1, the rectifier bridge turns-off at θ_2, when the diode current (2.1.4) zeroes:

$$\theta_2 = \frac{\pi}{2} + \frac{1}{2}\arcsin\left(\frac{1}{k}\right) \tag{2.1.6}$$

From (2.1.5) and (2.1.6) it can be noticed that, being the parameter *k* always positive, the angle θ_2 will be always greater than $\pi/2$, thus satisfying one of the constraint imposed by the standard.

Within the diode bridge conduction time, the DC-link voltage coincides with the rectified input voltage, so that, at the end of such interval, the normalized voltage across the input filter capacitor will be:

$$v_{inN}(\theta_2) = \frac{v_l(\theta_2)}{V_l} = \sin(\theta_2) \tag{2.1.7}$$

where $v_{in}(\theta)$ is the instantaneous DC-link voltage.

When the rectifier stops conducting, the input filter capacitor is discharged by the constant power load.

The equation describing the DC-link voltage behavior, is:

$$\omega_l C_{in} \frac{dv_{in}(\theta)}{d\theta} + \frac{P_{DC}}{v_{in}(\theta)} = 0 \tag{2.1.8}$$

that can be easily rewritten as:

$$\int_{V_2}^{v_{in}(\theta)} v_{in} dv_{in} = \frac{1}{2}\left(v_{in}^2(\theta) - v_{in}^2(\theta_2)\right) = -\frac{1}{k}\frac{V_l^2}{2}\int_{\theta_2}^{\theta} d\theta = -\frac{1}{k}\frac{V_l^2}{2}(\theta - \theta_2) \tag{2.1.9}$$

so that, once normalized, the solution will be the following:

$$v_{inN}(\theta) = \sqrt{\sin^2(\theta_2) - \frac{1}{k}(\theta - \theta_2)} \tag{2.1.10}$$

When, at θ_1, the DC-link voltage becomes sufficiently lower than the rectified line voltage the rectifier starts conducting:

$$v_{inN}(\pi + \theta_1) = \sin(\theta_1) \tag{2.1.11}$$

So, substituting (2.1.10) in the normalized form of (2.1.11), the following equation can be derived:

$$\sin^2(\theta_2) - \frac{1}{k}(\theta_1 + \pi - \theta_2) = \sin^2(\theta_1) \tag{2.1.12}$$

whose solution can only be found numerically. The result is plotted in Fig. 2.1.2 as a function of parameter *k* previously defined. As it can be noticed, the constraint regarding the starting point of the input current (θ_1 lower that the $\pi/3$) can be satisfied, if the value of the parameter *k* does not exceed the limit k_{limI}=10.35.

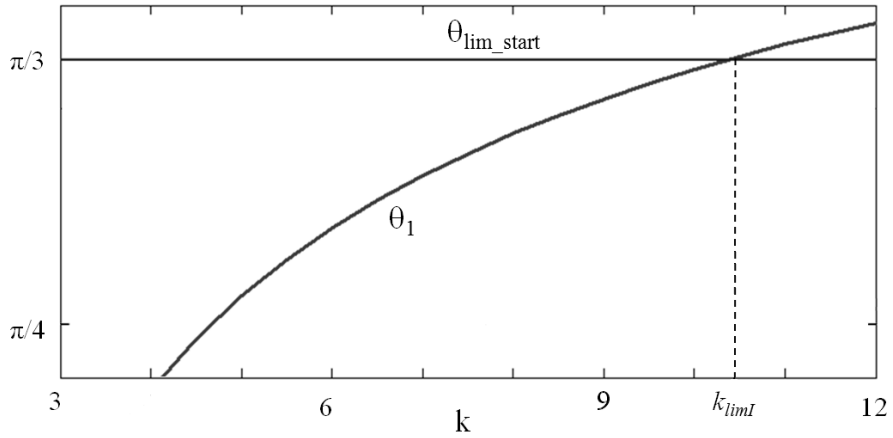


Fig. 2.1.2 – Angle θ_1 as a function of parameter k.

As concerns the line current peak, assuming the line current waveform to resemble a right triangle during full wave rectifier conduction, as evidenced also in Fig. 2.1.3, the current peak angle can be accurately approximated with the current start angle.

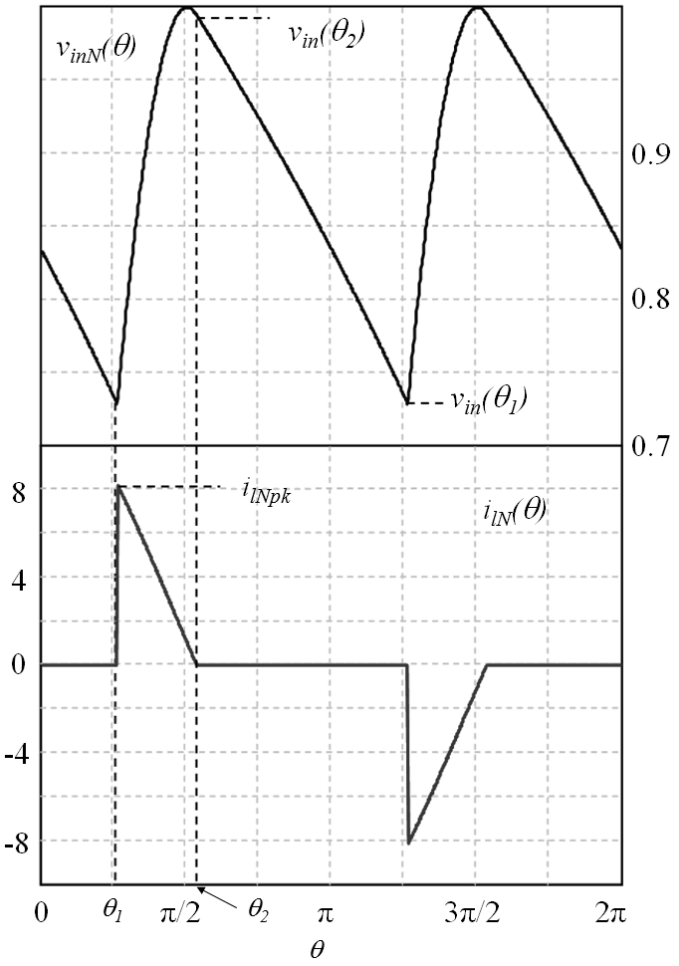


Fig. 2.1.3 – Normalized DC link voltage and line current waveforms within the line period.

As a consequence, once that the constraints limiting the latter are met, also the requirements constraining the former will result to be fulfilled.
Moreover, from the normalized DC-link voltage and input current waveforms, shown in Fig. 2.1.3 within the line period, the normalized DC-link voltage peak-to-peak ripple can be derived:

$$\Delta v_{inN} = \frac{\Delta V_{in}}{V_l} = 1 - \sin(\theta_1) \tag{2.1.13}$$

Once the limitations related to the requirements constraining the input current waveform have been discussed, it is worth focusing the attention on the absorbed current harmonic contents.
Now, being the input current $i_{in}(\theta)$ non sinusoidal, but periodic with period 2π, it can be written in the general normalized form as:

$$i_{inN}(\theta) = \frac{i_{in}(\theta)}{I_N} = I_{inN} + \sum_{j=1}^{\infty} i_{inN_j}(\theta) = \frac{1}{2}a_0 + \sum_{j=1}^{\infty}\left[a_j \cos(j\theta) + b_j \sin(j\theta)\right] \tag{2.1.14}$$

where:

$$a_{jN} = \frac{1}{\pi}\int_0^{2\pi} i_{inN}(\theta)\cdot\cos(j\theta)\, d\theta\,, \qquad j = 1,\ 2,\ 3... \infty \tag{2.1.15}$$

$$b_{jN} = \frac{1}{\pi}\int_0^{2\pi} i_{inN}(\theta)\cdot\sin(j\theta)\, d\theta\,, \qquad j = 1,\ 2,\ 3... \infty \tag{2.1.16}$$

while a_0 will be zero, being the average value of the input current null.
Consequently, the input current harmonics normalized amplitude will be:

$$I_{in\,jN} = \sqrt{a_{jN}^2 + b_{jN}^2} \tag{2.1.17}$$

in particular, the third and fifth harmonic amplitudes, normalized to the fundamental have been derived and reported in Fig. 2.1.4, as a function of parameter *k*.
By comparing such curved with the corresponding limits imposed by the EN61000-3-2 (i.e. $\lambda_3=0.86$ and $\lambda_5=0.61$,) two other constraints: k_{limII} = 5.14 and k_{limIII} =5.33, can be derived for the parameter k. Therefore, in order to guarantee all the requirements to be complied, the most restrictive constraint will have to be considered, yielding:

$$k < k_{\lim} = \min\left\{k_{\lim I}, k_{\lim II}, k_{\lim III}\right\} = k_{\lim II} = 5.14 \tag{2.1.18}$$

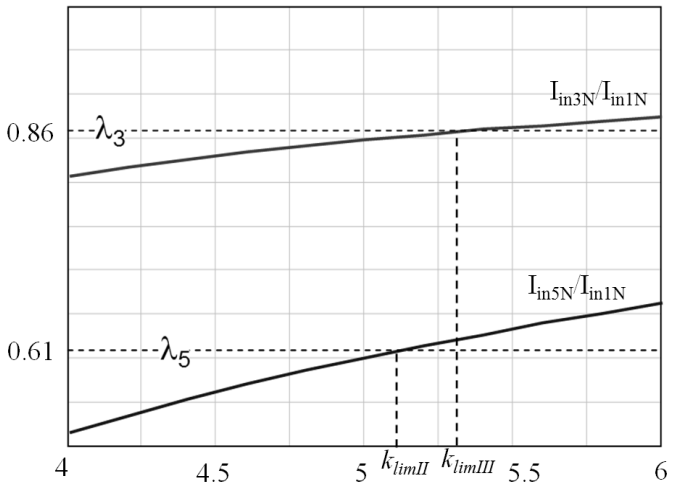


Fig. 2.1.4 – Comparison between the third and fifth harmonics, normalized to the fundamental component, and the EN61000-3-2 limits, as a function of parameter k.

As it can be observed, the strongest restriction to the parameter *k* value derives from the fifth harmonic limitations. Keeping in mind (2.1.5), the requirement expressed in (2.1.18) can be turned into a constraint limiting the maximum admissible value of the input filter capacitance, as a function of converter input power:

$$C_{in} < C_{in\,MAX} = \frac{2k_{\lim III}}{\omega_l V_l^2} \cdot P_{DC} \approx 309 \cdot 10^{-9} \left[\frac{F}{W}\right] \cdot P_{DC} \tag{2.1.19}$$

Keeping in mind the expression (2.1.13) and considering the angle θ_1, corresponding to k_{limIII} in Fig. 2.1.2, the resulting minimum relative peak to peak ripple of the DC-link voltage can be found to be equal to 26.3%.

It is worth to observe that, according to the analysis performed so far, the compliance with the fifth harmonic limitation is sufficient to respect also all the other requirements characterizing the second version of the EN61000-3-2 standard, previously presented.
So, being the compliance with the class D limits for all the odd harmonics up to the thirty-ninth the only alternative, it can be concluded that the one discussed will be actually the less demanding option to comply with the EN61000-3-2 standard, for lighting equipment of power lower than 25W, with the considered input filter stage.

2.2 The AHB-Flyback Converter

In the introduction paragraph, the use of an input stage based on the cascade of a full wave rectifier with an input filter capacitance has been carefully discussed, with the aim of pointing out the consequences deriving from need of guaranteeing the compliance with the EN61000-3-2 standard.

The main concern, from this stand point resulted to be the constraint regarding the input current fifth harmonic amplitude, that actually limits the maximum value of the filter capacitance value. As shown, this consequently turns in a large input voltage ripple that will have to be properly managed from the DC-DC power converter, in order to minimize the at twice the line frequency ripple on the LED current.

Therefore an in-depth study of the DC-DC power conversion stage operation is presented here in the following, with the aim of understanding the behavior of the selected converter, based on the asymmetrical half bridge flyback topology, as shown in

Fig. 2.2.1.

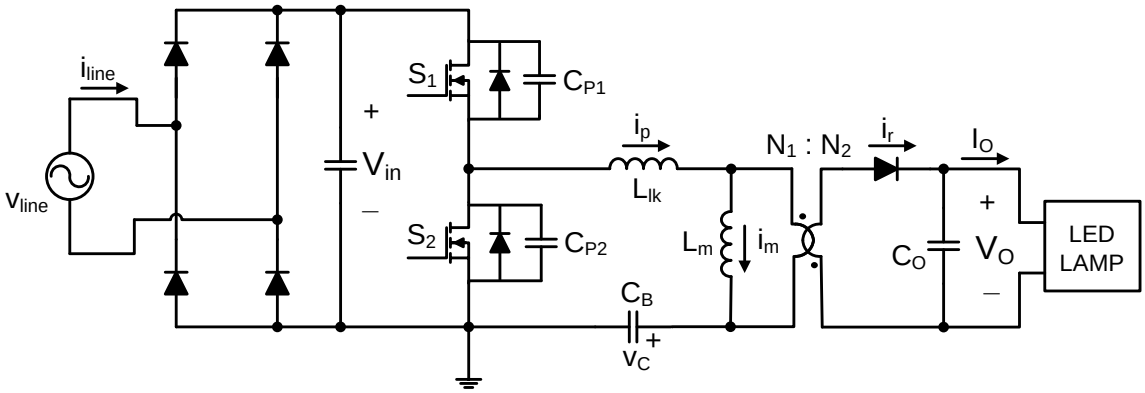


Fig. 2.2.1 - Asymmetrical half bridge flyback converter

For sake of simplicity, some preliminary assumptions can be done. In particular, all components are considered to be ideal, with the exception of the mutual inductor's leakage inductance (L_{lk}) and of the half bridge switches' body diodes and output parasitic capacitances (C_{P1} and C_{P2}). Then the magnetizing inductance (L_m) is assumed to be much larger than the leakage one, so that their ratio ($\lambda = L_{lk} / L_m$) results to be much smaller than unity. Furthermore, the voltage on the input and output filter capacitors is supposed to be

almost constant, within the switching period and, finally, converter steady-state operation is assumed.

The resulting simplified circuit, reported at transformer's primary side, is shown in Fig. 2.2.2, where n_{12} is the transformer turns ratio, defined as:

$$n_{12} = \frac{N_1}{N_2} \tag{2.2.1}$$

being N_1 and N_2 the number of transformer primary and secondary turns, respectively.

Moreover, converter discontinuous conduction mode operation will be considered, that is defined as the operating mode where the output rectifier diode stops conducting before the end of the switching period, thus avoiding any reverse recovery problem.

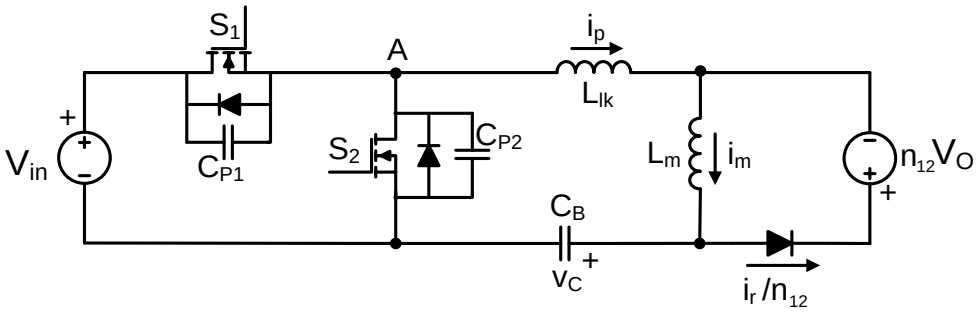


Fig. 2.2.2 - Simplified circuit reported at transformer's primary side

In the general case, when the converter is operated in this mode, with zero voltage turn-on commutations, six different topological phases can be identified throughout the switching period, considering also the switching transients of the half bridge MOSFETs.

Interval I: $t \in [t_0, t_1]$

At time t_0, the switch S_2 is off, supporting the whole input DC-link voltage V_{in} at its terminals. The parasitic diode of S_1 is therefore forward biased and conducts the whole converter primary current i_p until the switch is turned-on with zero voltage.

Therefore, during this first interval, the input voltage is connected in series with the DC blocking capacitor (C_B) and the mutual inductor's leakage and magnetizing inductances (L_{lk} and L_m), while the output rectifier diode is reverse biased. So, no input power will be delivered to the converter output side during this phase, being the whole primary current (i_p) recycling at transformer primary side through the magnetizing inductance. The equivalent circuit is shown in Fig. 2.2.3.

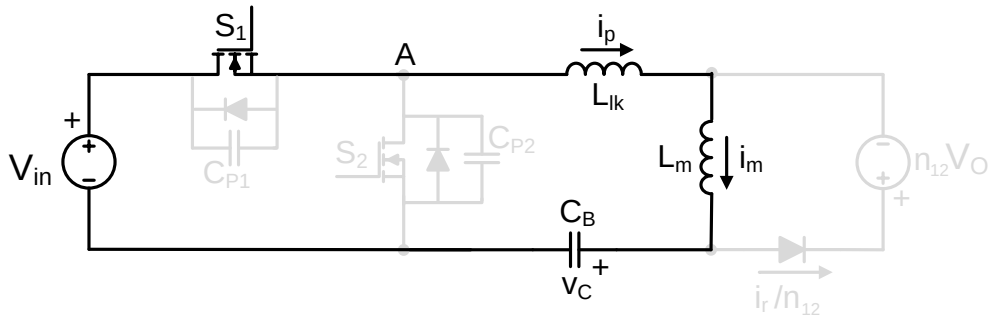


Fig. 2.2.3 - Simplified scheme of the AHB-flyback converter during the first interval.

Applying Kirchhoff's voltage law to the resulting resonant network, a second order homogeneous differential equation is obtained, whose solution, applying Dirichlet's conditions to the state variables $v_C(t)$ and $i_p(t)$, yields:

$$i_p(t) = i_{p0}\cos\left[\omega_{r1}(t-t_0)\right] + \frac{(V_{in}-v_{c0})}{Z_{r1}}\sin\left[\omega_{r1}(t-t_0)\right] \tag{2.2.2}$$

$$v_c(t) = V_{in} - (V_{in}-v_{c0})\cos\left[\omega_{r1}(t-t_0)\right] + Z_{r1}i_{p0}\sin\left[\omega_{r1}(t-t_0)\right] \tag{2.2.3}$$

where i_{p0} and v_{c0} are the state variable values in t_0 and

$$\omega_{r1} = \frac{1}{\sqrt{(L_{lk}+L_m)C_B}}, \qquad Z_{r1} = \sqrt{\frac{L_{lk}+L_m}{C_B}} \tag{2.2.4}$$

are the series resonant network resonance angular frequency and characteristic impedance, respectively.

It is worth to note that, typically, the resonance frequency characterizing this interval will result to be much lower than converter switching frequency, so that primary current waveform will resemble a linear trend, as shown in Fig. 2.2.8.

When, at t_1, the switch S_1 is turned-off, this first interval reaches its end. Note that the converter duty cycle (D) is defined as the time interval during which the converter is directly connected to the DC-link, over the length of the whole switching period (T_{sw}):

$$D = \frac{t_1 - t_0}{T_{sw}} \tag{2.2.5}$$

Interval II: $t \in [t_1, t_2]$

When S_1 is switched-off, the primary current starts charging its output parasitic capacitance while discharging that of the ground switch (C_{P1} and C_{P2} in Fig. 2.2.4, respectively).

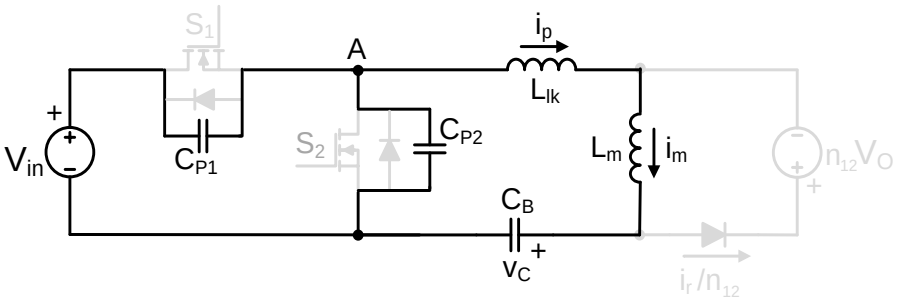


Fig. 2.2.4 - Simplified scheme of the AHB-flyback converter during the second interval.

Now, the equivalent circuit, according to Thévenin theorem, of the network composed by the input voltage generator and the output parasitic capacitances of the half bridge switches can be considered. In particular, assuming parasitic reactances to be equal (C_{P1}=C_{P2}=C_P), the simplified circuit of Fig. 2.2.5 will be actually obtained, where C_{OSS} corresponds to the parallel of C_{P1} and C_{P2} (supposed to be constant):

$$C_{oss} = C_{P1} + C_{P2} = 2C_P \tag{2.2.6}$$

and has an initial voltage value equal to:

$$v_{oss1} = v_{oss}(t_1) = v_A(t_1) = V_{in} \tag{2.2.7}$$

where v_A is the half bridge voltage, as shown in Fig. 2.2.5.

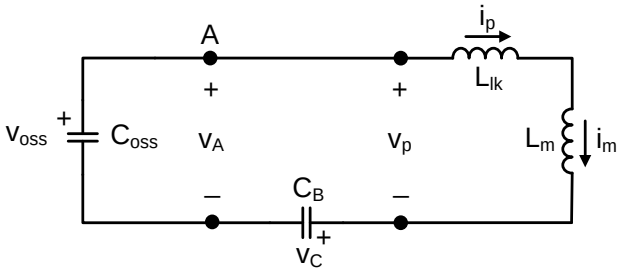


Fig. 2.2.5 - Converter equivalent circuit during the second interval.

Now, applying the Kirchhoff's voltage law to this new resonant network, solving the deriving second order homogeneous differential equation and imposing the Dirichlet's conditions to $v_C(t)$, $v_{oss}(t)$ and $i_p(t)$, keeping in mind (2.2.7), it is possible to write the following expressions:

$$i_p(t) = i_{p1}\cos\left[\omega_{r2}(t - t_1)\right] + \frac{1}{Z_{r2}}(V_{in} - v_{c1})\sin\left[\omega_{r2}(t - t_1)\right] \tag{2.2.8}$$

$$v_c(t) = v_{c1} + \frac{v_{c1} - V_{in}}{(C_B + C_{oss})} C_{oss} \left\{ \cos\left[\omega_{r2}(t - t_1)\right] - 1 \right\} + \frac{i_{p1}}{C_B \omega_{r2}} \sin\left[\omega_{r2}(t - t_1)\right] \quad (2.2.9)$$

$$v_{OSS}(t) = \frac{v_{c1} - V_{in}}{(C_B + C_{oss})} C_B \left\{ \cos\left[\omega_{r2}(t - t_1)\right] - 1 \right\} + \frac{i_{p1}}{C_B \omega_{r2}} \sin\left[\omega_{r2}(t - t_1)\right] \quad (2.2.10)$$

where the resonance angular frequency and impedance are:

$$\omega_{r2} = \sqrt{\frac{C_B + C_{oss}}{(L_{lk} + L_m) C_{oss} C_B}}, \quad Z_{r2} = \sqrt{\frac{(L_{lk} + L_m)(C_B + C_{oss})}{C_{oss} C_B}} \quad (2.2.11)$$

while i_{p1} and v_{c1} are the state variables values at t_1.

It is worth to note that, being in general $C_{oss} << C_B$, the series of the parasitic capacitances and the DC blocking capacitor will have a much higher reactance compared to that of the blocking capacitor only. Consequently, the resonance frequency characterizing this second interval, will be much higher than that of the previous one, as it can be clearly noticed observing the primary current waveform reported in Fig. 2.2.8.

When, at the instant t_2, the half bridge voltage reaches zero:

$$v_{oss}(t_2) = v_A(t_2) = 0 \quad (2.2.12)$$

the body diode of S_2 becomes forward biased and this second phase comes to an end.

Interval III: $t \in [t_2, t_3]$

Once the body diode of S_2 has started conducting, it is possible to turn-on the switch S_2 with zero voltage. If the magnitude of the magnetizing inductance voltage is lower than that of the output voltage reflected to the primary side:

$$\frac{v_c(t)}{1 + \lambda} < n_{12} V_O \quad (2.2.13)$$

the output rectifier diode remains reverse biased, so that the primary current keeps recycling through the magnetizing inductance at primary side, being the load still disconnected from transformer secondary side. The equivalent circuit is shown in Fig. 2.2.6.

It can be noticed, that the elements involved in this new resonant interval are the same of the first one, so that also the resonance frequency and the characteristic impedance will be

the same ($\omega_{r3} = \omega_{r1}$ and $Z_{r3} = Z_{r1}$) and, also in this case, the primary current waveform will resemble a linear trend.

Solving the differential equation, corresponding to the state equations governing this phase, and imposing Dirichlet's conditions, we find:

$$i_p(t) = i_{p2}\cos\left[\omega_{r3}(t-t_2)\right] - \frac{v_{c2}}{Z_{r3}}\sin\left[\omega_{r3}(t-t_2)\right] \tag{2.2.14}$$

$$v_c(t) = v_{c2}\cos\left[\omega_{r3}(t-t_2)\right] + Z_{r3}i_{p2}\sin\left[\omega_{r3}(t-t_2)\right] \tag{2.2.15}$$

where i_{p2} and v_{c2} are the state variable values in t_2.

When, at t_3, due to the increasing voltage on the DC blocking capacitor, the inequality (2.2.13) becomes no longer valid, the output rectifier diode is forward biased and the just described interval reaches its end.

It is worth to note that, if at t_2 the condition (2.2.13) is not verified, the output diode immediately starts conducting and, consequently, this phase will be skipped.

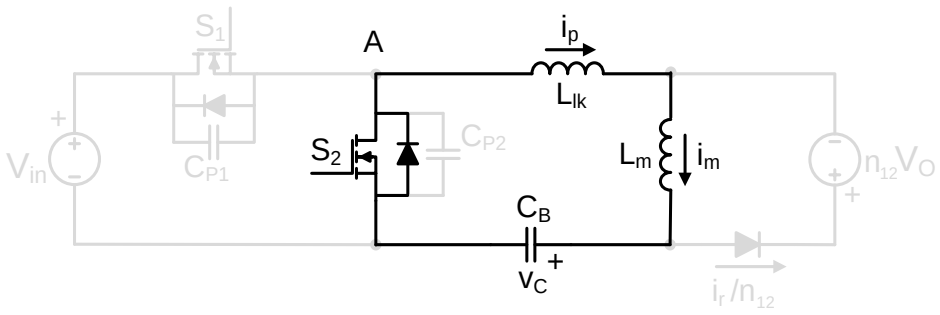


Fig. 2.2.6 - Simplified scheme of the AHB-flyback converter during the third interval.

Interval IV: $t \in [t_3, t_4]$

During the output diode conduction interval, the input line energy is delivered to the load and the voltage across the magnetizing inductance is clamped at the output voltage reflected to the transformer's primary side, as it is shown in Fig. 2.2.7. Therefore, while the DC blocking capacitor resonates with the leakage inductance, the magnetizing current will decrease linearly according to the law:

$$i_m(t) = i_{p3} - \frac{n_{12}V_O}{L_m}(t-t_3) \tag{2.2.16}$$

The equations, describing the state variable evolution during this interval, are here reported in the following:

$$i_p(t) = i_{p3}\cos\left[\omega_{r4}\left(t-t_3\right)\right] + \frac{1}{Z_{r4}}\left(n_{12}V_O - v_{C3}\right)\sin\left[\omega_{r4}\left(t-t_3\right)\right] \tag{2.2.17}$$

$$v_c(t) = n_{12}V_O - \left(n_{12}V_O - v_{C3}\right)\cos\left[\omega_{r4}\left(t-t_3\right)\right] + Z_{r4}i_{p3}\sin\left[\omega_{r4}\left(t-t_3\right)\right] \tag{2.2.18}$$

where: $\omega_{r4} = \frac{1}{\sqrt{L_{lk}C_B}}$, $Z_{r4} = \sqrt{\frac{L_{lk}}{C_B}}$, $i_{p3} = i_p(t_3)$, $v_{C3} = v_C(t_3)$.

Keeping in mind the preliminary hypothesis that assumes the leakage inductance to be much smaller than the magnetizing inductance, this interval will be characterized by a significantly higher resonance frequency compared to that of the first and third intervals, as the primary current waveform, reported in Fig. 2.2.8, clearly shows. The difference between the primary and the magnetizing current, scaled by the transformer turns ratio, ($i_r(t)$) is delivered to the output filter and to the load through the secondary side diode.

If the primary resonant current matches the magnetizing one before S_2 is switched-off, the output rectifier diode turns-off with zero current ($i_r(t_4)=0$), causing the end of the present phase and the beginning of the fifth interval.
This condition, that characterizes converter operation in discontinuous conduction mode, can be expressed as follows:

$$i_{p4} = i_p(t_4) = i_{p3} - \frac{n_{12}V_O}{L_m}\left(t_4 - t_3\right) \tag{2.2.19}$$

where $t_4 < t_0 + T_{sw}$.

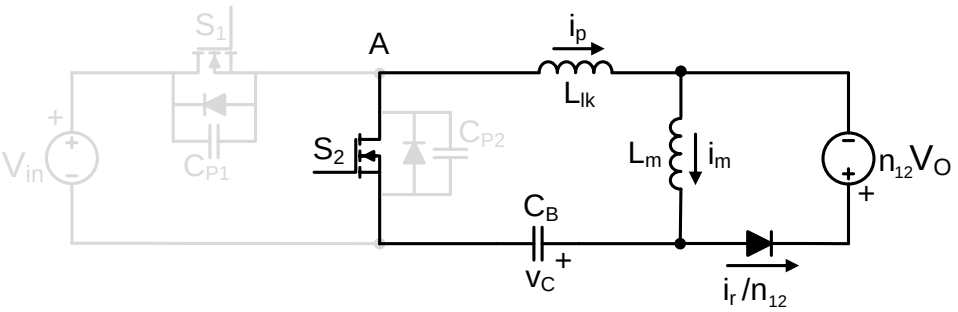


Fig. 2.2.7- Simplified scheme of the AHB-flyback converter during the fourth interval.

Interval V: $t \in [t_4, t_5]$

Once the output rectifier diode is turned-off, the load is disconnected from transformer secondary side and the primary current equals the magnetizing current recycling at primary side. The topological state characterizing this phase is identical to that of the previously considered third interval, shown in Fig. 2.2.6, with the exception of the initial values of the state variables: i_{p4} and v_{C4}.

It is thus possible to write:

$$i_p(t) = i_{p4}\cos\left[\omega_{r5}(t-t_4)\right] - \frac{v_{C4}}{Z_{r5}}\sin\left[\omega_{r5}(t-t_4)\right] \tag{2.2.20}$$

$$v_c(t) = v_{C4}\cos\left[\omega_{r5}(t-t_4)\right] + Z_{r5}i_{p4}\sin\left[\omega_{r5}(t-t_4)\right] \tag{2.2.21}$$

where ω_{r5} and Z_{r5} will be the same previously reported in (2.2.4) so that the primary current waveform will resemble, once again, a linear trend.

When, at t_5, S_2 is switched-off also this fifth interval comes to an end.
It is worth to note that he duration of this phase can vary depending on converter design. In particular, if (2.2.19) is never verified before the ground switch is switched-off, the just described interval will not occur and the topological sequence will directly skip to the sixth stage described here in the following.

Interval VI: $t \in [t_5, t_6]$

Once S_2 has been turned-off, the primary current starts charging and discharging S_2 and S_1 output parasitic capacitances, respectively. This topological stage is identical to that of the second interval, reported in Fig. 2.2.4, and Fig. 2.2.5. The only difference relies on the initial values of the state variables $i_{p5}=i_p(t_5)$, $v_{c5}=v_c(t_5)$ and $v_{OSS5}= v_{OSS}(t_5)=0$. The corresponding state variables expressions are:

$$i_p(t) = i_{p5}\cos\left[\omega_{r6}(t-t_5)\right] - \frac{1}{Z_{r6}}v_{c5}\sin\left[\omega_{r6}(t-t_5)\right] \tag{2.2.22}$$

$$v_c(t) = v_{c5} + \frac{v_{c5}C_{oss}}{(C_B + C_{oss})}\left\{\cos\left[\omega_{r6}(t-t_5)\right] - 1\right\} + \frac{i_{p5}}{C_B\omega_{r6}}\sin\left[\omega_{r6}(t-t_5)\right] \tag{2.2.23}$$

$$v_{OSS}(t) = V_{in} + \frac{v_{c5}C_B}{(C_B + C_{oss})}\left\{\cos\left[\omega_{r6}(t-t_5)\right] - 1\right\} + \frac{i_{p5}}{C_B\omega_{r6}}\sin\left[\omega_{r6}(t-t_5)\right] \tag{2.2.24}$$

where the expressions of ω_{r6} and Z_{r6} will be exactly the same of ω_{r2} and Z_{r2} reported in (2.2.11).

At the instant t_6, when the half bridge voltage reaches the DC-link voltage level (V_{in}):

$$v_{oss}(t_6) = v_A(t_6) = V_{in} \tag{2.2.25}$$

and the body diode of the switch S_1 starts conducting, also this sixth interval comes to an end and, consequently, another switching interval begins.

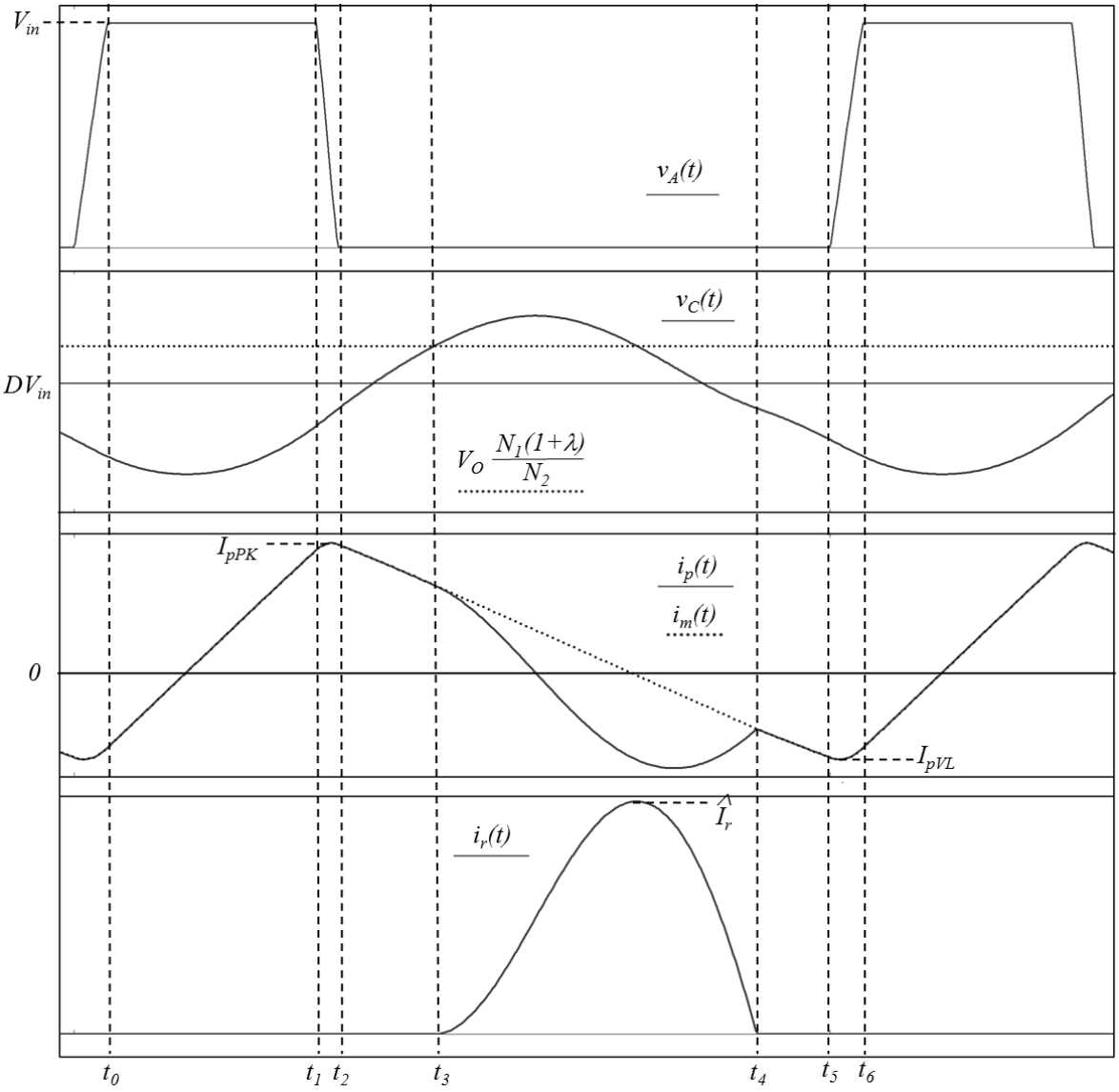


Fig. 2.2.8 - Main waveforms describing the behavior of the AHB-flyback converter within the switching period.

2.3 The Soft Switching Issue

In the analysis of converter operation principles, presented in the previous paragraph, the half bridge switches have been supposed to turn-on at zero voltage. This means that the process of charge and discharge of MOSFETs' parasitic output capacitances has been assumed to be completed within the dead time elapsing between the conduction intervals of the half bridge switches.

It is worth to note that this is a fundamental issue in order to allow high switching frequency operation. To have an idea of the significance of the problem, the effects of the half bridge MOSFETs hard switching on converter efficiency can be estimated.

To this end, let's consider, for example, the half bridge switching transient that occurs when the DC-link connected switch is turned-off and the ground switch is turned-on. If zero voltage switching is assumed, the sequence of the topological stages characterizing such switching interval, will be that represented in Fig. 2.3.1 (a)-(d).

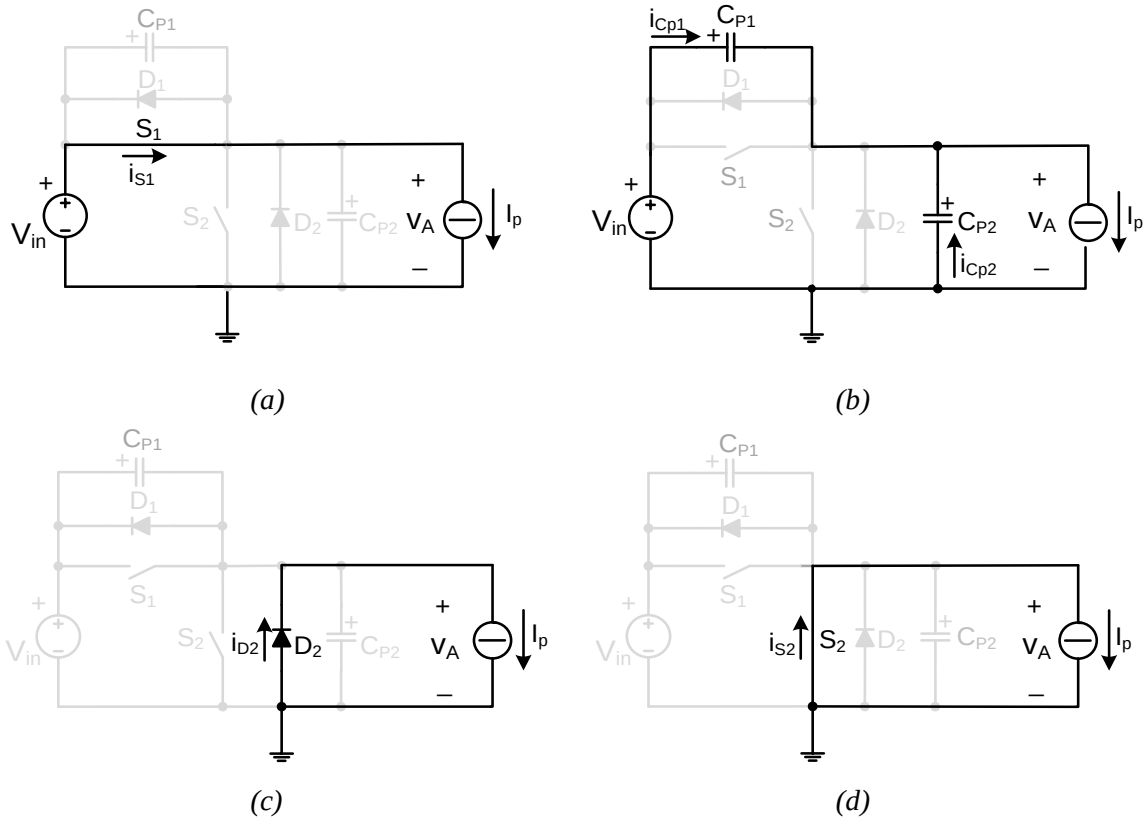


Fig. 2.3.1 - Topological stages characterizing the zero voltage turn-on switching transient of the ground connected switch.

As it can be noticed, the primary current has been assumed to be constant within the whole switching transient and each MOSFET has been modeled by the parallel of its body diode and parasitic capacitance with an ideal switch.

In the initial condition, the DC connected switch (S_1) is conducting, so that its parasitic capacitance (C_{P1}) results to be short-circuited and the whole input voltage is applied at the terminals of the other switch.

When S_1 is turned-off, the primary current starts flowing through the output capacitances of the switches, discharging C_{P2} and charging C_{P1}, while the half bridge voltage gradually decreases, as shown in Fig. 2.3.2.

Once the charge/discharge process is completed, the drain source voltage of the ground switch (S_2) zeroes and the corresponding body diode starts conducting the whole primary current.

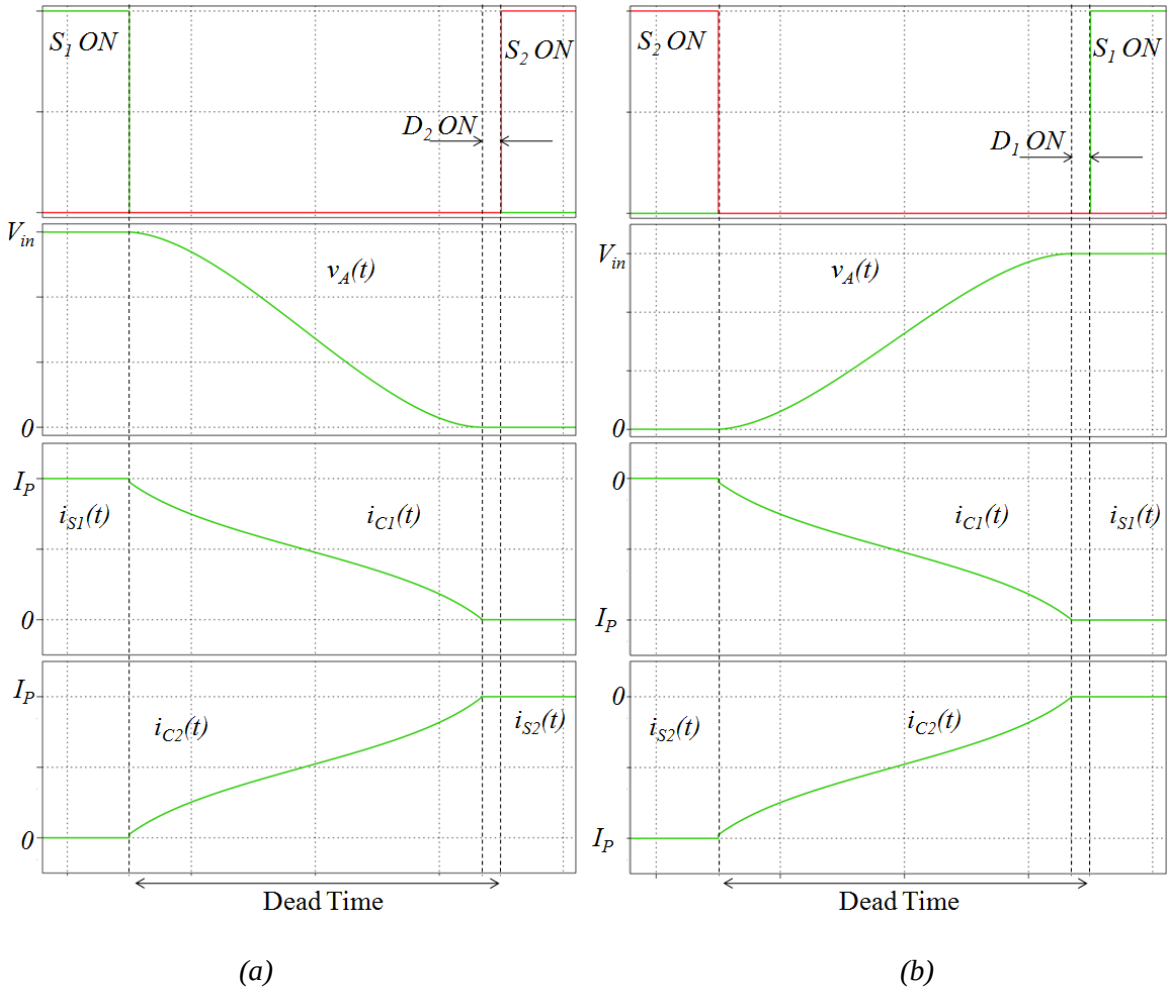


Fig. 2.3.2 - Half bridge current and voltage waveforms in zero voltage switching conditions: (a) S_2 turn-on commutation, (b) S_1 turn-on commutation.

In such situation the voltage levels across the half bridge switches are clamped, so that S_2 can be turned-on at zero voltage in a non dissipative way.

Similarly, during the other switching transition interval ($I_P<0$), the DC-link connected switch output parasitic capacitance will be gradually discharged, during the dead time, until the zero voltage level is reached and the MOSFET is turned-on, as evidenced also in Fig. 2.3.2.

It is worth to note that, in this conditions, the net amount of power supplied by the input line, to complete charge/discharge processes of the switches parasitic capacitances within each converter switching period, is ideally null.

The zero voltage turn-on guarantees, therefore, the half bridge commutations to be non dissipative, being the switching energy actually simply moved from one output parasitic capacitance to the other.

However, if the dead time is not sufficient to guarantee the complete output capacitances charge and discharge process, the drain-source voltage of the turning-on switch will be abruptly forced to zero, as shown in Fig. 2.3.3.

The residual energy (ΔE), still stored in the output parasitic capacitances, will be therefore dissipated in the channel resistance of the MOSFET that has just been turned-on.

As a consequence, for each switching cycle, the total amount of energy lost in the half bridge switches will be equal to:

$$E_{sw} = 2 \cdot \Delta E = 2 \cdot \left(\int_0^{V_{ON}} C_P(v) \cdot v \, dv + \int_{V_{in}-V_{ON}}^{V_{in}} C_P(v) \cdot v \, dv \right) \tag{2.3.1}$$

where $C_P(v)$ expresses the MOSFET parasitic capacitance value, as a function of its drain-source voltage level, while V_{ON} is the residual voltage at MOSFET terminals, in correspondence of the turn-on instant.

To get an estimation of the total amount of converter losses, due to the complete hard switching (i.e. $V_{ON}=V_{in}$ in (2.3.1)) of the half bridge MOSFETs, a model based on the following non linear function of the drain-source voltage can be considered for each switch output capacitance:

$$C_P(v) = C_{Px} \sqrt{\frac{V_x}{v}} \tag{2.3.2}$$

where C_{Px} is the MOSFET's output capacitance, measured at the voltage V_x provided by the device datasheet.

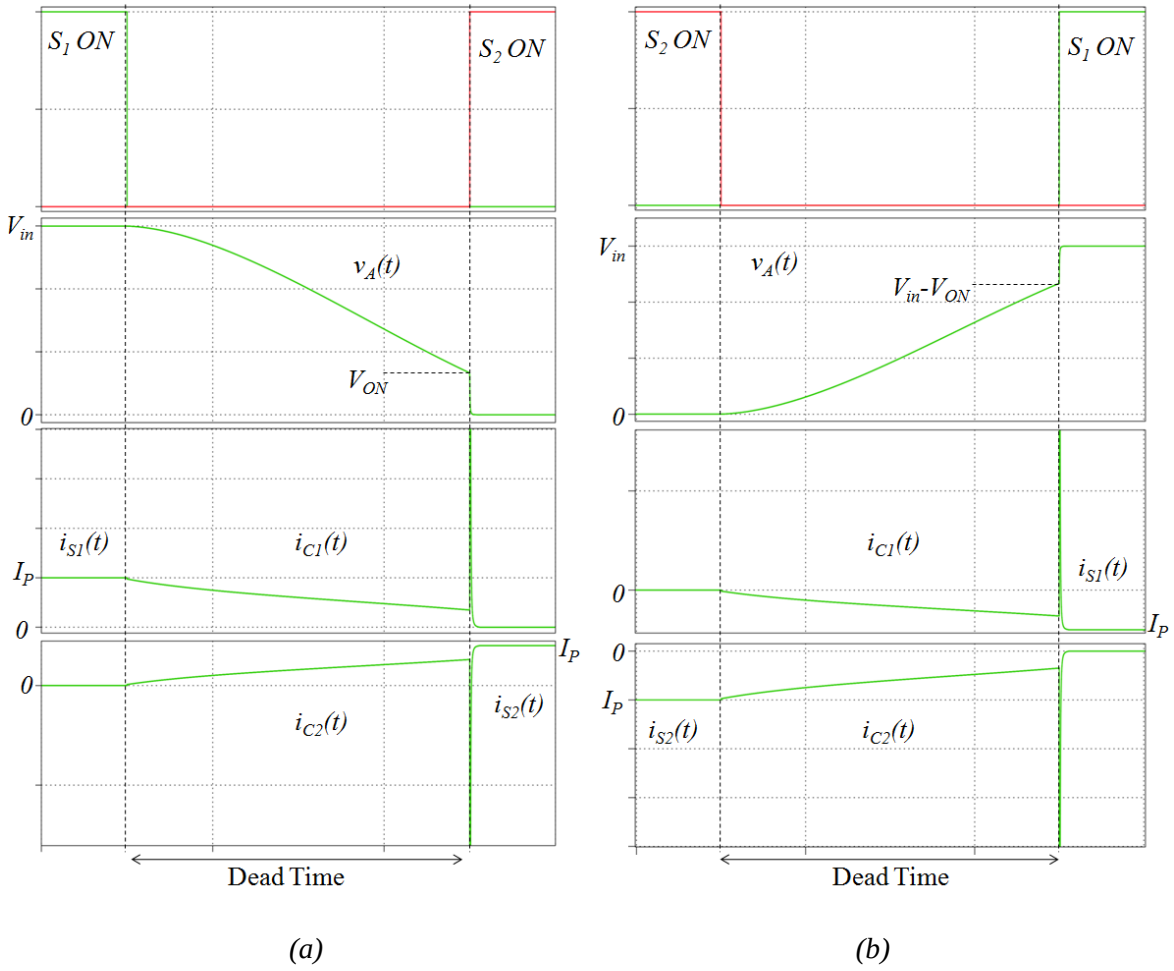


Fig. 2.3.3 - Half bridge current and voltage waveforms in partly hard switching conditions: (a) S_2 turn-on commutation, (b) S_1 turn-on commutation.

Note that this is the model actually used to derive the waveforms of Fig. 2.3.2 and of Fig. 2.3.3, by simulating the half bridge switches behavior in the PLECS® software platform, where each parasitic capacitance has been implemented according to the scheme of Fig. 2.3.4.

As it can be noticed, in order to implement the variable capacitor model, besides the expression of the capacitance as a function of the voltage at its terminal, namely (2.3.2), the derivative of the capacitance with respect to the time is also required, whose expression has been derived as:

$$\frac{dC_P(v)}{dt} = \frac{dC_P(v)}{dv}\cdot\frac{dv}{dt} = -\frac{C_{Px}}{2v}\sqrt{\frac{V_x}{v}}\cdot\frac{dv}{dt} = -\frac{C_P(v)}{2v}\cdot\frac{dv}{dt} = -\frac{1}{2v}\cdot i_{C_P}(t) \qquad (2.3.3)$$

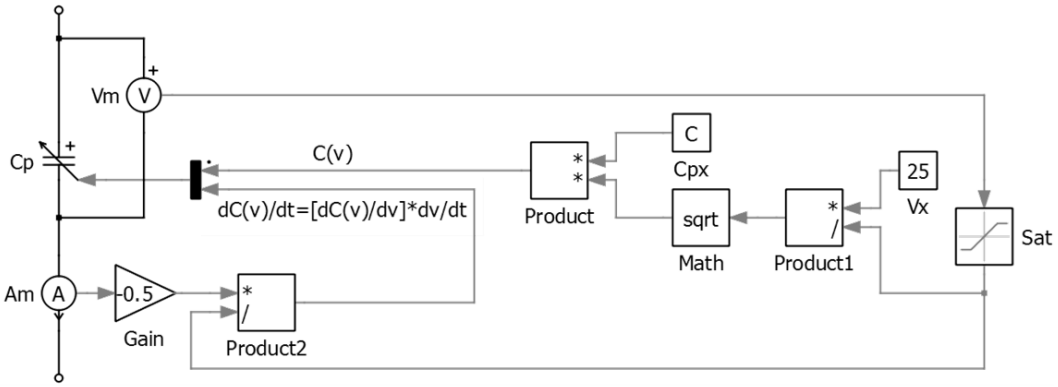


Fig. 2.3.4 - Model of the variable output parasitic capacitance in PLECS®.

Now, considering for the typical bulb replacement application, a representative value of the parameter C_{Px} of about 50pF at 25V and taking into account that, as concerns the European case, the line voltage ($230V_{RMS}$ ± *20%*) peak is about 390V, the estimated converter power loss as a function of the switching frequency will be:

$$P_{sw} = E_{sw} \cdot f_{sw} = 4 \cdot \int_0^{V_{in}} C_P(v) \cdot v \, dv = \frac{8}{3} \cdot C_{Px} \sqrt{\frac{V_x}{V_{in}}} \cdot {V_{in}}^2 \cdot f_{sw} = 5.1 \cdot 10^{-6}[J] \cdot f_{sw} \qquad (2.3.4)$$

So, being the converter, for compactness requirements, supposed to operate in the frequency range of the several hundreds of kHz, it is possible to conclude that usually about 20% of the power supplied to the LED lamp (approximately 10W for the typical target application) will be dissipated because of the only switching losses.

This is clearly unacceptable, if an overall converter efficiency higher than 80% is required, and therefore the achievement of zero voltage commutations is considered a mandatory requirement for the topology under study.

Since, in the AHB-flyback topology, the responsible for MOSFETs output capacitances charge and discharge is converter primary current, a minimum commutated level of this current will be necessary in order to guarantee soft switching operation.

To find out an analytical expression of such threshold value, the primary and magnetizing current waveform in discontinuous conduction mode (namely the considered converter operation mode), reported in Fig. 2.2.8, should be considered, making, for sake of simplicity, some preliminary assumptions.

First of all, as already specified, the primary current is supposed to be almost constant during the whole switching transitions. Furthermore, converter magnetizing current waveform is assumed to be piecewise linear within the entire switching period. (i.e.

$f_{sw} >> 1/\left(2\pi\sqrt{(L_{lk}+L_m)C_B}\right)$ and, finally, the contributions of the transient intervals to the peak to peak primary ripple amplitude is neglected, so that the magnetizing current peak to peak ripple can be reasonably approximated as:

$$\Delta i_m \simeq \frac{V_O n_{12}(1-D)}{f_{sw} L_m} \tag{2.3.5}$$

Now, being at steady state the average current through the DC blocking capacitor (corresponding to the primary current) equal to zero, the average magnetizing current will be positive and equal to:

$$\bar{i}_m = \frac{I_O}{n_{12}} \tag{2.3.6}$$

where I_O is the average load current and n_{12} is the primary to secondary transformer turns ratio.

So, being in DCM operation the primary current's peak and valley values, respectively equal to the magnetizing current minimum and maximum values:

$$I_{pPK} = I_{m_{MAX}} \simeq \bar{i}_m + \frac{\Delta i_m}{2} = \frac{I_O}{n_{12}} + \frac{V_O n_{12}(1-D)T_{sw}}{2L_m} \tag{2.3.7}$$

$$I_{pVL} = I_{m_{MIN}} \simeq \bar{i}_m - \frac{\Delta i_m}{2} = \frac{I_O}{n_{12}} - \frac{V_O n_{12}(1-D)T_{sw}}{2L_m} \tag{2.3.8}$$

the relationship between their modules will be:

$$\left|I_{pVL}\right| < \left|I_{pPK}\right| = \left|I_{pVL}\right| + 2\bar{i}_m = \left|I_{pVL}\right| + 2\frac{I_O}{n_{12}} \tag{2.3.9}$$

denoting that the critical design parameter, as concerns the need to guarantee zero voltage switching, corresponds to primary current valley value.

Now, according to the parasitic capacitances model proposed in (2.3.2), the total amount of charge that has to be drained to complete the charge and discharge process, can be computed as:

$$Q = 2\cdot\int_0^{V_{in}} C_p(v)dv = 4C_p(V_{in})\cdot V_{in} \ , \tag{2.3.10}$$

so that, keeping in mind the preliminary assumptions of constant commutated current, the following charge balance can be written:

$$Q = 4C_p(V_{in}) \cdot V_{in} = \int_{\Delta t_d} ip(t)\, dt = I_{p\min} \cdot \Delta t_d \ . \tag{2.3.11}$$

where Δt_d is the duration of the dead time elapsing between the half bridge switches conduction intervals.

Therefore, imposing (2.3.11) to be verified, the desired analytical expression of the primary commutated current threshold level (I_{pVLmin}), that is required to guarantee soft switching operation, can be found:

$$I_{pVL\min} = \frac{4C_{Px}\sqrt{V_x \cdot V_{in}}}{\Delta t_d} \tag{2.3.12}$$

where C_{Px} is the value of each MOSFET's output capacitance, measured in correspondence of the voltage V_x, as formerly defined.

2.4 Main Converter Design Issues

On the basis of the analysis performed so far, keeping in mind the restrictions deriving from the need of complying with the EN61000-3-2 standard and of guaranteeing soft switching operation, discussed in the previous paragraphs, it is now worth focusing on the investigation of the main converter design issues, with the aim of developing a suitable design procedure.

As formerly pointed out, analyzing the operating principles of the AHB-flyback converter in discontinuous conduction mode, in this topology the transfer of the line input energy to the load is limited to the only conduction time of the output rectifier diode.

A proper converter design technique should be, therefore, aimed at maximizing the corresponding interval, in order to minimize the rectified current peak ($\hat{I}_r$ in Fig. 2.2.8). On the other hand, to avoid any recovery issue, a zero current turn-off of the output diode is desirable. As a result, the best trade-off seems, consequently, to be a design approach meant to achieve borderline operation between continuous and discontinuous conduction mode. This means that the third and the fifth interval, previously described in the converter operation analysis, should be minimized and possibly reduced to zero.

Now, neglecting DC blocking capacitor voltage ripple (i.e. the instantaneous voltage is approximated with its average value: $v_c(t)=DV_{in}$) and assuming operation at the boundary between continuous and discontinuous conduction mode to be guaranteed, the flux balance across magnetizing inductance in steady state conditions can be written as:

$$\frac{1}{(1+\lambda)} \cdot V_{in}(1-D) \cdot DT_{sw} = n_{12} V_O \cdot (1-D) T_{sw} \tag{2.4.1}$$

where the average output voltage (V_O), on the basis of the specification reported in Table 2.4.1, can be expressed as:

$$V_O = V_\gamma + R_\gamma I_{LED} \ . \tag{2.4.2}$$

From (2.4.1) the following expression of the output to input voltage conversion ratio can be derived:

$$M = \frac{V_O}{V_{in}} = \frac{D}{n_{12}(1+\lambda)} \simeq \frac{D}{n_{12}} \tag{2.4.3}$$

where the last equality exploits the reasonable assumption (according to which the whole converter analysis has been done) of dealing with a transformer characterized by leakage to magnetizing inductance ratio (λ) much smaller than unity.

It is worth to note that, in order to optimize the input energy transfer to the load, a further improvement could be obtained by minimizing converter duty cycle.
As long as borderline operation is considered, this will indeed consequently result in maximizing the length of the output diode conduction interval over the switching period, with beneficial effects concerning the output diode current stresses and the secondary side current RMS value.
On the other hand, from (2.4.3) it can be noticed that for a given voltage conversion ratio, the lower is the duty cycle the lower will have to be the primary to secondary side transformer turns ratio, therefore resulting in a higher magnetizing current average value, as shown in (2.3.6).
This will obviously call for a higher magnetizing current peak to peak ripple, in order to guarantee the threshold primary current valley value, required to guarantee the zero voltage switching, as it can easily be inferred from (2.3.8) and (2.3.12), thus increasing the amount of recycling current and affecting converter efficiency.

TABLE 2.4.1 - TARGET APPLICATION SPECIFICATIONS

MAIN CONVERTER PARAMETERS		
NAME	SYMBOL	VALUE
Line input nominal RMS voltage	V_{lRMS_N}	230V
Line input RMS voltage variation	ε_{Vl}	± 20% V_{lRMS_N}
Line frequency	f_l	50Hz
Average LED load current	I_{LED}	0.45A
Maximum LED current ripple	ΔI_{LED}	±5%
LED lamp threshold voltage	V_γ	14V
LED lamp series resistance	R_γ	5Ω
Converter switching frequency	f_{SW}	> 100kHz
Estimated MOS parasitic capacitance	C_P	50pF@V_x=25V
Overall Converter efficiency	η	> 80%

Furthermore, it can be observed that the beneficial effects, deriving from the decrease of the output current (i_r) RMS value, will be confined at secondary side, being compensated, at transformer primary side, by the decreasing of the turns ratio n_{12}.
For all this reasons, given the specifications of the target application, reported in Table 2.4.1, the issue considered at first (that calls for the minimization of converter duty ratio) will be regarded as a minor aspect, when selecting a proper maximum value for the converter duty ratio.

Once that the maximum converter duty ratio has been determined, the value of the transformer turns ratio can be easily computed from (2.4.3) in correspondence of the minimum input voltage:

$$n_{12} = \frac{D_{MAX} \cdot V_{inMIN}}{V_O \cdot (1+\lambda)} \simeq \frac{D_{MAX} \cdot V_{inMIN}}{V_O} \tag{2.4.4}$$

It is worth to note that, as formerly discussed, according to the (2.1.19), in order to comply with the EN61000-3-2 standard, the input filter capacitance has to be lower than:

$$C_{in\,MAX} = 309 \cdot 10^{-9} \left[\frac{s}{V^2}\right] \cdot P_{DC} = 309 \cdot 10^{-9} \left[\frac{s}{V^2}\right] \cdot \frac{\left(V_\gamma + R_\gamma I_{LED}\right) I_{LED}}{\eta} \tag{2.4.5}$$

(where η is the estimated converter efficiency), resulting in a DC-link voltage ripple at twice the line frequency, of about the 30% of the line peak.
Moreover, keeping in mind that a variation of ±20% of the line RMS nominal voltage is tolerated, an overall peak to peak input voltage ripple:

$$\Delta V_{in} = V_{in\,MAX} - V_{in\,MIN} \simeq (1.2 - 0.56) \cdot \sqrt{2} \cdot V_{lRMS\_N} = 64\% \cdot \sqrt{2} \cdot V_{lRMS\_N} \tag{2.4.6}$$

will actually have to be managed, by properly regulating converter duty-cycle.

Now, reached this point, the next step in the proposed design procedure concerns the selection of converter switching frequency. In this regards, it should be taken into account that in the typical light bulb replacement application, the ballast should be suitably compact so as to give the possibility to locate the whole driving circuitry in the E27 standard sockets.
Therefore, in order to achieve the desired converter volume minimization, the switching frequency should be sufficiently high, at least in the range of hundreds of kHz.

However, on the other hand, in order to improve converter efficiency, the recycling current should be optimized, calling for proper trade-off between the minimum charge/discharge current level required (I_{pVLmin}) and dead time duration (Δt_d), as clearly shown in (2.3.12). So, in order to prevent the dead time to become a significant percentage of the switching period (e.g. $2\Delta t_d < 5\%T_{sw}$), while guaranteeing the achievement of zero voltage commutations, the switching frequency should be kept suitably low.
As a result, a switching frequency of few hundreds of kHz can be considered a proper compromise between these contrasting requirements, calling for compactness on one hand and recycling current optimization on the other.

Once that converter switching frequency has been selected, magnetizing inductance value can be derived so as to get the minimum commutated current required to guarantee zero voltage commutations.
As formerly explained in paragraph 2.3 the critical design parameter from this standpoint is the valley value of the primary current.
Now, since, the magnetizing current average value is fixed (load specifications are known and transformer's turns ratio has already been designed), according to (2.3.8), the constraint on the primary current valley value will clearly turn in a minimum magnetizing current ripple requirement, thus constraining the magnetizing inductance value.
Therefore, equating (2.3.12) to (2.3.8), the expression of the maximum acceptable magnetizing inductance can be written as:

$$L_{mMAX} = \frac{V_O n_{12}\left(1-D\right)}{2 f_{sw}\left(\bar{i}_m + I_{pVL\min}\right)} = \frac{V_O n_{12}\left(1-D\right)}{2 f_{sw}\left(\frac{I_O}{n_{12}} + \frac{4C_{Px}\sqrt{V_x \cdot V_{in}}}{\Delta t_d}\right)} \tag{2.4.7}$$

whose value, should be computed in correspondence of the worst case condition (i.e., according to the parameters considered in Table 2.4.1 and Table 2.4.2, for the minimum input voltage and maximum duty cycle).

Now, on the basis of the parameters just designed, a transformer prototype, can thus be implemented, so that its leakage inductance can be measured, to be used in the computation of the DC blocking capacitor value.
The latter parameter is selected so as to guarantee converter operation at the boundary between continuous and discontinuous operation mode.

That is to guarantee the condition reported in (2.2.13) to actually reduce to an equality at the end of the first topological interval and the primary resonant current to effectively meet the magnetizing current exactly at the end of the switching period.
In this way, indeed, the third interval, described in converter operation analysis, will be skipped and also the length of the fifth interval will be reduced to zero (the intervals II and VI are neglected according to the design preliminary assumption).
In practice, this will turn into solving, for the blocking capacitor value (C_B), the following equation describing the primary current behavior during the output rectifier diode conduction interval:

$$i_{p0} = i_{p3}\cos\left[\frac{(1-D)}{f_{sw}\sqrt{L_{lk}C_B}}\right] + \sqrt{\frac{C_B}{L_{lk}}}\left(n_{12}V_O - v_{C3}\right)\sin\left[\frac{(1-D)}{f_{sw}\sqrt{L_{lk}C_B}}\right] \tag{2.4.8}$$

where, in border line conduction mode conditions, the primary current boundary values (i_{p0} and i_{p3}) will be given by (2.3.7) and (2.3.8) while v_{c3} can be obtained by reducing (2.2.13) to an equality.

Finally, the output filter capacitor can be selected in order to minimize the switching frequency ripple on the LED current under a given percentage of the nominal value:

$$C_O = \frac{\int_{t_3}^{t_4}\left(i_r(t) - I_{LED}\right)dt}{R_\gamma \cdot \Delta i_{LEDsw}} \tag{2.4.9}$$

where t_3 and t_4 are the boundary instants of the output diode conduction interval (with reference to the analysis of paragraph 2.2), I_{LED} is the average load current and Δi_{LEDsw} is the maximum acceptable amplitude of the peak to peak switching frequency ripple on the LED current.

Fig. 2.4.2 shows the main waveforms, describing the behavior of the AHB-flyback converter within the switching period, obtained by simulating, in PLECS® software platform, for a given operating point (i.e. at the minimum input voltage, in nominal conditions: V_{inMIN}=70% $\sqrt{2}$ V_{lRMS_N}) the circuit of Fig. 2.4.1, designed according to the outcomes of the formerly described procedure, listed in Table 2.4.2.

TABLE 2.4.2 - CONVERTER DESIGN OUTCOMES

MAIN CONVERTER PARAMETERS		
NAME	SYMBOL	VALUE
Input voltage variation range	V_{in}	182V - 390V
Maximum input filter capacitance	C_{in}	2.5 μF
Switching frequency	f_{SW}	300 kHz
Transformer turns ratio	n_{12}	8.824
Maximum Magnetizing inductance	L_{mMAX}	250μH
DC blocking capacitor (for L_{lk}~6μH)	C_B	18nF
LED current switching frequency ripple	Δi_{LEDsw}	5% I_{LED}
Output filter capacitor	C_O	20μF
Single dead time interval length	Δt_d	80ns

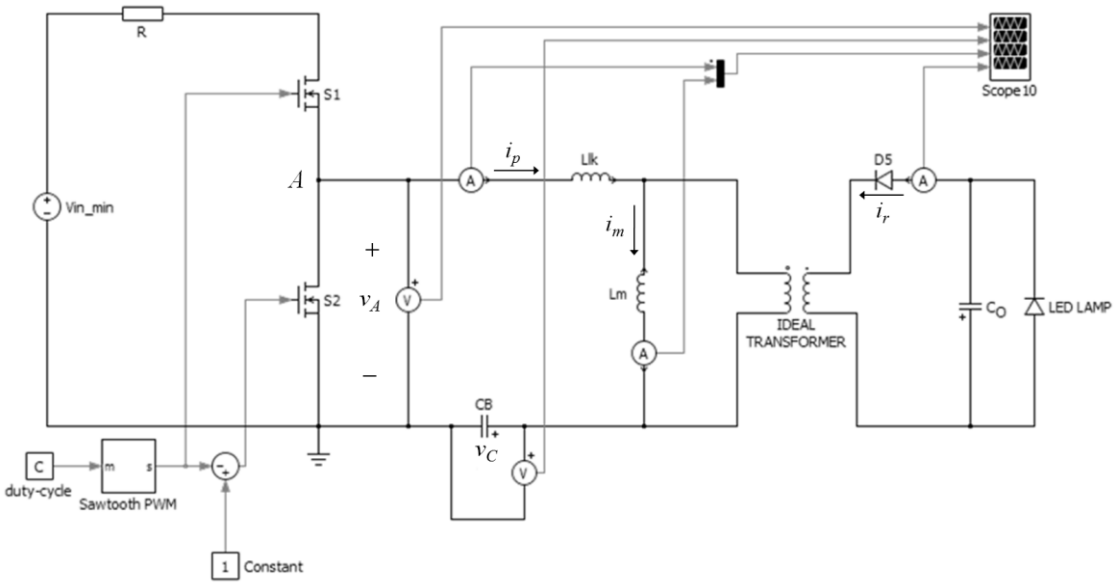


Fig. 2.4.1 - AHB-flyback converter model used for PLECS® simulations.

It can be noticed that, being the DC blocking capacitance designed so as to guarantee CCM/DCM border line operation exactly in this condition, only two different intervals can be identified within the converter switching period (neglecting the switching transients, according to design preliminary assumptions).

The first one corresponds to the conduction of the DC-link connected switch, during a time interval equal to DT_{sw}, while the second one coincides with the turn-on of the ground connected switch and of the output diode, during the remaining part of the switching period ($(1\text{-}D)T_{sw}$).

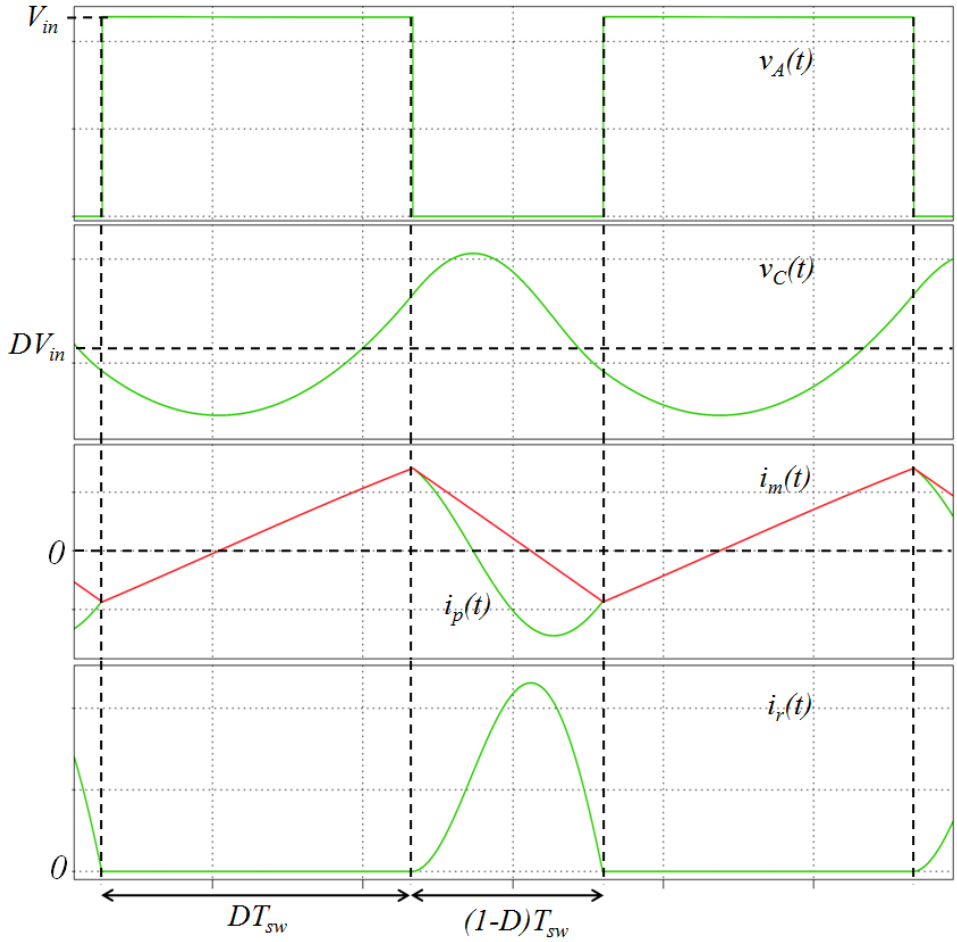


Fig. 2.4.2 - Simulated waveform of the AHB-flyback converter in border line conditions obtained according to the design outcomes of Table 2.4.2.

2.5 AHB-Flyback Converter Control

In the previous paragraph an useful design procedure, based on the AHB-flyback converter operation analysis, presented in paragraph 2.2, and on the hints deriving from the discussion of the soft switching issue, performed in paragraph 2.3, has been proposed.
Its effectiveness has been proved by simulating the converter behavior in the switching period.
However, once converter design has been carried out, the next step will be the implementation of a proper control technique capable of providing output voltage regulation, despite the large input voltage variability, and minimize LED current ripple at double the line frequency.
Keeping in mind the analysis performed in paragraph 2.2, retaining, for sake of simplicity, the design assumption of negligible switching transients (i.e. $t_2=t_1$ and $t_6=t_5$, $i_{p2}=i_{p1}$, $v_{c2}=v_{c1}$, $i_{p6}=i_{p5}=i_{p0}$ and $v_{c6}=v_{c5}=v_{c0}$), by imposing the boundary conditions among the different intervals, the following set of equations ((2.5.1)-(2.5.12))can be found:

$$i_{p1} = i_{p0}\cos\left[\omega_{r1}\cdot\Delta t_1\right] + \frac{\left(V_{in}-v_{c0}\right)}{Z_{r1}}\sin\left[\omega_{r1}\cdot\Delta t_1\right] \tag{2.5.1}$$

$$v_{c1} = V_{in} - \left(V_{in}-v_{c0}\right)\cos\left[\omega_{r1}\cdot\Delta t_1\right] + Z_{r1}i_{p0}\sin\left[\omega_{r1}\cdot\Delta t_1\right] \tag{2.5.2}$$

$$i_{p3} = i_{p2}\cos\left[\omega_{r3}\cdot\Delta t_3\right] - \frac{v_{c2}}{Z_{r3}}\sin\left[\omega_{r3}\cdot\Delta t_3\right] \tag{2.5.3}$$

$$v_{c3} = v_{c2}\cos\left[\omega_{r3}\cdot\Delta t_3\right] + Z_{r3}i_{p2}\sin\left[\omega_{r3}\cdot\Delta t_3\right] \tag{2.5.4}$$

$$i_{p4} = i_{p3}\cos\left[\omega_{r4}\cdot\Delta t_4\right] + \frac{1}{Z_{r4}}\left(n_{12}V_O - v_{C3}\right)\sin\left[\omega_{r4}\cdot\Delta t_4\right] \tag{2.5.5}$$

$$v_{c4} = n_{12}V_O - \left(n_{12}V_O - v_{C3}\right)\cos\left[\omega_{r4}\cdot\Delta t_4\right] + Z_{r4}i_{p3}\sin\left[\omega_{r4}\cdot\Delta t_4\right] \tag{2.5.6}$$

$$i_{p0} = i_{p4}\cos\left[\omega_{r5}\cdot\Delta t_5\right] - \frac{v_{C4}}{Z_{r5}}\sin\left[\omega_{r5}\cdot\Delta t_5\right] \tag{2.5.7}$$

$$v_{c0} = v_{C4}\cos\left[\omega_{r5}\cdot\Delta t_5\right] + Z_{r5}i_{p4}\sin\left[\omega_{r5}\cdot\Delta t_5\right] \tag{2.5.8}$$

$$I_O \cdot n_{21} = f_{sw} \cdot \int_{\Delta t_4} \left[i_m(\tau) - i_p(\tau) \right] d\tau \tag{2.5.9}$$

$$v_{c3} = n_{12} V_O (1+\lambda) \tag{2.5.10}$$

$$i_{p4} = i_{p3} - \frac{n_{12} V_O}{L_m} \Delta t_4 \tag{2.5.11}$$

$$(\Delta t_1 + \Delta t_3 + \Delta t_4 + \Delta t_5) \cdot f_{sw} = 1 \tag{2.5.12}$$

where Δt_i indicates the length of the i^{th} interval.

So, once all converter parameters are known, an accurate estimation of the duty cycle variation can be derived by solving (2.5.1)-(2.5.12) in the unknowns corresponding to the state variables boundary values (i_{p0}, i_{p1}, i_{p3}, i_{p4}, v_{c0}, v_{c1}, v_{c3} and v_{c4}) and by the different intervals' durations (Δt_1, Δt_3, Δt_4 and Δt_5), as a function of the input voltage, so that the desired duty cycle law will be given by:

$$D(V_{in}) = \Delta t_1(V_{in}) \cdot f_{sw} \tag{2.5.13}$$

Otherwise, by observing (2.4.3), it may be inferred that a suitable alternative, to shorten the computation procedure, is to implement a converter duty cycle feed forward control that modulates such parameter according to the law:

$$D(V_{in}) = \frac{V_O n_{12} (1+\lambda)}{V_{in}} \tag{2.5.14}$$

assuming, for sake of simplicity, converter border line operation in the whole input voltage variation range.

Indeed, even if, with the varying input voltage, converter operation will move from CCM/DCM border line conditions, so that (2.5.14) will no longer be rigorously valid, it will still remain a suitably good approximation.

The corresponding duty cycle variation, within the input voltage range (in nominal line conditions, i.e. $V_{lRMS} = V_{lRMS\_N}$), is represented by the continuous trace in Fig. 2.5.1.

As it can be noticed, a further simplification of duty cycle regulation law can be derived by approximating the function (2.5.14) with a piecewise linear trend (dotted trace), that can be easily implemented through a straightforward feed-forward control network (as shown in paragraph 2.7).

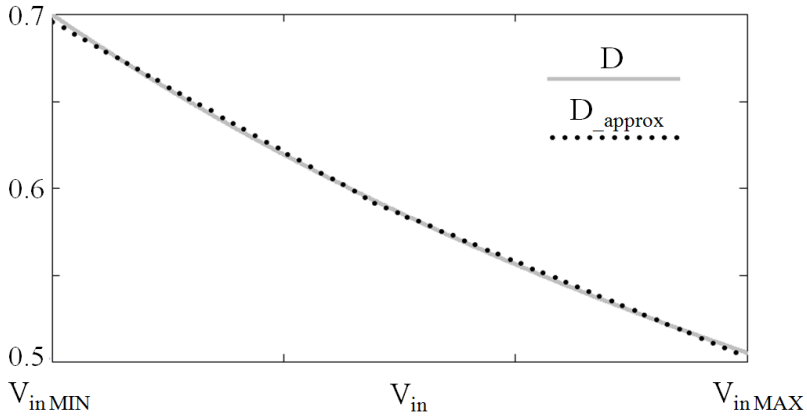


Fig. 2.5.1 - Converter duty-cycle variation (continuous line) and its piecewise linear approximation (dotted line) as a function of the input voltage, needed to keep the output voltage constant despite input voltage variation.

In order to evaluate converter performance, the AHB-flyback converter behavior within the line period has been simulated in PLECS®, controlling duty cycle in feed-forward according to both the law reported in (2.5.14) and also its piecewise linear approximation. The LED current waveform is reported in Fig. 2.5.2 together with the rectified line and the DC-link voltage.

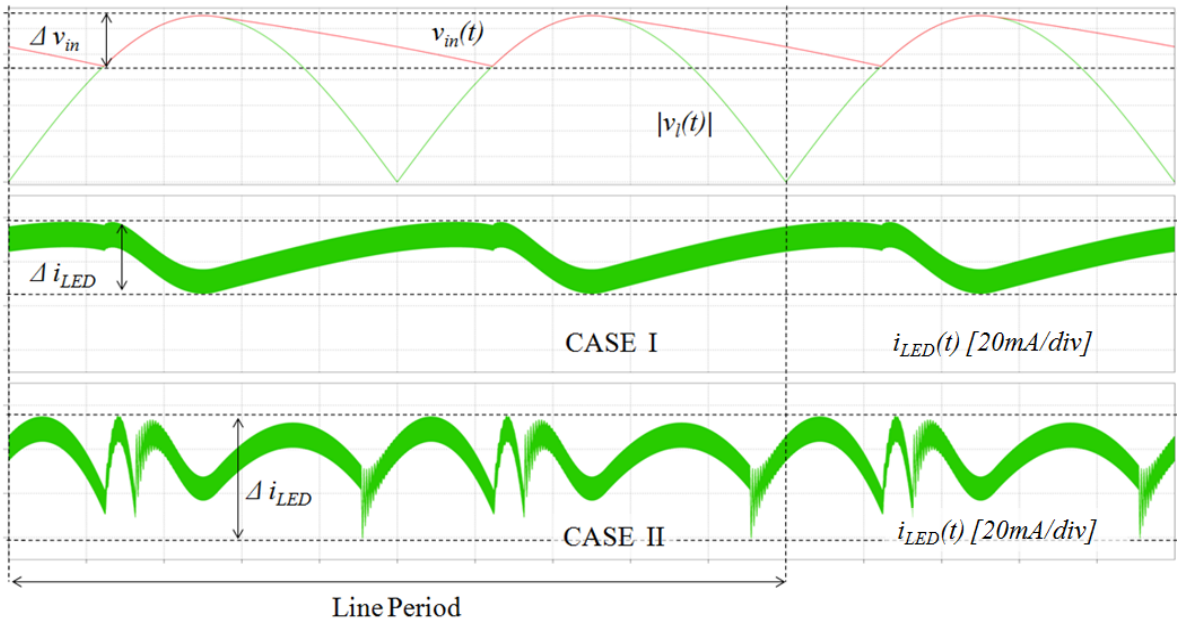


Fig. 2.5.2 - Rectified line voltage, DC-link voltage and LED current simulated waveforms with duty-cycle feed-forward control according to the law (2.5.14) (CASE I) and to the proposed piecewise linear approximation (CASE II).

A residual LED current peak to peak ripple, equal to about 7% of the average output current, can be noticed in the CASE I, corresponding to the implementation of the feed-forward law reported in (2.5.14), that increase up to the 11% in the CASE II, corresponding to the implementation of the piecewise linear approximated law.

Although such measured output current ripple can be considered a quite good result, thus ideally proving the effectiveness of feed-forward duty cycle control in providing output current stabilization, implementation inaccuracy, thermal drifts and several parasitic phenomena could deeply affect its performance in a not easily predictable way.

Moreover if also line voltage (±20%) variability is taken into account, the accuracy of the proposed piecewise linear approximation will decrease, with negative effects on LED current regulation effectiveness.

Therefore, in order to get a more accurate and reliable solution, it is inevitably necessary to turn to the use of a feedback control, adjusting converter duty cycle so as to regulate to zero the difference between the sensed LED current and a fixed current reference.

Hence, in order to be able of properly designing such feedback control loop, the knowledge of converter dynamics, and in particular of the transfer function between the output current and the controlled parameter (i.e. the duty cycle), becomes a mandatory requirement.

A suitable option to get such information could be that of considering the average model of the AHB-flyback converter assuming CCM/DCM border line operating conditions. This will indeed give the possibility to predict converter dynamics, with a quite good approximation, for frequencies up to about one tenth of the switching frequency, namely the range of interest for feedback control loop design.

Since the actual purpose is to find out the dominant poles influencing converter response, the dynamic effects of transformer leakage inductance (L_{lk}) and of the DC-blocking capacitor (C_B) will be assumed to be negligible.

The main reasons underlying this assumption are that on one hand transformer leakage to magnetizing inductance ratio has been supposed to be much lower than unity and on the other the DC-blocking capacitance, that is designed so as to resonate with leakage inductance, actually results to be much lower than the output capacitance.

Therefore, on the basis of these remarks, converter dynamics can be reasonably expected to be effectively dominated by the effects of the transformer magnetizing inductance and of the output filter capacitor. Hypothesis that will be shown to be supported also by simulation outcomes.

In order to derive the desired model, the circuit of Fig. 2.5.3 can be considered, where all components have been reported at transformer primary side, so that:

$$C_O' = \frac{C_O}{n_{12}^2} \tag{2.5.15}$$

$$V_\gamma' = V_\gamma \cdot n_{12}, \qquad R_\gamma' = R_\gamma \cdot n_{12}^2 \tag{2.5.16}$$

$$v_O' = v_O \cdot n_{12} \tag{2.5.17}$$

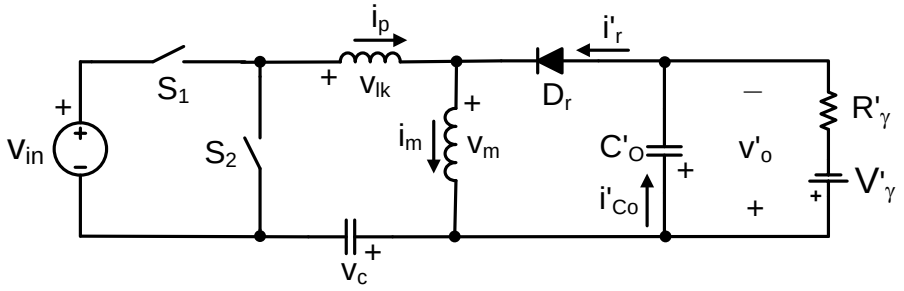


Fig. 2.5.3 - Simplified AHB-flyback converter reported at transformer primary side.

Now, in order to analyze the dynamic behavior of converter average quantities, it is necessary to express them as a function of the system input and control variables (i.e. converter input voltage and duty-cycle). In particular, with reference to the circuit of Fig. 2.5.3, keeping in mind that $\bar{i}_p = 0$ and, in CCM, $\bar{v}_C \simeq \delta \bar{v}_{in} \simeq \bar{v}_O'$, it is possible to write:

$$\begin{cases} \bar{v}_m = \left(\bar{v}_{in} - \bar{v}_O'\right) \cdot \delta - \bar{v}_O' \cdot \left(1 - \delta\right) = \bar{v}_{in} \cdot \delta - \bar{v}_O' \\ \bar{i}_{Co}' = \bar{i}_r' - \dfrac{\bar{v}_O' - V_\gamma'}{R_\gamma'} = \bar{i}_m' - \dfrac{\bar{v}_O' - V_\gamma'}{R_\gamma'} \end{cases} \tag{2.5.18}$$

that, to derive the small signal model, can be rewritten in a more suitable form, by identifying for each quantity (x) a constant contribution (X), related to steady state condition, and a perturbation variable($\hat{x}$):

$$\begin{cases} V_m + \hat{v}_m = \left(V_{in} + \hat{v}_{in}\right) \cdot \left(D + \hat{\delta}\right) - \left(V_O' + \hat{v}_O'\right) \\ I_{Co}' + \hat{i}_{Co}' = I_m + \hat{i}_m + \dfrac{V_\gamma' - V_O'}{R_\gamma'} - \dfrac{\hat{v}_O'}{R_\gamma'} \end{cases} \tag{2.5.19}$$

As concerns the perturbation variables, under small signal assumption, (i.e. $\hat{x} \ll X$), the perturbation product can be neglected, so that, from (2.5.19), the following small signal equations can be derived:

$$\begin{cases} \hat{\mathrm{v}}_m(t) = L_m \dfrac{\partial i_m(t)}{\partial t} \simeq V_{in}\hat{\delta}(t) + D\hat{v}_{in}(t) - \hat{v}_O\,'(t) \\ \hat{\mathrm{i}}_{Co}\,' = C_O\,' \dfrac{\partial v_0\,'(t)}{\partial t} = \hat{i}_m - \dfrac{1}{R_\gamma\,'}\hat{v}_O\,' \end{cases} \tag{2.5.20}$$

from which, by taking the Laplace transform, letting the initial condition to be null, it can be written:

$$\begin{cases} \mathrm{sL_m} \cdot \hat{\mathrm{i}}_m(s) \simeq V_{in}\hat{\delta}(s) + D\hat{v}_{in}(s) - \hat{v}_O\,'(s) \\ \mathrm{sC_O}\,' \cdot \hat{v}_O\,'(s) = \hat{i}_m(s) - \dfrac{1}{R_\gamma\,'}\hat{v}_O\,'(s) \end{cases} \tag{2.5.21}$$

So, solving the first equation for $\hat{\mathrm{i}}_m(s)$ and substituting the obtained solution in the second equation, an expression of the output voltage as a function of the input voltage and of the control variable can be finally found:

$$\hat{v}_O\,'(s) = \frac{V_{in}}{\left(\mathrm{s^2L_mC_O}\,' + \mathrm{s}\dfrac{\mathrm{L_m}}{R_\gamma\,'} + 1\right)} \cdot \hat{\delta}(s) + \frac{D}{\left(\mathrm{s^2L_mC_O}\,' + \mathrm{s}\dfrac{\mathrm{L_m}}{R_\gamma\,'} + 1\right)} \cdot \hat{v}_{in}(s) \tag{2.5.22}$$

from which the input to output and control to output transfer functions can be respectively derived:

$$G_{ui}(s) = \left.\frac{\hat{v}_O\,'(s)}{\hat{v}_{in}(s)}\right|_{\hat{\delta}(s)=0} = \frac{D}{\left(\mathrm{s^2L_mC_O}\,' + \mathrm{s}\dfrac{\mathrm{L_m}}{R_\gamma\,'} + 1\right)} \tag{2.5.23}$$

$$G_{ud}(s) = \left.\frac{\hat{v}_O\,'(s)}{\hat{\delta}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{V_{in}}{\left(\mathrm{s^2L_mC_O}\,' + \mathrm{s}\dfrac{\mathrm{L_m}}{R_\gamma\,'} + 1\right)} \tag{2.5.24}$$

Finally, from (2.5.24), keeping in mind (2.5.15), (2.5.16) and (2.5.17), the desired transfer function between converter load current and duty cycle small signal variation can be computed and written as:

$$G_{id}(s) = \left.\frac{\hat{i}_{LED}(s)}{\hat{\delta}(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{G_{ud}(s)}{n_{12}R_\gamma} = \frac{V_{in}}{n_{12}R_\gamma} \cdot \frac{1}{\left(1 + \mathrm{s}\dfrac{\mathrm{L_m}}{n_{12}^2 R_\gamma} + \mathrm{s}^2\dfrac{\mathrm{L_mC_O}}{n_{12}^2}\right)} \tag{2.5.25}$$

So, as it can be observed from (2.5.25), for frequencies sufficiently lower than the switching frequency, the resulting duty cycle to output current transfer function will

behave like a second order function, characterized by the presence of two complex conjugate poles at the frequency:

$$f_{p1,2} = \frac{1}{2\pi} \cdot \frac{n_{12}}{\sqrt{\mathrm{L_m C_O}}} \tag{2.5.26}$$

and by a DC gain (in dB) equal to:

$$G_{id0\_dB} = 20\log\left(\frac{V_{in}}{n_{12}R_{\gamma}}\right) \tag{2.5.27}$$

The bode plot of magnitude and phase of the derived control to LED current transfer function, computed in correspondence of the maximum input voltage in nominal conditions (V_{in}=325V), with reference to the converter design outcomes listed in Table 2.4.2, is shown in Fig. 2.5.4.

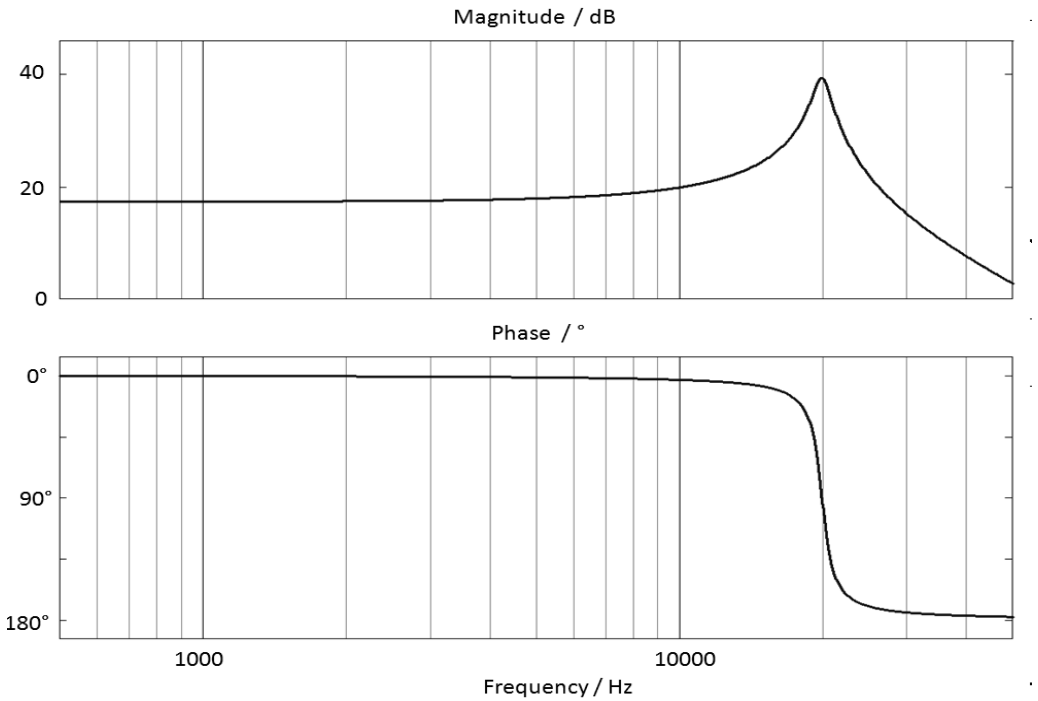


Fig. 2.5.4 - Bode plot of the control to LED current transfer function of the AHB-flyback converter analytically derived.

By comparing such diagram with that obtained in the same conditions through the AC sweep converter simulation in PLECS®, shown in Fig. 2.5.5, the effectiveness of the model predictions can be proved.

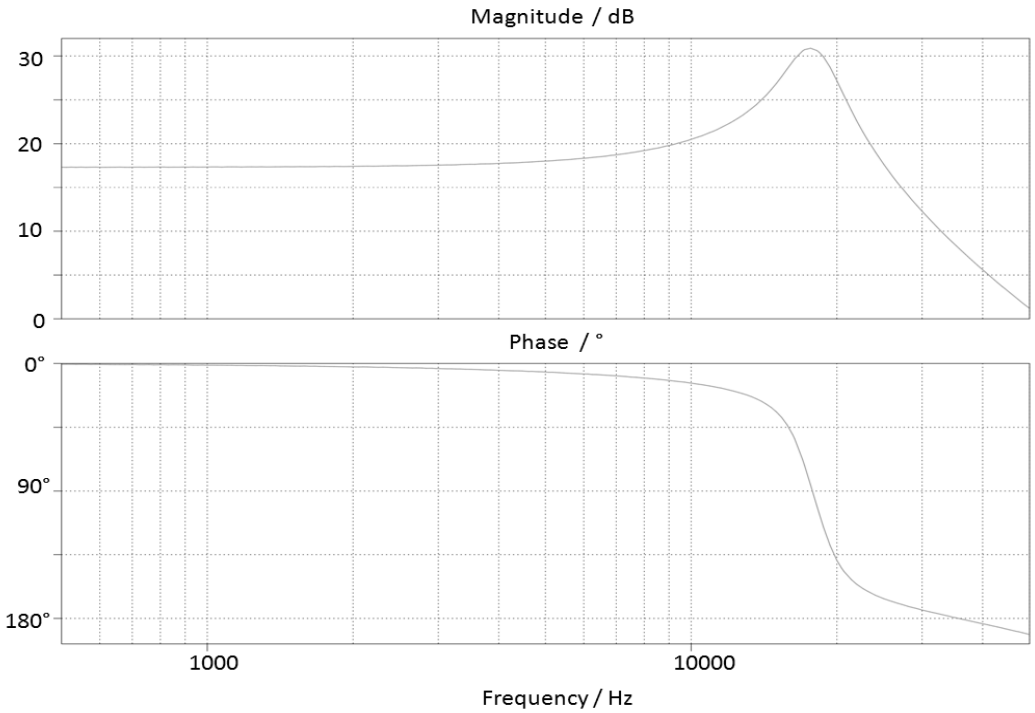


Fig. 2.5.5 - Bode plot of the control to LED current transfer function of the AHB-flyback converter derived through AC-sweep simulation in PLECS®.

As it can be noticed, the model accurately catches the AHB-flyback converter dynamic behavior in the whole frequency range of interest, being the effects of the unpredicted high frequency dynamics visible only above one tenth of converter switching frequency (i.e. above 30kHz).

It is worth to mention, however, that, in order to get a complete description of converter dynamics including its high frequency behavior, a more general approach based on the state space averaging technique can be considered, as shown in [49].

Once the desired converter control to LED current transfer function, has been derived, assuming all the other contributions shown in the block diagram of Fig. 2.5.6 to be known, it is therefore possible to carry out the control loop design.

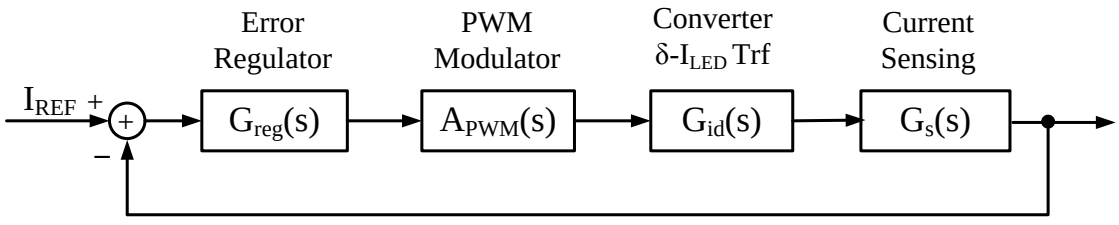


Fig. 2.5.6- Block diagram of converter feedback control loop.

In order to improve the controlled converter performances three main goals should be achieved.

The first one is to guarantee a high loop gain in the largest possible frequency range, in order to get high system static precision and noise rejection; the second objective is to maximize loop frequency response bandwidth, in order to speed up system transient response; finally, the last goal is to assure proper loop frequency response phase margins, with the aim of preventing control instability and transient overshoots.

As an example, Fig. 2.5.7 shows the input voltage and LED current waveforms, obtained by simulating converter behavior, when a feedback control loop, with an overall frequency response bandwidth of 5kHz, is implemented, relying on the use of a PI regulator.

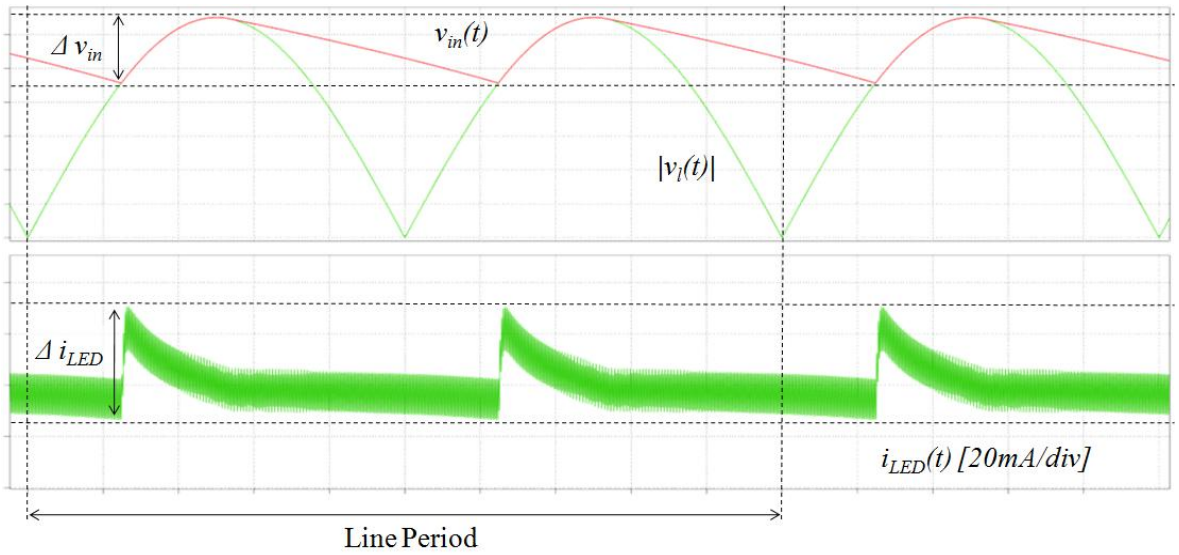


Fig. 2.5.7 - Rectified line voltage, DC-link voltage and LED current simulated waveforms in correspondence of load current feedback control.

As it can be noticed, the load current feedback control allows to achieve a good current stabilization, being the residual current ripple reduced to only 5% of current average value.

A further improvement of LED current control can be obtained by combining the feedback control with the previously proposed feed-forward control technique, that is presetting converter duty-cycle, as a function of the varying input voltage, through a feed-forward action and then adjusting its value through the use of feedback control. The beneficial effects deriving from the combination of both feedback and feed-forward actions can be observed by looking at the LED current simulated waveform reported in Fig. 2.5.8, from which it can be noticed that the peak to peak ripple at twice the line frequency of the LED current is reduced to 2% of current average value.

It is worth to finally observe that, being the perturbation at twice the line frequency well within the control loop bandwidth, it will be effectively rejected.

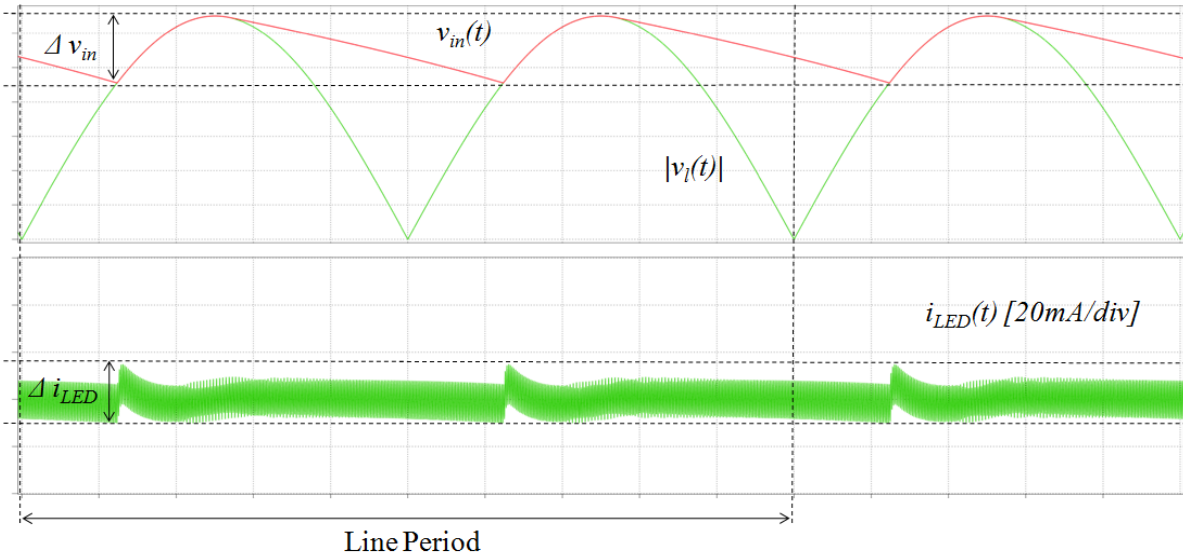


Fig. 2.5.8 - Rectified line voltage, DC-link voltage and LED current simulated waveforms in correspondence of the combination of load current feedback and feed-forward control.

2.6 Optimization Techniques

Observing the primary current waveform, derived thorough the analysis of converter operation principles of paragraph 2.2 and reported in Fig. 2.2.8, it can be noticed that only a minor part of the current circulating at transformer primary side is delivered to the output filter capacitor and to the LED load, being the majority of it recycling, through transformer magnetizing inductance.
Nevertheless, the fundamental importance of converter magnetizing current to guarantee the zero voltage switching of the half bridge MOSFETs has been discussed, focusing on switching transients, in paragraph 2.3.
Consequently, according to the converter design procedure proposed in paragraph 2.4, the magnetizing inductance value has to be selected so as to guarantee the minimum commutated current, necessary to complete the charge/discharge of the half bridge switches parasitic capacitances, within the switching transient dead times, in correspondence of the worst case condition (i.e. at the minimum input voltage).

However, as discussed above in chapter introduction, the need of limiting the harmonic content of converter input current, so as to comply with the EN 61000-3-2 standard, calls for a minimization of the input filter capacitance that results in a large converter input voltage ripple that has to be properly managed.
So, in order to minimize LED current ripple at twice the line frequency, the implementation of a load current control by a proper feedback and /or feed-forward regulation of converter duty-cycle has been discussed in paragraph 2.5.
Therefore, once the magnetizing inductance value has been selected, from (2.3.5) it can be easily inferred that the decrease of converter duty cycle, with the increasing input voltage, will produce recycling current values, highly exceeding the threshold level necessary to guarantee the zero voltage switching operation, with detrimental effects on converter efficiency.

As a proof, the simulated magnetizing current envelope waveform reported in Fig. 2.6.1, showing a significant variation of recycling current peak to peak ripple as a function of the input voltage, can be considered.
As it can be observed, in correspondence of the nominal line voltage, the magnetizing current envelope almost doubles within the line half period due to the varying input voltage.

Moreover, a further variation of peak to peak magnetizing current ripple is registered if also the line voltage variability (±20% of the nominal RMS voltage value) is taken into account, calling for the study of a ripple stabilization method.

Indeed, although sub-optimum converter operation is a well known intrinsic limitation of single stage topology based solutions, some kind of optimization, aimed at minimizing the amount of converter recycling current, is necessary in order to fulfill the specification mandating an overall ballast efficiency higher than 80%.

Now, observing the magnetizing current ripple expression, reported in (2.3.5), it can be noticed that the output voltage (V_O) is imposed by the specifications of the considered application, while transformer's turns ratio (n_{12}) and converter's duty cycle (D) are fixed by design.

Therefore the only parameters that can be handled in order to adjust the recycling current level, results to be the converter switching frequency (f_{sw}) and the transformer magnetizing inductance (L_m).

Based on this observation, two different kinds of approach has been investigated, to address the magnetizing current peak to peak stabilization issue, and will be presented here in the following.

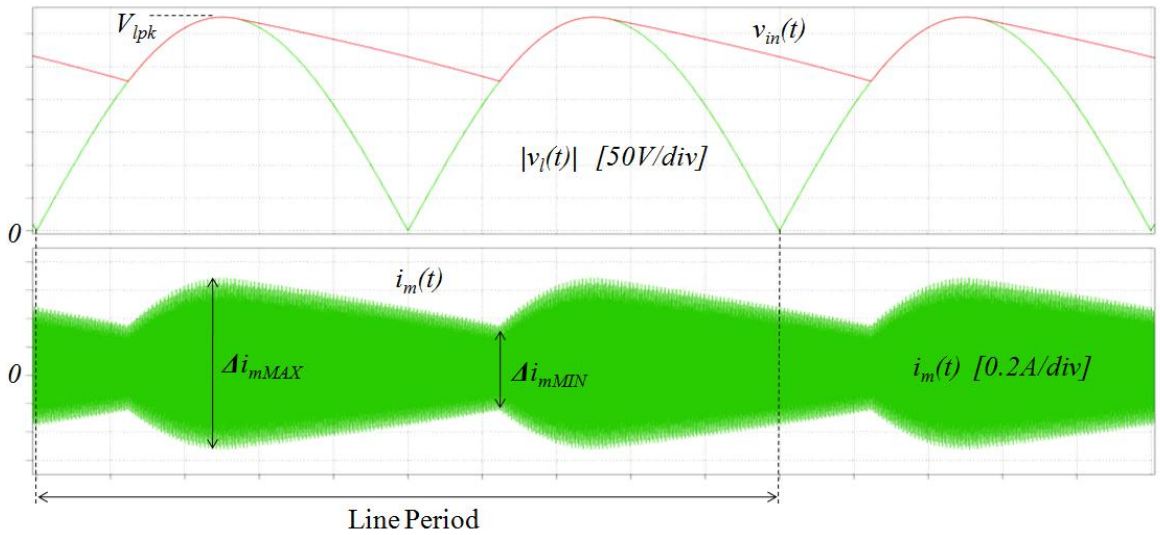


Fig. 2.6.1 - Rectified line voltage, DC-link voltage and recycling current envelope waveforms, in nominal line voltage conditions.

2.6.1 Switching Frequency Modulation

The first optimization technique that will be described, relies on the idea of varying converter switching frequency as a function of the input voltage, so as to compensate for the DC-link voltage ripple effects.

The main concern in this regards, is, clearly, the need to find out a proper modulation law, expressing the switching frequency as a function of the DC-link voltage, capable of guaranteeing the desired magnetizing current stabilization.

In order to reach this goal, another constraint, imposing the recycling current peak to peak ripple (i_{p2}-i_{p0}) to remain constant, despite the input voltage variation, can be added to the set of the equations describing converter behavior within the switching period ((2.5.1)-(2.5.12)).

Solving this new system, as a function of the input voltage, in the unknowns corresponding to state variables boundary values, topologic intervals lengths and converter switching frequency, the desired modulation law can be derived.

Otherwise, a suitable alternative, to shorten the computation procedure and get an handy, although approximate, version of such law, could be to assume, for sake of simplicity, converter border line operation in the whole input voltage variation range.

Under such assumption, indeed, keeping in mind (2.3.5) and (2.4.3) the switching frequency modulation law can be reasonably expressed as:

$$f_{sw} \simeq \frac{n_{12} V_O (1-D)}{L_m \Delta i_m} \tag{2.6.1}$$

where:

$$D = \left[n_{12} V_O (1+\lambda) \right] \cdot \frac{1}{V_{in}} \tag{2.6.2}$$

and Δi_m is the magnetizing peak to peak ripple in correspondence of the minimum DC-link voltage level, designed so as to comply with soft switching requirements.

The switching frequency variation, corresponding to (2.6.1), computed according to the parameters listed in Table 2.4.1 and Table 2.4.2 and normalized to its value in correspondence of the minimum input voltage, is shown by the continuous trace in Fig. 2.6.2, as a function of the DC-link voltage.

Also in this case, the expression derived in (2.6.1) can be suitably approximated through a piecewise linear trend (as shown by the dotted trace in Fig. 2.6.2) in order to simplify the set-up of the feed-forward switching frequency control network.

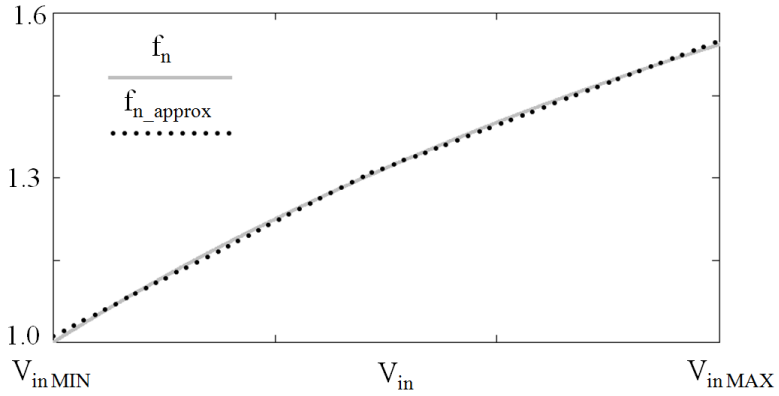


Fig. 2.6.2 – Switching frequency variation (normalized to its minimum value) needed to keep the primary current ripple constant in the whole input voltage range: analytical (continuous trace), linear piecewise approximation (dotted trace).

The performance of the proposed technique have been tested, through converter simulation in the PLECS® platform, regulating converter switching frequency according to both the law reported in (2.6.1) and its piecewise linear approximation.

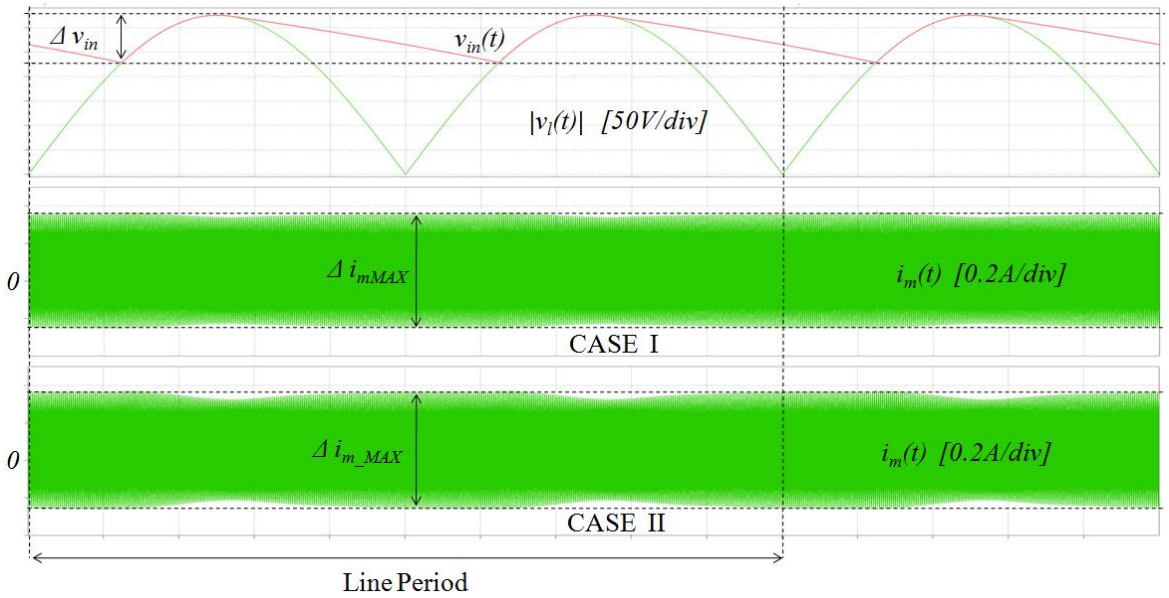


Fig. 2.6.3 – Rectified line voltage, DC-link voltage and recycling current envelope waveforms with switching frequency feed-forward control according to the law (2.6.1) *(CASE I) and to the proposed piecewise linear approximation (CASE II).*

By observing the envelope waveform of the simulated magnetizing current, reported in Fig. 2.6.3, it can be noticed the effectiveness of the described switching frequency control in stabilizing converter recycling current, despite the DC-link voltage variation. The peak to peak magnetizing ripple variation results indeed to be almost canceled, being the residual alteration lower than 10% of the minimum ripple value.

2.6.2 Magnetizing Inductance Modulation

The second approach to the recycling current stabilization issue is based on the idea of balancing the input voltage ripple effects by varying the transformer magnetizing inductance value.

The purpose is to exploit the current controlled variable inductors technique ([50]-[77]) in order to modulate the magnetizing inductance value as a function of DC-link level, with the aim of keeping the magnetizing current peak to peak ripple constantly equal to the minimum level that is necessary to guarantee zero voltage switching operation.

By observing the typical magnetization curve of a magnetic material (Fig. 2.6.4), it can be noticed that, by increasingly biasing the magnetic field strength (H) through the transformer core, it is possible to gradually force its material toward the saturation region, so as to progressively reduce its magnetic permeability ($\mu = \partial B / \partial H$).

The consequence is the increasing of material equivalent reluctance to the magnetic flux:

$$\mathrm{R}_{eq} = \frac{1}{\mu}\frac{l_e}{A_e} \tag{2.6.3}$$

that obviously turns, as can be easily derived from Faraday's law, in a decreasing of the inductance value:

$$L = \frac{\partial\left[\int u(t)dt\right]}{\partial I} = \frac{N^2}{\mathrm{R}_{eq}} = \frac{N^2 A_e}{l_e}\frac{\partial B}{\partial H} = \mu\frac{N^2 A_e}{l_e} \tag{2.6.4}$$

where A_e and l_e are the effective cross section and length of the magnetic path and N is the number of the winding's turns.

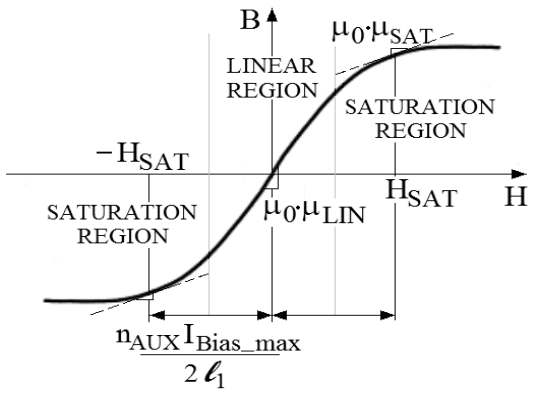


Fig. 2.6.4 - Typical magnetization curve of magnetic materials.

It is thus easy to understand that, in order to change the inductance value within the following boundary values:

$$L_{\max} = \mu_{LIN} \frac{N^2 A_e}{l_e} \quad \text{and} \quad L_{\min} = \mu_{SAT} \frac{N^2 A_e}{l_e} \tag{2.6.5}$$

it will be sufficient to add an auxiliary winding to the transformer, biased with a continuous current, ranging between zero and:

$$I_{BIAS\_\max} = \frac{H_{SAT} \cdot l_e}{n_{AUX}} \tag{2.6.6}$$

where n_{AUX} is the total number of the bias winding turns and the magnetic field strength (H_{SAT}) is assumed to be constant along the whole magnetic path l_e.

Hence, as concerns the target application, it can be inferred that, the desired goal of adjusting transformer magnetizing inductance as a function of the input voltage, can be easily achieved by properly controlling the auxiliary winding bias current as a function of the DC-link voltage level.

The procedure to find out a proper magnetizing inductance modulation law is similar to that previously described for the switching frequency control technique. So, once again, an accurate control function can be derived by solving the set of equations (2.5.1)-(2.5.12), with the addition of an extra constraint imposing the recycling current ripple to be constant. The only difference is that this time the switching frequency will be kept constant, while the magnetizing inductance is treated as an unknown variable. However, also in this case, a simpler solution can be found under the assumption of border line conduction mode converter operation. This approximated relationship can be easily derived by solving (2.6.1) for the magnetizing inductance:

$$L_m \simeq \frac{n_{12} V_O (1-D)}{f_{sw} \Delta i_m} \tag{2.6.7}$$

where, the duty cycle depends on the input voltage value according to (2.6.2) and, once again, the magnetizing ripple (Δi_m) is that designed, at the minimum input voltage, so as to comply with soft switching requirements.

The corresponding magnetizing inductance variation (L_{Mn}), computed according to the parameters listed in Table 2.4.1 and Table 2.4.2 and normalized to its value in correspondence of the minimum input voltage, is shown by the continuous trace in Fig. 2.6.5 as a function of the DC-link voltage.

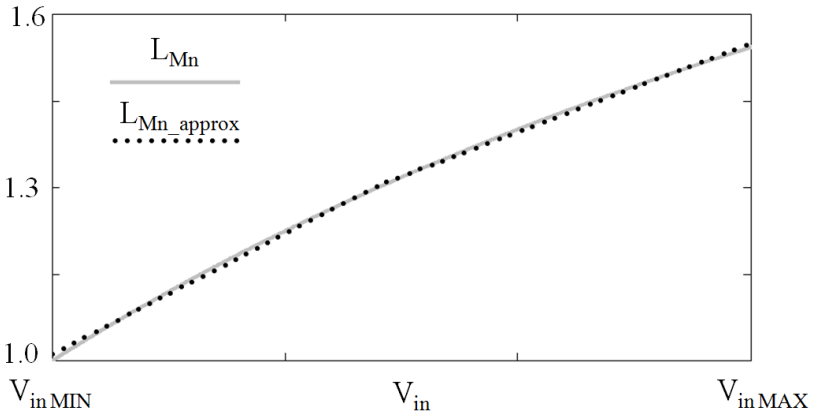


Fig. 2.6.5 - Magnetizing inductance variation (normalized to its minimum value) needed to keep the primary current ripple constant in the whole input voltage range: analytical (continuous trace), linear piecewise approximation (dotted trace).

Also in this case the proposed optimization technique performance have been tested, by means of converter simulation, exploiting the model of the variable inductor provided in PLECS® and implementing a magnetizing inductance feed-forward control law based on both (2.6.7) and its piecewise linear approximation. The outcomes in both cases, as concerns recycling current envelope are illustrated in Fig. 2.6.6.

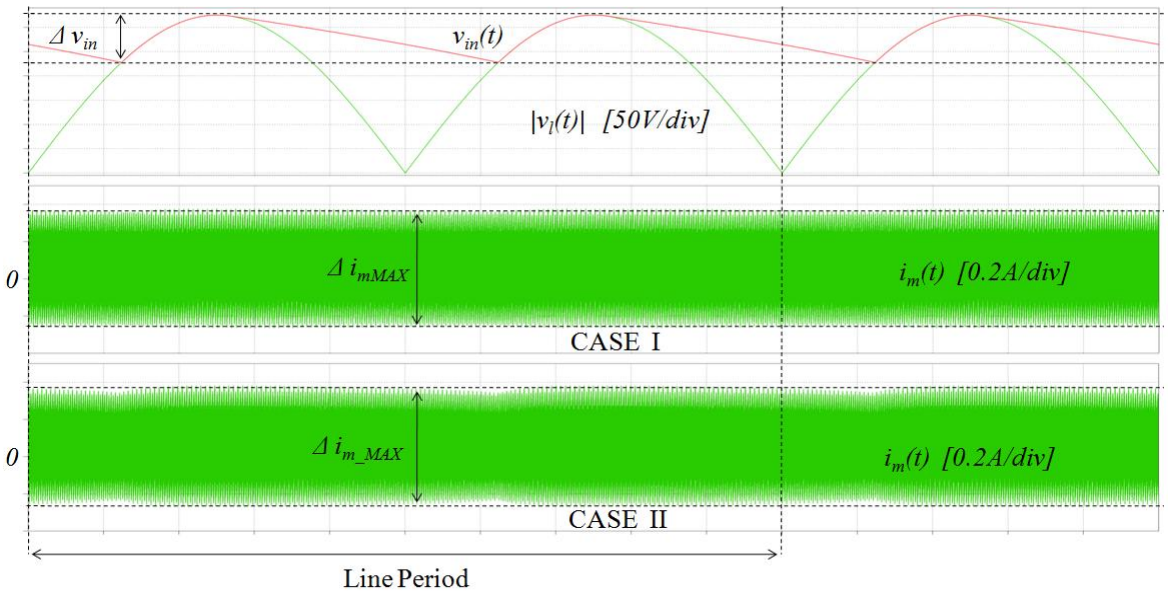


Fig. 2.6.6 – Rectified line voltage, DC-link voltage and recycling current envelope waveforms with magnetizing inductance feed-forward control according to the law (2.6.7) (CASE I) and to the proposed piecewise linear approximation (CASE II).

As it can be noticed, the effectiveness of the presented technique is proven, being the resulting peak to peak ripple of the recycling current almost constant in both the considered cases, despite DC-link voltage variation, in the whole line period.

2.7 Experimental Results

A prototype of the asymmetrical half bridge flyback converter has been built, according to the outcomes of the design procedure reported in Table 2.4.2, using the devices listed in Table 2.7.1, with the aim of testing the correspondence of the real converter behavior with the analysis performed.

In particular, the attention has been focused on checking the achievement of zero voltage switching operation, the compliance with the EN 61000-3-2 standard and the practical effectiveness of the proposed optimization techniques.

Therefore, converter open loop behavior within the switching period, has been tested at first. From the experimental waveforms of converter primary current and half bridge voltage, shown in Fig. 2.7.1, in correspondence of the minimum input voltage, two main aspects should be noticed. The first one is the achievement of border line operation between continuous and discontinuous operation mode, proven by converter primary current waveform, whose resonant interval actually matches the whole conduction interval of the ground connected switch. The second aspect is, instead, the accomplishment of the half bridge switches soft turn-on confirmed by the gradually rising and falling edges of the half bridge voltage, within the switching transient dead times.

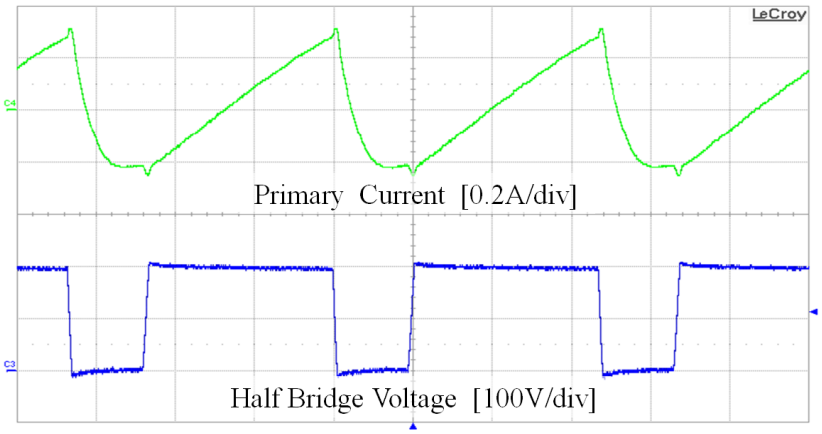


Fig. 2.7.1 – Converter primary current and half bridge voltage experimental waveforms Timebase 1μs/div.

Furthermore, as regards converter behavior in the line period, the effectiveness of the single feed-forward and feedback proposed output regulation techniques has been tested and compared with the performance guaranteed by the combination of both control actions.

It is worth to note that, if the piecewise linear approximation, discussed in paragraph 2.6, is considered, the feed-forward duty cycle regulation network can be easily implemented. As shown in the simplified scheme of Fig. 2.7.2, it can be simply made by means of some resistances, an operational amplifier and a zener diode, necessary to change the input voltage divider ratio in correspondence of a given DC-link level.

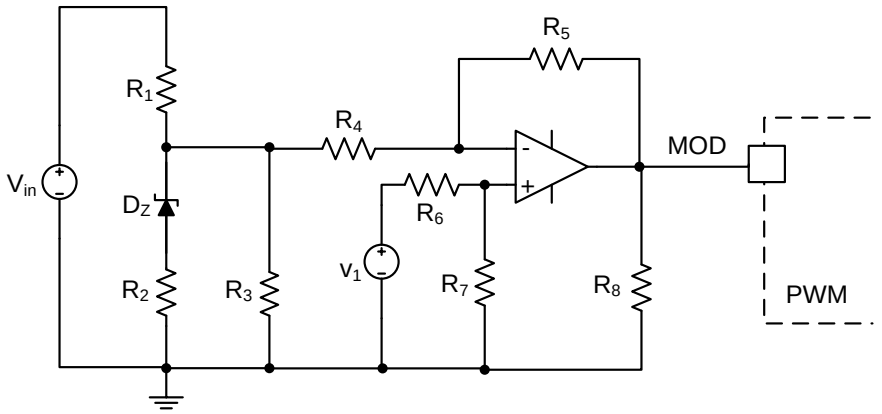


Fig. 2.7.2 – Simplified electrical scheme of converter duty cycle feed-forward control network.

On the other hand, feedback control is realized, according to the block diagram of Fig. 2.5.6, by regulating to zero the difference between a proper reference signal and the load current by means of a PI controller, capable of guaranteeing an overall loop bandwidth of 5 kHz and a phase margin of about 60°. An hall effect sensor is used to measure the output current in order to preserve the galvanic isolation provided by the transformer.

TABLE 2.7.1 - MAIN PROTOTYPE DEVICES

POWER STAGE		CONTROL STAGE	
DEVICE	NAME	DEVICE	NAME
Diode bridge	DBS155G	P.W. Modulator	UC3824
Input filter capacitor	B32562J6105K	Driver	NCP5181
Half bridge switches	FQS4903	Current sensor	AC712
DC blocking capacitor	ECWU2183V16	Operational Amplifiers	LM358
Transformer	EFD15 N87	Zener diode	BZX84C10
Output rectifier diode	IR 10BQ060	NPN transistor	BC817
Output filter capacitor	20μF	PNP transistor	BC807

The experimental waveform of the LED current, in correspondence of load current feed-forward control, feedback control and the combination of both control actions is shown in Fig. 2.7.3.

As it can be noticed, the measured current ripple at twice the line frequency perfectly agrees with the outcomes of the converter simulations performed in the same conditions (Fig. 2.5.2 - CASE II, Fig. 2.5.7 and Fig. 2.5.8, respectively).

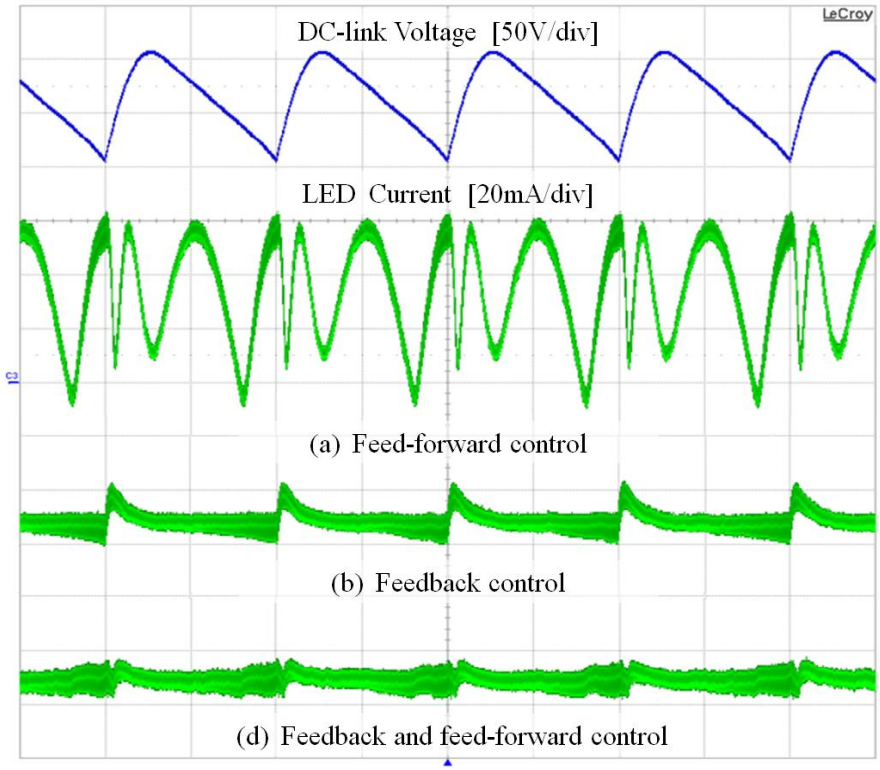


Fig. 2.7.3 – Converter DC-link voltage and LED current experimental waveforms with: (a) feed- forward, (b) feedback, (c) feedback and feed-forward load current control. Timebase: 5ms/div.

As formerly discussed, in such conditions, if no kind of recycling current ripple stabilization action is performed, the magnetizing current envelope widely varies within the line period due to DC-link input voltage ripple. This negative effect, first inferred through converter analysis and then confirmed by simulations, has been also experimentally verified, as can be noticed by looking at the primary current envelope reported in Fig. 2.7.4.

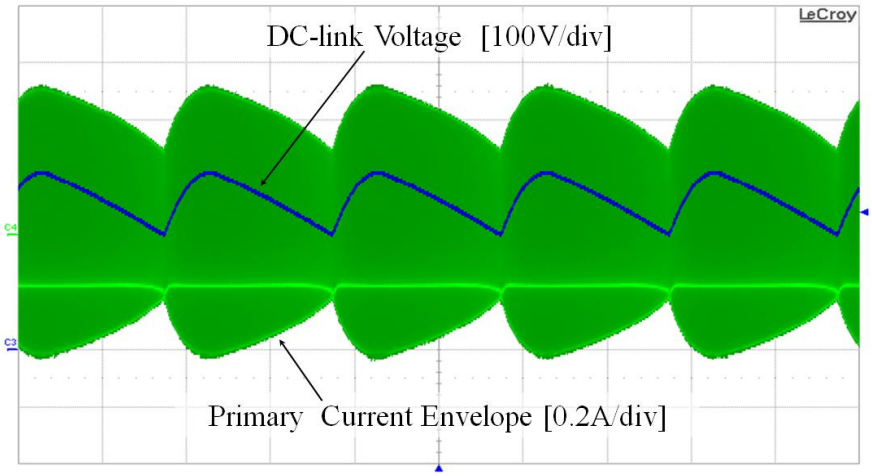
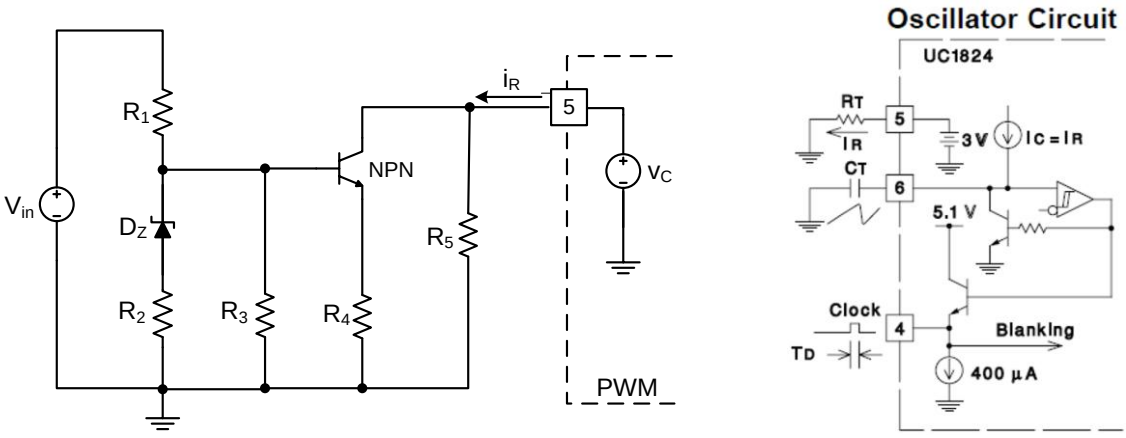


Fig. 2.7.4 - Converter DC-link voltage and primary current envelope experimental waveforms. Timebase: 5ms/div.

The previously discussed optimization techniques have therefore been implemented, with the aim of improving converter behavior.

In particular, as concerns the converter switching frequency modulation technique, a feed forward control network has been built, according to the scheme reported in Fig. 2.7.5 (a), to implement the piecewise linear approximation of the frequency control law, proposed in paragraph 2.6.

As it can be observed, the idea is to dynamically change, as a function of the DC-link voltage level, the equivalent timing resistance of the PWM oscillator circuit (Fig. 2.7.5 (b)), so as to change the pulse width modulation ramp frequency and consequently the converter switching frequency.



(a) *(b)*

Fig. 2.7.5 - Simplified electrical scheme of: (a) converter switching frequency feed-forward control network, (b) pulse width modulator oscillator circuit.

Also in this case, the transition from one linear piece to the other is achieve through the use of a zener diode that, above a given DC-link voltage level starts conducting, varying the relationship between the input voltage and the NPN bipolar junction transistor driving signal.

The improvement achieved thanks to the use of this technique is shown in Fig. 2.7.6, that gives evidence of the effectiveness of the proposed optimization method in reducing the primary current envelope peak to peak ripple from almost 100% to less than 10%.

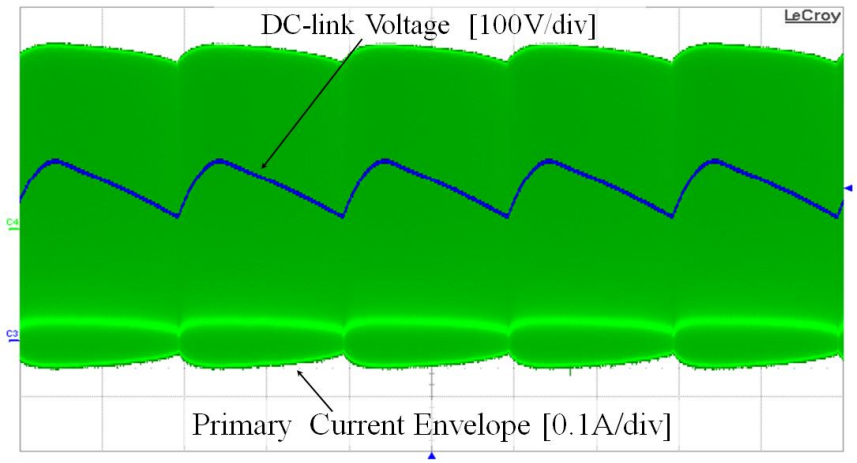


Fig. 2.7.6 - Converter DC-link voltage and primary current envelope experimental waveforms, with switching frequency feed-forward control. Timebase: 5ms/div.

As concerns the other kind of ripple stabilization approach, based on the use of the current controlled inductors technique, according to the analysis performed in paragraph 2.6, a variable mutual inductor has been implemented on a double E magnetic core.

As shown in Fig. 2.7.7 (a), the main (primary and secondary) windings have been placed on the center leg, while two series connected auxiliary windings have been positioned on transformer's outer legs, wrapped with opposite polarity, so as to compensate for the AC voltage induced by the main windings.

Now, considering the equivalent reluctance model of the magnetic circuit, reported in Fig. 2.7.7 (b) the total equivalent reluctance of the core can be written as:

$$R_{eq} = \frac{R_1}{2} + 2R_2 + R_g \tag{2.7.1}$$

where:

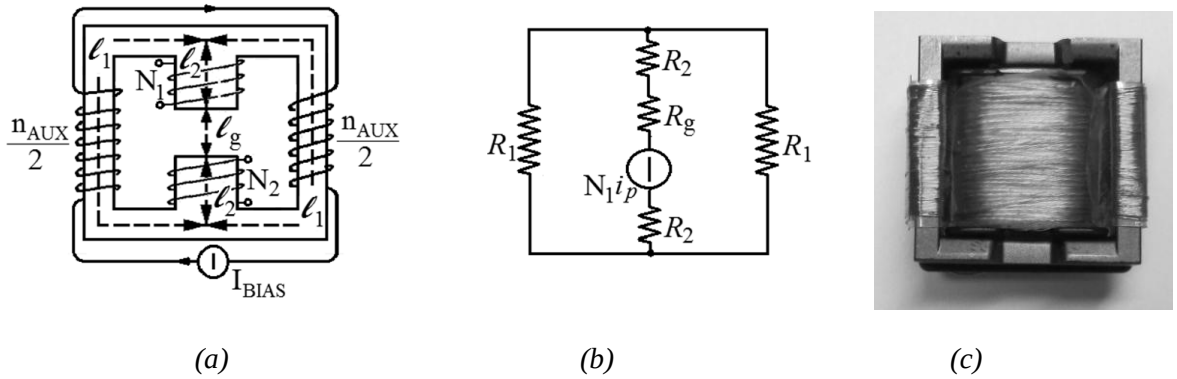
$$R_1 = \frac{l_1}{\mu_0 \mu_{r1} A_1} \quad , \quad R_2 = \frac{l_2}{\mu_0 \mu_{r2} A_2} \quad , \quad R_g \cong \frac{l_g}{\mu_0 A_2} \tag{2.7.2}$$

are the contributions corresponding to the paths l_1, l_2 and l_g, respectively (being: A_1 and A_2 the cross section of the outer and central legs, μ_0 the vacuum permeability and μ_{r1} and μ_{r2} the relative permeability of the core material along the corresponding magnetic paths l_1 and l_2, respectively).

So, that from (2.6.4), the expression of the magnetizing inductance results to be:

$$L_m = \frac{N_1^2}{R_{eq}} = \mu_0 N_1^2 \cdot \left(\frac{l_1}{2\mu_{r1} A_1} + \frac{2l_2 + \mu_{r2} l_g}{\mu_{r2} A_2} \right)^{-1} \tag{2.7.3}$$

where N_1 is the number of primary winding's turns.



(a) *(b)* *(c)*

Fig. 2.7.7 - (a) Variable mutual inductor scheme, (b) equivalent reluctance model of the magnetic circuit, (c) variable inductor prototype.

With such configuration, controlling the auxiliary winding bias current it is therefore possible to vary the relative magnetic permeability of the core material along transformer peripheral path, consequently changing the magnetizing inductance value in the interval limited between the following two boundary values:

$$L_{m\_\min} = \frac{\mu_0 N_1^2}{\frac{l_1}{2\mu_{SAT} A_1} + \frac{2l_2 + \mu_{LIN} l_g}{\mu_{LIN} A_2}} \tag{2.7.4}$$

$$L_{m\_\max} = \frac{\mu_0 N_1^2}{\frac{l_1}{2\mu_{LIN} A_1} + \frac{2l_2 + \mu_{LIN} l_g}{\mu_{LIN} A_2}} \tag{2.7.5}$$

where μ_{LIN} is the core material relative magnetic permeability in zero bias conditions, while being μ_{SAT} its value in correspondence of material saturation.

The variation of the magnetizing inductance value, of the implemented transformer prototype (Fig. 2.7.7 (c)), as a function of the bias current applied to the auxiliary windings has been tested; the resulting magnetizing inductance (L_m) versus bias current (I_{Bias}) characteristic is reported in Fig. 2.7.8.

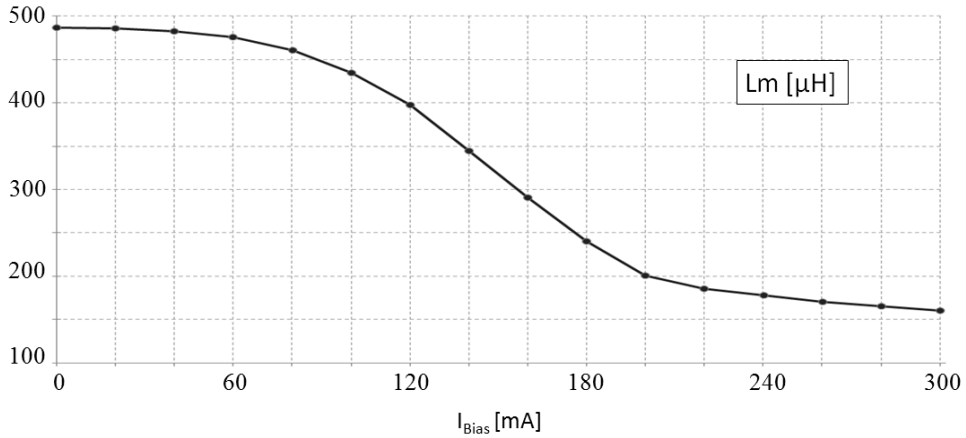


Fig. 2.7.8 - Characteristic of transformer magnetizing inductance variation as a function of the bias current.

By combining the data illustrated in such figure, with the information relative to the desired inductance variation law, it is therefore possible to derive the curve of the bias current as a function of the input voltage, shown in Fig. 2.7.9.

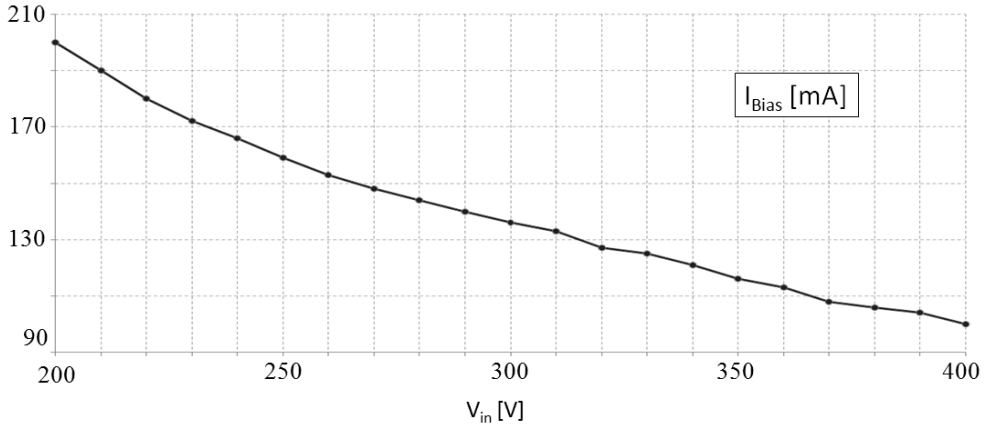


Fig. 2.7.9 - Characteristic of the bias current variation, as a function of the input voltage, necessary to keep the magnetizing current peak to peak ripple stable within the line half period.

Observing Fig. 2.7.9 it can be noticed that the bias current function of the input voltage can be reasonably approximated with a linear trend, so that the needed bias current can easily

be generated, as a function of the DC-link voltage, simply implementing a feed-forward network like the one shown in Fig. 2.7.10.

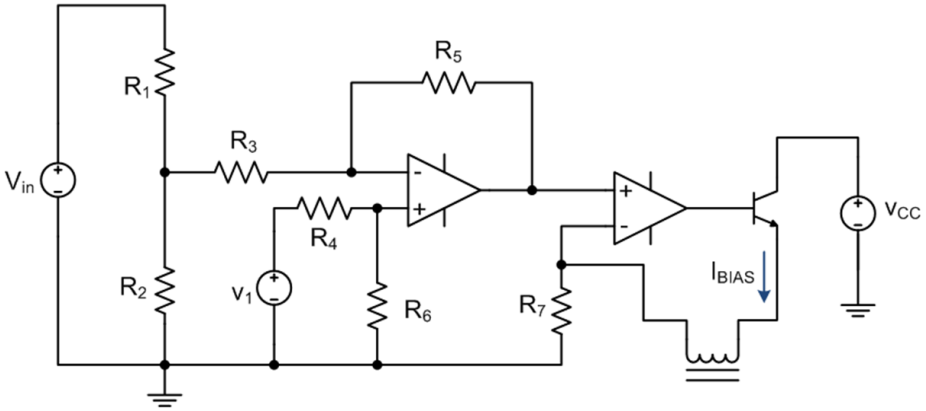


Fig. 2.7.10 - Simplified electrical scheme of transformer magnetizing inductance feed-forward control network.

The results achieved thanks to the use of this technique are shown in Fig. 2.7.11. From the primary current envelope waveform, indeed, it can be noticed that, properly varying the bias current as a function of the input voltage, the peak to peak ripple variation of the recycling current can be effectively canceled.

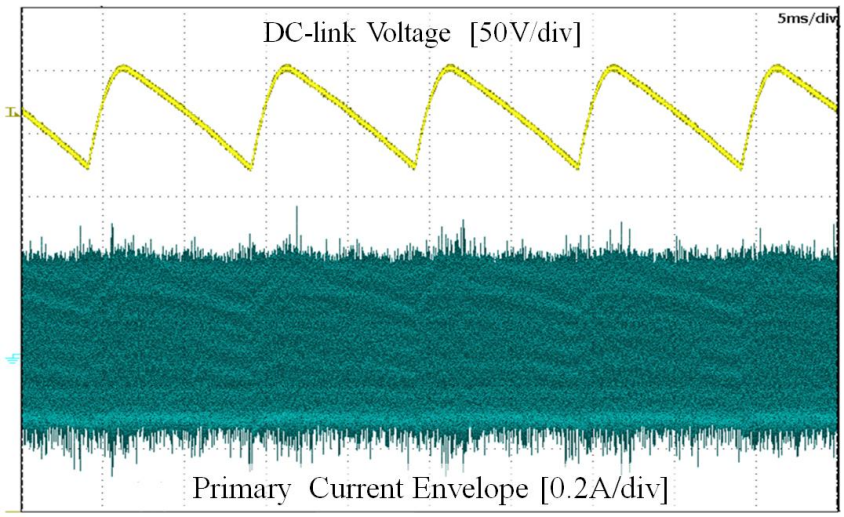


Fig. 2.7.11 - DC-link voltage and primary current envelope experimental waveforms. Timebase: 5ms/div.

The line side performance of the asymmetrical half bridge flyback converter have also been tested, in order to verify the compliance with the EN61000-3-2 standard for power equipments of power lower than 25W.

The input current waveform resulted to satisfy the current shape requirements of the standard. Indeed, as it can be noticed by observing Fig. 2.7.12, the start (θ_1) and peak angle (θ_2) are both lower than 45°, while the corresponding constraints require $\theta_1<60°$ and $\theta_2<65°$, and the end angle (θ_3) is about 100°, in accordance with the standard that requires: $\theta_3>90°$.

Moreover, the third and fifth harmonic values have also been tested, in order to check the compliance with the constraints imposed by the second version of the EN61000-3-2 standard, described in the introduction paragraph of this chapter.

The measured values resulted to be respectively equal to the 80.92% and to the 53.18% of the fundamental harmonic, in agreement with the standard requirements, that impose the third harmonic to be lower than the 86% and the fifth harmonic to be lower than the 61% of the fundamental harmonic.

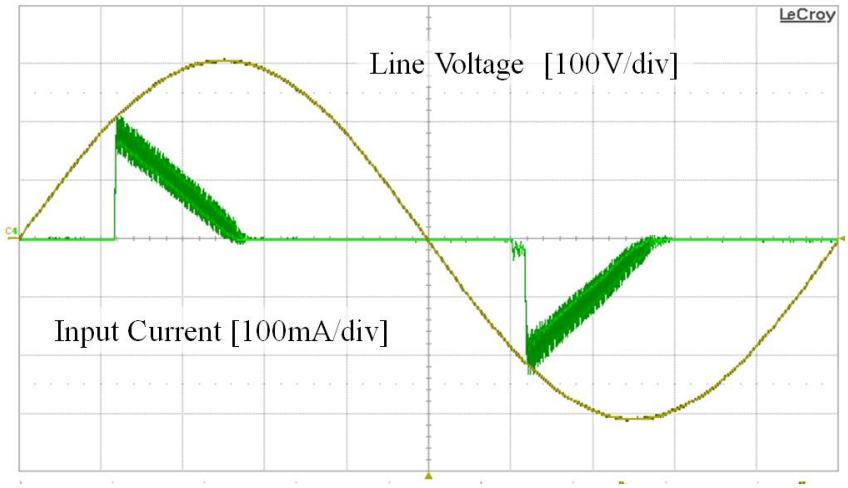


Fig. 2.7.12 - Waveform of the: (a) DC-link voltage, primary current envelope and bias current control voltage, (b) DC-link voltage and nominal load current, (c) line voltage, DC-link voltage and input line current.

Chapter 3

The Double Integrated Stage Approach

3.1 Introduction

In the previous chapter, the single stage approach to the offline LED driving issue has been designated as the most suitable solution for low power applications in which cost and volume minimization are actually the main concerns, as for example in the typical bulb replacement case.

However, as observed, the main drawbacks of this kind of solution are poor line side performance and converter suboptimum operation, calling for the implementation of optimization techniques in order to improve converter behavior. Therefore, in solid state lighting applications where compactness and cost reduction, although being important applicable requirements, are not considered the main goal, other kinds of offline driving solutions can be investigated.

In general, in order to achieve multiple functions, two or more converters can be connected in cascade. So, to fulfill solid state lighting electronic ballasts typical requirements, like guaranteeing input power factor correction, while providing galvanic isolation and tight output regulation, multiple converters, performing different tasks, could be combined.

However, despite the simplicity of such approach, it is worth keeping in mind that, especially in low power applications, to simplify converter's structure, increase power density and improve system reliability, component count reduction is desirable.
In order to achieve this goal, in recent years many novel converter topologies have been proposed in literature, based on the idea of merging converters by sharing the main switch and the whole relative control circuitry ([78]-[86]).

3.1.1. The Integration Technique

To be able to derive grafted converters, the only key requirement to be matched is to provide that the switches of the two converter units share a common node and can be operated synchronously, without altering each single converters' behavior. Switches that meet such constraints can be integrated and replaced by the corresponding grafted switch. Four different switches' common node options can be identified, as illustrated in Fig. 3.1.1, namely: the source to source and drain to drain connections, also called T-type and inverted T-type (I-T-type) configurations, respectively, and the drain to source and source to drain connections, respectively known as Π-type and inverted Π-type (I-Π-type) configurations ([87]-[89]).

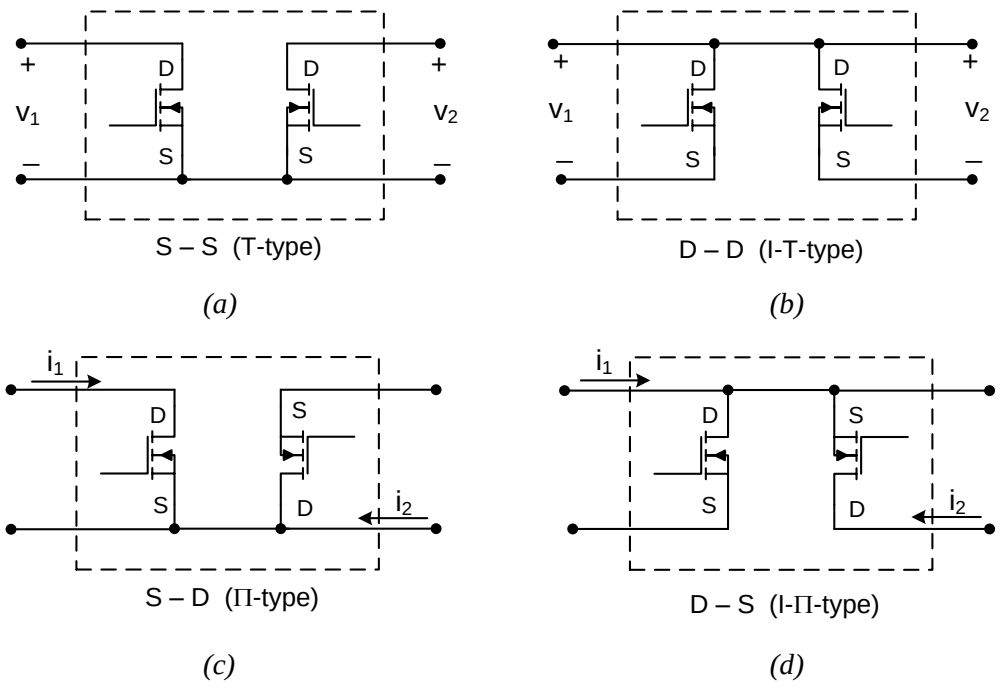


Fig. 3.1.1 - MOSFET nodes connections: a) common source, b) common drain, c) source to drain, d) drain to source.

Clearly, once the converters are integrated, interactions between the two units will occur, calling for the introduction of auxiliary diodes in order to prevent harmful interferences between the semi-stages, as shown in Fig. 3.1.2.

In particular, considering for example the case of two switches with a common source (common drain) connection combined to form a T-type (I-T-type) grafted switch TGS (I-TGS), two auxiliary diodes (D_{A1} and D_{A2} in Fig. 3.1.2 (a) and (b)) are supplemented for blocking a possible voltage difference between V_1 and V_2 during the grafted switch off state. On the other hand, as concerns Π-type (I-Π-type) grafted switch, deriving from the integration of two switches with a source to drain (drain to source) connection, such auxiliary diodes will be both no longer needed because the grafted switch only need to unidirectionally block the voltage difference and it is capable of accomplish this aim during the off-state. However, being the currents flowing through the separated switches generally not equal to each other, two auxiliary diodes (D_{A1} and D_{A2} in Fig. 3.1.2 (c) and (d)) will be in any case necessary to provide a circulating path for the current difference.
Therefore, the integration process allows to save an active switch and all its driving and control circuitry, while requiring the addition of two extra diodes. However this only in the most general case, since in many practical applications one or both diodes can be eliminated.

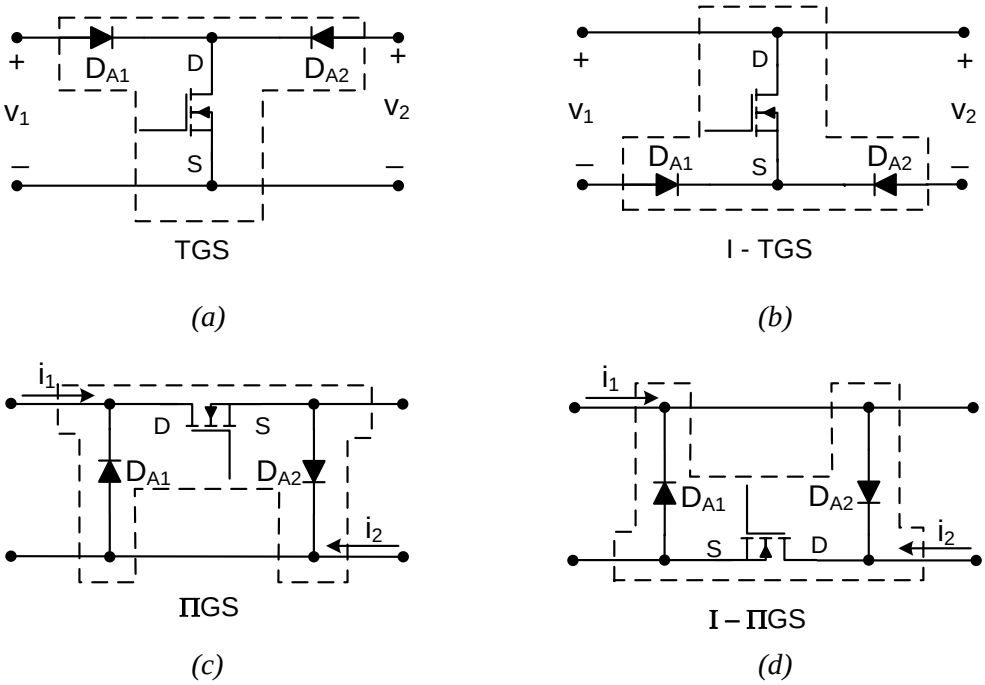


Fig. 3.1.2 - Grafted switches configurations: (a) T-type, (b) inverted T-type, (c) Π-type, (d) inverted Π-type.

For example, in Fig. 3.1.2 (a), if the voltage level V_1 is always higher than V_2, when the grafted switch is in the off state, the blocking diode D_{A1} will be always in forward biased so that it can be short-circuited. Vice versa, if V_1 is always lower than V_2, it will D_{A1} to be removed and, finally, if V_1 equals V_2 in all operating conditions, both auxiliary diodes will be no longer needed. Analogously, as concerns Π and I-Π-type grafted configurations, if current relationship can be consistently classified as $I_1>I_2$, $I_1<I_2$ or $I_1=I_2$ at all times during converter operation, one or both the auxiliary diodes could be removed and replaced with open-circuits.

According to the described integration approach, the resulting topology will be a single stage converter whose grafted switch will have to manage both the input power and the output current, in order to give the possibility of performing power factor correction and load current regulation through the input and output semi-stages, respectively.
The issues related to both these kinds of function will be carefully investigated in the following, with the aim of mitigating the effects of the pulsating input power on the LED current ripple, on load side, and to guarantee the compliance to the constraints imposed by the standards limiting the input current harmonic content on line side.

3.2 Input Stage: the PFC Issue

Since the introduction of harmonic injection and energy saving standards, like EN61000-3-2 and the Energy Star, converter input side performance have become a critical aspect in offline applications.

As formerly discussed in the previous chapter, conventional single stage switching mode power supplies, that rely on the only use of an input stage made of a line full wave voltage rectifier cascaded with a capacitive filter, can suffer high input current peaks and therefore excessive input current harmonic content.

As a result, as thoroughly explained in paragraph 2.1, the need of complying with the EN61000-3-2 standard requirements actually limits input filter capacitance maximum value, forcing the converter to manage a large input voltage ripple at twice the line frequency.

As concerns integrated topologies, the presence of two different semi-stages gives the possibility to optimize converter line side behavior, therefore improving its performance.

Before proceeding with the analysis of this issue, examining the possible approaches to this problem, it is worth to fix the fundamental notions of active, reactive and apparent power and the concept of power factor, that is commonly used as reference parameter in this regards.

To this end, let's assume the line voltage to be purely sinusoidal:

$$v_l(t) = \sqrt{2} \cdot V_{lRMS} \cdot sin(\omega_l t) \tag{3.2.1}$$

and the offline converter to behave as an equivalent linear impedance (Z_{eq}), so that also the line current results to be sinusoidal, with the same angular frequency (ω_l):

$$i_l(t) = \frac{v_l(t)}{Z_{eq}} = \sqrt{2} \cdot I_{lRMS} \cdot sin(\omega_l t - \varphi) \tag{3.2.2}$$

where $I_{lRMS}=V_{lRMS}/|Z_{eq}|$ and φ is the phase shift with respect to the line voltage

In such conditions, the instantaneous power supplied by the line will be:

$$p_l(t) = 2V_{lRMS}I_{lRMS} \cdot sen(\omega_l t) \cdot sin(\omega_l t - \varphi) = V_{lRMS}I_{lRMS} \cdot \left[cos\varphi - cos(2\omega_l t - \varphi)\right] \tag{3.2.3}$$

whose average value is called active power:

$$P = \frac{\omega_l}{\pi} \int_{\pi/\omega_l} p_l(t)\ dt = V_{lRMS}I_{lRMS} \cdot cos\varphi \tag{3.2.4}$$

and is measured in Watts [W].Now, rewriting (2.3.2) as:

$$p_l(t) = V_{lRMS} I_{lRMS} cos\varphi \cdot \left[1 - cos\left(2\omega_l t\right)\right] - V_{lRMS} I_{lRMS} sin\varphi \cdot sen\left(2\omega_l t\right) \tag{3.2.5}$$

two different components can be identified.

The first:

$$p_1(t) = V_{lRMS} I_{lRMS} \cdot cos\varphi \cdot \left[1 - cos\left(2\omega_l t\right)\right] \tag{3.2.6}$$

that is always positive, with average value equal to the active power, on one hand indicates the net energy delivered to the equivalent impedance (Z_{eq}).

The second one:

$$p_2(t) = V_{lRMS} I_{lRMS} sin\varphi \cdot sin\left(2\omega_l t\right) \tag{3.2.7}$$

on the other hand, whose amplitude:

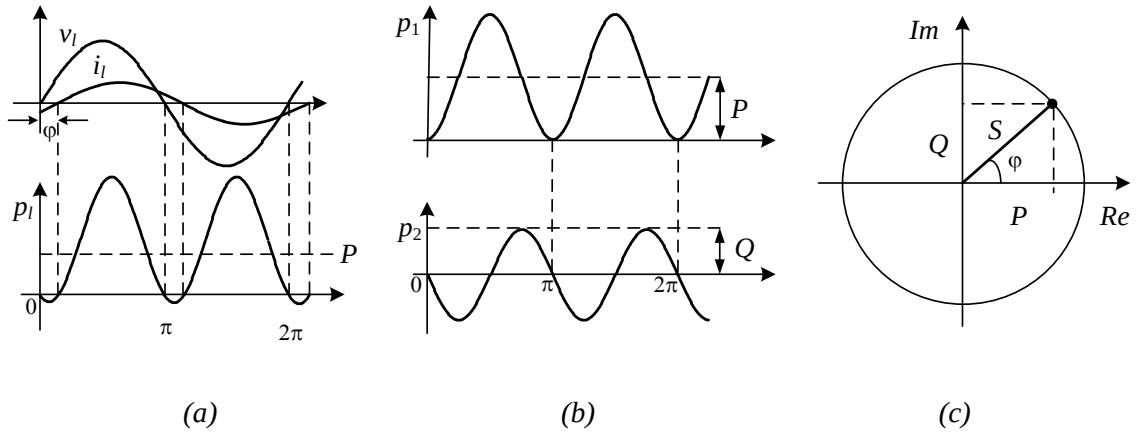
$$Q = V_{lRMS} I_{lRMS} \cdot sin\varphi \tag{3.2.8}$$

is called reactive power and is measured in reactive Volt Ampéres [VAR], accounts for the energy exchanged between such impedance and the line, with average value equal to zero.

On the basis of (3.2.4) and (3.2.8), the apparent power (S), is finally defined as the magnitude of the complex power $P+jQ$, as shown in Fig. 3.2.1:

$$S = \left|P + jQ\right| = \sqrt{P^2 + Q^2} = V_{lRMS} I_{lRMS} \tag{3.2.9}$$

and is measured in Volt Ampéres [VA].



(a) *(b)* *(c)*

Fig. 3.2.1 - (a) Line current, voltage and instantaneous power waveforms, (b) instantaneous line power components, (c)graphic representation of the relationship between active (P), reactive (Q) and apparent (S) power.

So, on the basis of such notions, the power factor can be defined as the ratio of the net power that is effectively delivered to the equivalent impedance over the whole power supplied by the line, that is as the ratio between the real and apparent power.
Therefore, under the considered assuption of linear equivalent impedance, the power factor will actually result to be equal to the cosine of the phase shift angle between the line voltage and current (cos(φ)), also called "displacement factor"

$$PF = \frac{P}{S} = \cos(\varphi) \tag{3.2.10}$$

As it can be noticed, the maximum line power transfer condition corresponds to the case of fully resistive equivalent resistance ($Z_{eq}=R_{eq}$), in which line current and voltage are in phase ($\varphi=0$), so that the power factor results to be unity.

In general, if the line results to be periodic but not purely sinusoidal, it can be written as:

$$i_l(t) = I_0 + \sum_{k=1}^{\infty} \sqrt{2} \cdot I_k \sin(k\omega_l + \gamma_k) \tag{3.2.11}$$

where I_0 is the average value, while I_k and γ_k are the RMS value and the phase of each different harmonic.
Now, being the current harmonic at the line frequency the only one that actually contributes to the transfer of active power, the power factor will be given by:

$$PF = \frac{V_1 \cdot I_1 \cdot \cos(\Phi)}{V_{lRMS} \cdot I_{lRMS}} = \frac{I_1}{I_{lRMS}} \cdot \cos(\Phi) = \frac{I_1}{\sqrt{I_1^{\,2} + \sum_{k=2}^{\infty} i_k^{\,2}}} \cdot \cos(\Phi) \tag{3.2.12}$$

where the assumption of purely sinusoidal line voltage ($V_{lRMS}=V_1$) has been exploited.

From the considerations made so far it can be easily inferred that, in order to improve the efficiency of the energy distribution system, it is worth to minimize the line injected current harmonic content and maximize power factor. Although not doing any effective work, indeed, the current associated with reactive power actually results in energy waste and calls for an oversize of utility grid components.

A lot of solutions have been proposed in literature, in order to improve line side converters' behavior and get high PF values, by performing input current shaping, through the use of a dedicated power factor correction stage (PFC).
Some of these involve the use of switching converters operated in discontinuous conduction mode under constant duty cycle and switching frequency in order to provide an

"automatic" power factor correction, as shown in [90]-[92]. Others, are converters operated at the boundary between continuous and discontinuous conduction mode with variable switching frequency and constant on time, as in [93]-[96]. Others use continuous conduction mode operated converters with constant switching frequency and variable duty cycle, forcing sinusoidal input current waveforms by using an analog multiplier, as in [97]-[99].

Despite the many differences between the possible applicable strategies, however, two main ways of addressing the problem can be identified, that will be briefly summarized here in the following.

3.2.1 Ideal Power Factor Correctors

In particular, the first kind of approach relies on the use of an "ideal" power factor correction input stage, that can be implemented by means of buck-boost based topologies. These are operated so as to emulate, from line perspective, an equivalent purely resistive load (R_{eq}), resulting in a sinusoidal input current waveform, as shown in Fig. 3.2.2.

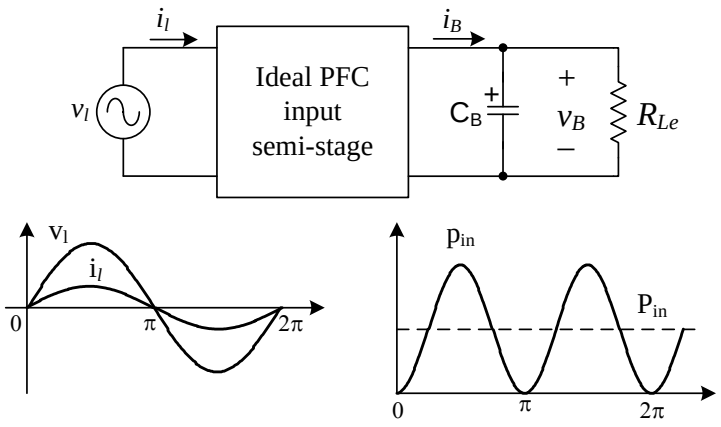


Fig. 3.2.2 - Use of an "ideal" PFC input semi-stage in an integrated topology for offline driving of solid state light sources.

In such conditions, the power absorbed at converter input, averaged over converter switching period, will be:

$$p_{in}(t) = \frac{v_l^{\,2}(t)}{R_{eq}} = \frac{2V_{lRMS}^2 sin^2(\omega_l t)}{R_{eq}} = \frac{V_{lRMS}^2}{R_{eq}}\left[1 - cos(2\omega_l t)\right] \tag{3.2.13}$$

whose mean value is:

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} p_{in}(\theta)d\theta = \frac{1}{\pi}\frac{V_{lRMS}^2}{R_{eq}}\int_0^{\pi}\left[1 - cos(2\theta)\right]\,d\theta = \frac{V_{lRMS}^2}{R_{eq}} \tag{3.2.14}$$

where $\theta=\omega_l t$.

Assuming ideal non dissipative operation of the input semi-stage, being the ideal PFC devoid of any low frequency energy storage element, the power delivered to BUS capacitor (C_B in Fig. 3.2.2) will be equal to the input power.

Therefore, if BUS capacitor voltage ripple is negligible compared to the average value, the expression of the PFC semi-stage output current (i_B) can be written as follows:

$$i_B(t) \simeq \frac{p_B(t)}{V_B} = \frac{p_{in}(t)}{V_B} = \frac{V_{lRMS}^2}{V_B R_{eq}}(1-cos2\omega_l t) \tag{3.2.15}$$

where it can be noticed the presence of both a DC and an AC component with the same amplitude:

$$I_B = \hat{I}_B = \frac{V_{lRMS}^2}{V_B R_{eq}} \tag{3.2.16}$$

Keeping in mind (3.2.13) and (3.2.15), the averaged model of an ideal PFC stage can therefore easily be implemented, as reported in Fig. 3.2.3.

To emulate converter behavior, the equivalent resistance (R_{eq}) current is sensed and multiplied by the rectified line voltage in order to get the instantaneous input power (p_{in}). The obtained value is then divided by the PFC output voltage (v_B), in order to get a reference signal for the controlled current source that generates the current (i_B), feeding the BUS capacitor and the equivalent input resistance of the downstream placed DC/DC conversion semi-stage. This simple averaged model can be used to perform fast simulations and derive the waveforms describing the evolution of the main input semi-stage variable quantities within the line period, neglecting the high frequency harmonics related to converter switching process.

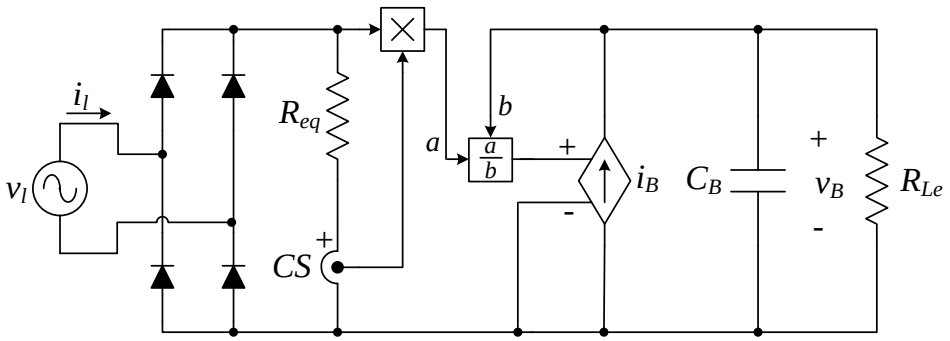


Fig. 3.2.3 - Averaged model of an ideal input PFC stage.

3.2.2 Quasi Power Factor Correctors

The other way of addressing the power factor correction issue, relies on the use of a "quasi" PFC input stage, implemented through the use of a step-down topology.
Although unable of providing unity power factor, such kind of solution is capable of significantly improving line side converter performance.
If properly controlled, indeed, quasi PFC can be operated so as to behave, from line perspective, as an equivalent resistance (R'_{eq}) series connected with a constant BUS voltage source. However, this can be done only during a given conduction interval [θ_1, π-θ_1], within the line angular half period, in which the line voltage results to be greater or equal than the voltage level of the BUS.
In the remaining parts of the angular half period, called "dead angles", namely [0, θ_1] and [θ_1, π], the PFC semi-stage will be switched-off and the input current will be zero, as illustrated in Fig. 3.2.4.

In particular, during the previously mentioned conduction interval, the expression of the input current, averaged over the switching period, will be:

$$i_l(t) = \frac{v_l(t) - V_B}{\mathrm{R'}_{eq}} = \frac{\sqrt{2} \cdot V_{lRMS} \sin(\omega_l t) - V_B}{\mathrm{R'}_{eq}} \tag{3.2.17}$$

where BUS voltage ripple has been neglected.

So, being the average output voltage of such an input stage equal to:

$$V_B = \sqrt{2} \cdot V_{lRMS} \cdot \sin(\theta_1) \tag{3.2.18}$$

the expressions of the instantaneous input power, averaged over converter switching period, will be:

$$p_{in}(t) = v_l(t) \cdot i_l(t) = \begin{cases} \dfrac{2V_{lRMS}^2}{\mathrm{R'}_{eq}} sin^2(\omega_l t) - \dfrac{2V_{lRMS}^2}{\mathrm{R'}_{eq}} \cdot \sin(\theta_1) sin(\omega_l t), & \text{if } \dfrac{\theta_1}{\omega_l} < \mathrm{t} < \dfrac{\pi\text{-}\theta_1}{\omega_l} \\ 0, & \text{elsewhere} \end{cases} \tag{3.2.19}$$

whose mean value results:

$$P_{in} = \frac{1}{\pi}\int_0^{\pi} p_{in}(\theta) d\theta = \frac{1}{\pi}\frac{2V_{lRMS}^2}{\mathrm{R'}_{eq}} \int_{\theta_1}^{\pi-\theta_1} \left[sin^2(\theta) - sin(\theta_1) sin(\theta) \right] d\theta = \frac{V_{lRMS}^2}{\mathrm{R'}_{eq}} \left(1 - \frac{2\theta_1}{\pi} - \frac{\sin(2\theta_1)}{\pi} \right) \tag{3.2.20}$$

Under the same unity efficiency assumption, previously considered for ideal PFC case, the output current will be:

$$\begin{cases} i_B(t) = \dfrac{p_B(t)}{V_B} = \dfrac{p_{in}(t)}{V_B} = \dfrac{V_{lRMS}}{\mathrm{R'}_{eq}} \cdot \dfrac{1-\cos(2\omega_l t)}{\sqrt{2}\cdot\sin(\theta_1)} - \dfrac{\sqrt{2}\cdot V_{lRMS}}{\mathrm{R'}_{eq}} sin(\omega_l t), & \text{if } \dfrac{\theta_1}{\omega_l} < \mathrm{t} < \dfrac{\pi\text{-}\theta_1}{\omega_l} \\ i_B(t) = 0, & \text{elsewhere} \end{cases}$$

(3.2.21)

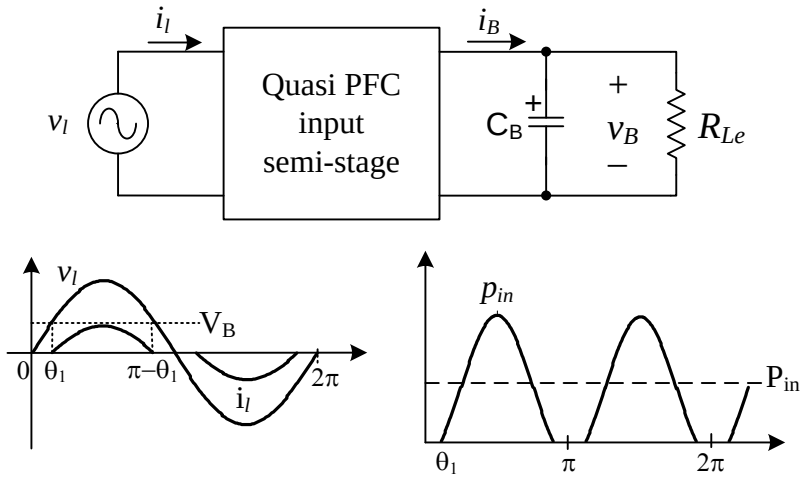


Fig. 3.2.4 - Use of a "quasi" PFC input semi-stage in an integrated topology for offline driving of solid state light sources.

Following a procedure similar to that previously used for the ideal PFC stage case, the averaged electrical model of a quasi-PFC stage, capable of simulating its behavior, providing the waveforms of converter variables averaged over the switching period, can be derived. As shown in Fig. 3.2.5, the model is made of the equivalent resistance (R'_{eq}), a voltage-controlled voltage source that replicates the instantaneous output (BUS) voltage and a controlled current source that generates the output BUS current (i_B) on the basis of the input current reference signal provided by a sensor.

It is worth noting that, despite in the analysis performed the BUS voltage ripple has been neglected when calculating the output current, the averaged circuits presented in Fig. 3.2.3 and Fig. 3.2.5 will suits even in case of large BUS voltage ripple amplitudes.

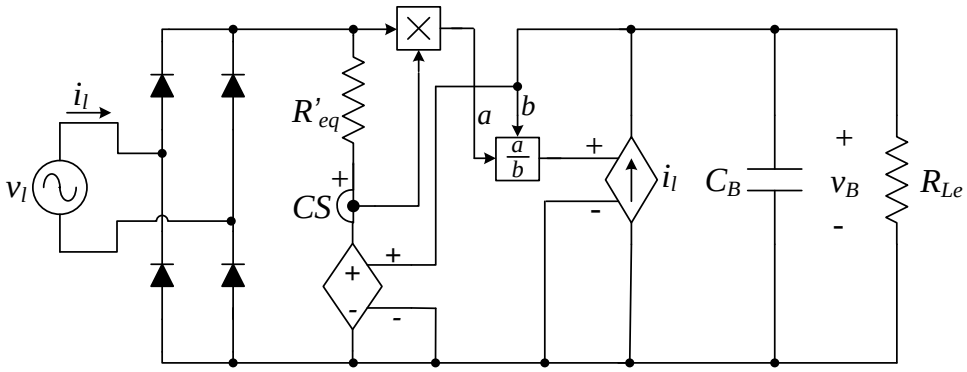


Fig. 3.2.5 - Averaged model of a quasi-PFC input stage.

3.3 Output Stage: the Load Current Ripple Reduction Issue

Once clarified the main issues regarding line side converter behavior, it is now worth to make some considerations about the output DC/DC conversion stage. Depending on the specific requirements of each different application, the most disparate topologies, can be used to implement the output semi-stage. However, despite the many various aspects that could be taken into account, it is worth to focus on a particular feature that can be considered a common requirement in all solid state lighting driving applications of the integrated topologies.

This is the capability to reduce the effects on load current of the BUS voltage ripple, due to the input line power pulsation at twice the line frequency.

As already observed, since the previously described PFC semi-stage has no low frequency energy storage elements, assuming ideal lossless converter operation, the input power will be completely transferred to the BUS capacitor.

In a typical application, the AC component of the BUS current (i_B) computed in (3.2.15) and (3.2.21) will almost entirely flow through the BUS capacitor equivalent reactance, so that the PFC stage output voltage will be characterized by both a DC and an AC component:

$$v_B(t) = V_B + \hat{v}_B(t) \tag{3.3.1}$$

where $\hat{v}_B(t)$ accounts for the only twice the line frequency oscillation, being the switching frequency component of the BUS voltage ripple neglected.

From the total amount of charge injected by the AC current in the BUS capacitor:

$$\Delta Q_B = \begin{cases} \dfrac{1}{\omega_l}\displaystyle\int_{\pi/4}^{3\pi/4} \left[i_B(\theta) - I_B \right] d\theta \,, & \text{with an ideal PFC stage} \\ \dfrac{1}{2\omega_l}\displaystyle\int_{0}^{\pi} \left| i_B(\theta) - I_B \right| d\theta \,, & \text{with a Quasi-PFC stage} \end{cases} \tag{3.3.2}$$

the peak amplitude ($\hat{V}_B$) of such voltage ripple can be expressed as:

$$\hat{V}_B = \frac{\Delta Q_B}{C_B} = \frac{V_{lRMS}^2}{4\pi f_L V_B R_{eq} C_B} \tag{3.3.3}$$

in the case of an ideal PFC stage, or as:

$$\hat{V}_B = \frac{\Delta Q_B}{2C_B} = \frac{V_{IRMS}^2}{8\pi f_L V_B R_{eq} C_B}\left\{2\theta_1 \cdot \left(1 - \frac{2\theta_1}{\pi} - \frac{\sin(2\theta_1)}{\pi}\right) + \int_{\theta_1}^{\pi-\theta_1}\left[1 - \cos(2\omega_l t) - 2\sin(\theta_1)\sin(\omega_l t)\right]d\theta\right\} \tag{3.3.4}$$

if, instead, a quasi-PFC is used to implement the input stage.

In general, in standard two stage configurations, the load voltage ripple can be minimized by compensating the alternate BUS voltage component through a proper regulation of the output stage converter duty-cycle or switching frequency.
However, in an integrated topology, such parameters will be clearly already constrained by input power factor correction requirements, so that, any duty ratio or frequency modulation within the line half period, aimed at regulating the load current, will result in line current distortion, actually affecting line side converter performance.

As a result, if not otherwise compensated, the twice the line frequency BUS voltage ripple will be transferred to the load, whose voltage will be therefore, as illustrated in Fig. 3.3.1, also composed by both a constant and an alternate component:

$$v_O(t) = V_O + \hat{v}_O(t) \tag{3.3.5}$$

where once again the switching frequency component of the ripple is neglected.

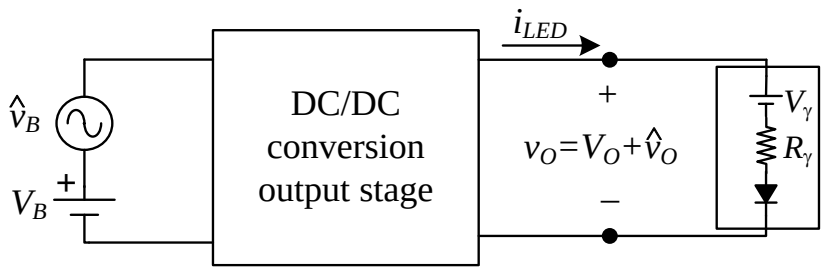


Fig. 3.3.1 - Simplified scheme of the DC/DC conversion output semi-stage.

It is therefore easy to understand that, being the minimization of the LED current peak to peak ripple amplitude a major concern in solid state lighting applications, the BUS voltage ripple attenuation performed by the output semi-stage actually results to be a key feature of integrated topologies.
In order to effectively address this issue, the relation between the BUS and output voltage ripple should be therefore carefully investigated.

In this regard, it should be noticed that, in general, in order to avoid an excessively slow response, the poles dominating the dynamics of such output power conversion stage, are usually at frequencies well above the twice the line frequency.

So, as long as the switching frequency ripple is neglected, the relation between the input and output voltages of the output stage can be studied by considering the static relation between such variables.

The output voltage can be, therefore, expressed as follows:

$$v_O(t) = M\left(v_B(t)\right) \tag{3.3.6}$$

where M is a function representing the static relationship between the BUS and the output voltage.

Therefore the voltage ripple transformation factor (ν), that is the ratio between the peak amplitudes of the output ($\hat{V}_O$) and of the BUS ($\hat{V}_B$) voltage ripple, can be easily obtained by taking the partial derivative on (3.3.6):

$$\nu = \frac{\hat{V}_O}{\hat{V}_B} \simeq \frac{\partial M\left(v_B(t)\right)}{\partial v_B} \tag{3.3.7}$$

So, being in solid state lighting applications the typical relationship between the load voltage and current given by:

$$v_O(t) = V_\gamma + R_\gamma i_{LED}(t) \tag{3.3.8}$$

(where V_γ is the threshold voltage and R_γ is the series resistance of the lamp) the LED current ripple peak amplitude ($\hat{I}_{LED}$), namely the parameter of interest in this kinds of applications, can be written as follows:

$$\hat{I}_{LED} = \frac{\hat{V}_O}{R_\gamma} = \nu \frac{\hat{V}_B}{R_\gamma} \tag{3.3.9}$$

By observing (3.3.9) it can be inferred that three different kinds of approach can be considered in order to address the LED current ripple minimization issue.

The first one is based on the reduction of BUS voltage ripple, the second one relies on the use of a suitable output semi-stage topology capable of guaranteeing a high voltage ripple attenuation, while the last one involves the choice of high series resistance LED lamps.

Keeping in mind (3.3.3) and (3.3.4), as concerns the first kind of solution it can be noticed that the higher are the BUS voltage and capacitance values, the lower will be the bus voltage ripple.

However, this will turn into increased voltage stress on the semiconductors and will imply the use of low lifetime electrolytic capacitors, affecting the overall converter efficiency and reliability.

Then, with regard to the third way of approaching the problem, it can be observed that, once fixed the load characteristics according to the specific application considered, the lamp resistance will be already determined, therefore resulting to be a parameter of difficult manipulation.

Nevertheless, a simple hint that can be taken into account is that, given the output power, luminous flux, color temperature, color rendering index, and all the other application requirements the use of a lamp made of long series LED strings instead of many short paralleled strings would be of benefit from this perspective, being the resulting series resistance much higher.

Finally, the effectiveness of the remaining option, that refers to the capability of the output semi-stage of providing high voltage ripple attenuation, will depend on the ripple transformation factor characterizing the specific topology that is selected to implement the stage.

Some reference examples, in this regards, will be given in the following paragraph, that provides a generalized analysis of some of the typical integrated topologies, proposed so far in literature, for solid state lighting applications.

3.4 Integrated Topologies for Solid State Lighting Applications: a General Design Approach

In paragraphs 3.2 and 3.3 the issues related with the input PFC and the output DC/DC conversion stages were analyzed separately. However, as previously explained, in integrated topologies such stages are merged in order to get compact offline converters.
Indeed, exploiting the grafting technique presented in paragraph 3.1, the two stages can be conveniently adjusted so as to share the same active switch, giving the possibility to actually save one power switch and its whole control and driving circuitry.
This enables a significant ballast miniaturization, cost reduction and reliability improvement, with respect to standard multi-stage solutions, while enhancing line side behavior, if compared to classical single stage topologies.
All such characteristics make the integrated approach, whose general simplified scheme is reported in Fig. 3.4.1, particularly attractive in cost-effective solid state lighting applications that require high reliability and good line side performance levels, even if at cost of a slower and less accurate LED lamp current control.

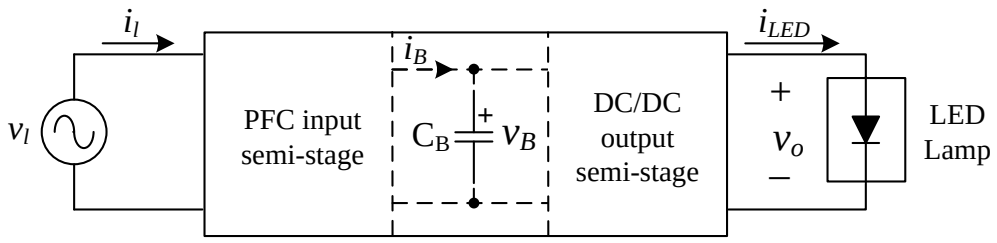
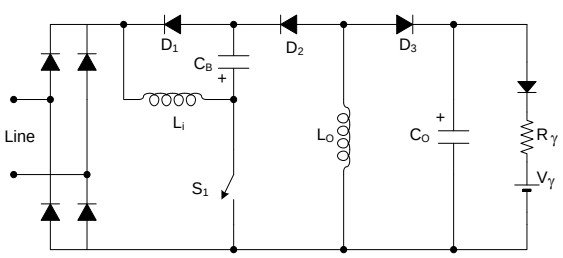
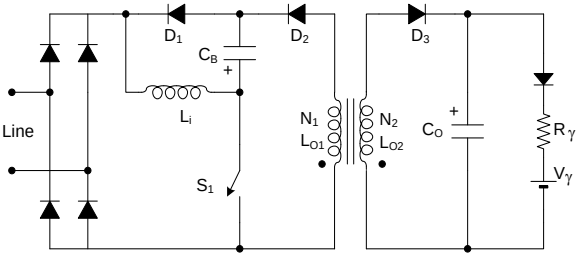


Fig. 3.4.1 - Simplified scheme of the typical offline LED integrated driver.

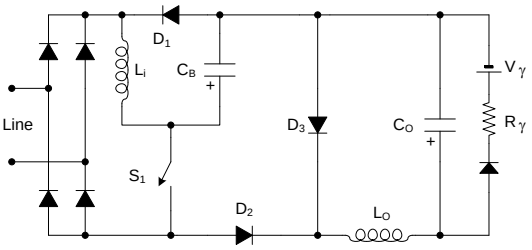
Some of the major solutions, proposed in literature (e.g. [100]-[107]) to meet the offline supply requirements of lighting applications, are reported in Fig. 3.4.2.
As it can be easily guessed, depending on the specific topologies selected for the implementation of the input and output stages, the actual characteristics of the integrated converter obtained will significantly vary. However, regardless of the specific features of each integrated topology, a general analysis and design procedure can be outlined, as presented here in the following. It is worth to mention that, while the input semi-stage is assumed to perform power factor correction operating in discontinuous conduction mode, both continuous (CCM) and discontinuous (DCM) conduction mode will be taken into account as concern the operation of the output stage.



Buck-Boost/Buck-Boost



Buck-Boost/Flyback



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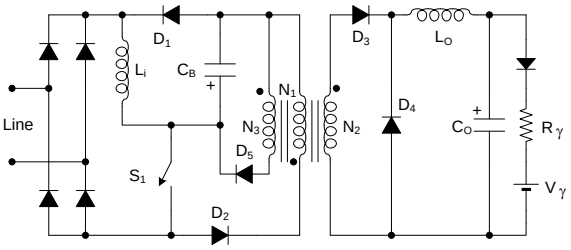
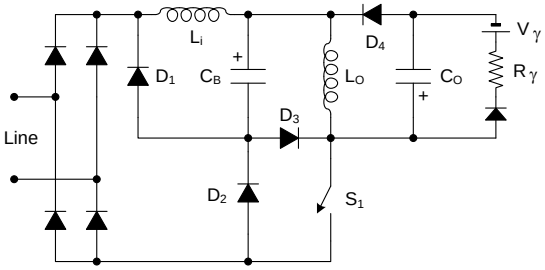
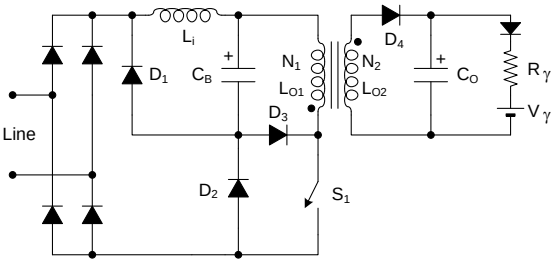


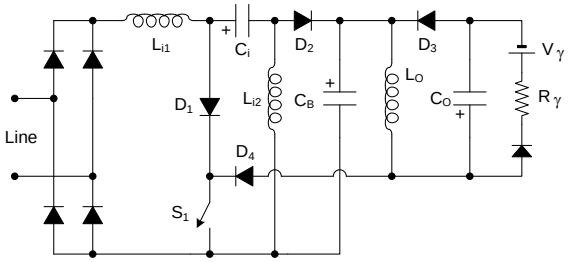
Buck-Boost/Forward



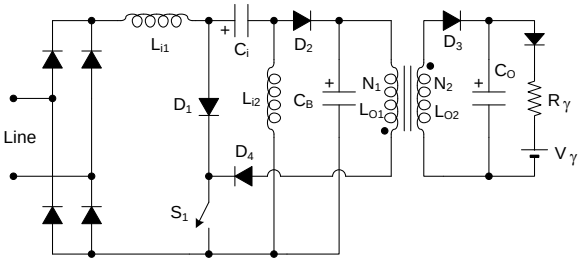
Buck/Buck-Boost



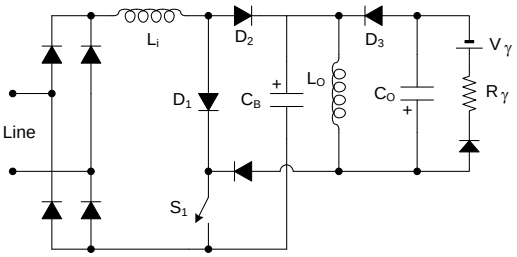
Buck/Flyback



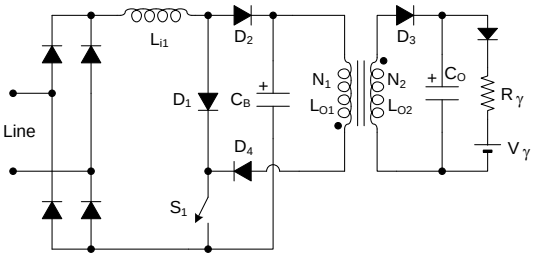
SEPIC/Buck-Boost



SEPIC/Flyback



Boost/Buck-Boost



Boost/Flyback

Fig. 3.4.2 - Typical integrated topologies proposed in literature for solid state lighting applications.

To begin with, the first step is to compute the average load voltage, on the basis of the known load parameters, namely: the threshold voltage (V_γ), the series resistance (R_γ) and the average current (I_{LED}) of the LED lamp:

$$V_O = V_\gamma + R_\gamma I_{LED} \tag{3.4.1}$$

Now, under the assumption of small load current ripple, that allows to approximate LED RMS current with the average value, converter average load power (P_O) can be computed as:

$$P_O = V_O \cdot I_{LED} \tag{3.4.2}$$

So, if overall converter efficiency is assumed to be ideally unity, the power that has to be managed by both converter semi-stages will be:

$$P_{in} = P_B = P_O = R_\gamma I_{LED}{}^2 + I_{LED} V_\gamma \tag{3.4.3}$$

where P_{in} and P_B refer to the average input power of the PFC and of the output semi-stage, respectively.

Another relevant parameter for converter design is the average value of the BUS voltage (V_B), at the interface between the input and the output semi-stages.

As explained above, indeed, when dealing with quasi-PFC input stages, this voltage level is actually a key factor in order to meet the power factor requirements, being the dead angle:

$$\theta_1 = \sin^{-1}\left(\frac{V_B}{\sqrt{2}V_{IRMS}}\right) \tag{3.4.4}$$

responsible for input current distortion.

Nevertheless, also for solutions based on the use of an ideal power factor correction input stage the design of such parameter will not be a minor aspect, since it determines the voltage stress and current levels on PFC converter semiconductor devices.

Once a proper BUS voltage has been determined, the value of another parameter, that will turn out to be useful in the continuation of the design procedure, can be computed; namely the equivalent input resistance (R_B) of the output DC/DC conversion stage operated in DCM. Knowing the power (P_B) processed by the output stage, and its input and output average voltages (V_B and V_O, respectively) such parameter can be indeed easily derived, under the assumption of negligible voltage ripple. As reference, the expressions given in the first column of Table 3.4.1, related to the output stages of the topologies of Fig. 3.4.2, can be considered.

On the basis of all the information derived so far, converter duty cycle (D) and, if necessary, transformer turns ratio (n) can now be computed.

Indeed, knowing the value of the required output stage voltage conversion ratio:

$$M_{out} = V_O / V_B \tag{3.4.5}$$

from the expression describing such parameter in the corresponding output semi-stage conduction mode (see Table 3.4.2, as reference for the topologies shown in Fig. 3.4.2), the desired quantities can be derived.

Note that, if input stage conduction mode conditions (Table 3.4.3), turn out to be not satisfied for the values of the computed quantities, another suitable BUS voltage level should be selected and the duty cycle and turns ratio should be recalculated.

TABLE 3.4.1 - AVERAGE INPUT POWER
EQUIVALENT INPUT RESISTANCE AND OF THE OUTPUT STAGE

DC/DC STAGE TOPOLOGY	AVERAGE OUTPUT STAGE INPUT POWER P_B (DCM OPERATION)	EQUIVALENT INPUT RESISTANCE R_B (DCM OPERATION)
Buck	$(V_B^2 - V_B V_o) / R_B$	$2 f_{sw} L_O / D^2$
Forward	$(V_B^2 - V_B V_o / n) / R_B$	$2 f_{sw} L_O / (nD)^2$
Buck-Boost	V_B^2 / R_B	$2 f_{sw} L_O / D^2$
Flyback	V_B^2 / R_B	$2 f_{sw} L_{O1} / D^2$
$n = N_2 / N_1$		

TABLE 3.4.2 - VOLTAGE CONVERSION RATIO EXPRESSIONS

DC/DC STAGE TOPOLOGY	$V_O = M(V_B)$	
	CCM	DCM
Buck	DV_B	$\frac{1}{2}V_\gamma - \frac{1}{2}\frac{(V_B R_\gamma)}{R_B} + \frac{1}{2}\sqrt{\left(V_\gamma - \frac{V_B R_\gamma}{R_B}\right)^2 + \frac{4V_B^2 R_\gamma}{R_B}}$
Forward	nDV_B	$\frac{1}{2}V_\gamma - \frac{1}{2}\frac{nV_B R_\gamma}{R_B} + \frac{1}{2}\sqrt{\left(V_\gamma - \frac{nV_B R_\gamma}{R_B}\right)^2 + \frac{4n^2 V_B^2 R_\gamma}{R_B}}$
Buck-Boost	$\frac{D}{1-D}V_B$	$\frac{1}{2}V_\gamma + \frac{1}{2}\sqrt{V_\gamma^2 + \frac{4V_B^2 R_\gamma}{R_B}}$
Flyback	$\frac{nD}{1-D}V_B$	$\frac{1}{2}V_\gamma + \frac{1}{2}\sqrt{V_\gamma^2 + \frac{4V_B^2 R_\gamma}{R_B}}$

TABLE 3.4.3 - DUTY CYCLE RANGES FOR DIFFERENT OPERATION MODES

INTEGRATEDCONVERTER	OPERATION MODE (INPUT STAGE-OUTPUT STAGE)	
	DCM-CCM	DCM-DCM
Buck-Boost/ Buck-Boost	$D<1/(1+V_l/V_B)$ $D=1/(1+V_B/V_O)$	$D<1/(1+V_l/V_B)$ $D<1/(1+V_B/V_O)$
Buck-Boost/ Flyback	$D<1/(1+V_l/V_B)$ $D=1/(1+nV_B/V_O)$	$D<1/(1+V_l/V_B)$ $D<1/(1+nV_B/V_O)$
Buck-Boost/ Buck	$D<1/(1+V_l/V_B)$ $D=V_O/V_B$	$D<1/(1+V_l/V_B)$ $D<V_O/V_B$
Buck-Boost/ Forward	$D<1/(1+V_l/V_B)$ $D=V_O/nV_B$	$D<1/(1+V_l/V_B)$ $D<V_O/nV_B$
Buck/ Buck-Boost	$D<V_B/V_l$ $D=1/(1+V_B/V_O)$	$D<V_B/V_l$ $D<1/(1+V_B/V_O)$
Buck/ Flyback	$D<V_B/V_l$ $D=1/(1+nV_B/V_O)$	$D<V_B/V_l$ $D<1/(1+nV_B/V_O)$
SEPIC/ Buck-Boost	$D<1/(1+V_l/V_B)$ $D=1/(1+V_B/V_O)$	$D<1/(1+V_l/V_B)$ $D<1/(1+V_B/V_O)$
SEPIC/ Flyback	$D<1/(1+V_l/V_B)$ $D=1/(1+nV_B/V_O)$	$D<1/(1+V_l/V_B)$ $D=1/(1+nV_B/V_O)$
Boost/ Buck-Boost	$D<1-V_l/V_B$ $D=1/(1+V_B/V_O)$	$D<1-V_l/V_B$ $D<1/(1+V_B/V_O)$
Boost/ Flyback	$D<1-V_l/V_B$ $D=1/(1+nV_B/V_O)$	$D<1-V_l/V_B$ $D<1/(1+nV_B/V_O)$
	$V_l=\sqrt{2}\cdot V_{lRMS}$	

Now, keeping in mind the expression of the average input power of a quasi PFC, previously derived in (3.2.20), the value of the input resistance of converter input semi-stage can be derived as:

$$R'_{eq}=\frac{{V_{lRMS}}^2}{P_{in}}\left[1-\frac{2\theta_1}{\pi}-\frac{\sin(2\theta_1)}{\pi}\right] \tag{3.4.6}$$

As it can be noticed, the ideal PFC case (R_{eq}) can also be easily included by simply setting the dead angle (θ_1) to zero, keeping in mind the different meaning of such parameter in the two different cases (as evidenced also by the models reported in Fig. 3.2.3 and Fig. 3.2.5).

So, once the input equivalent resistance have been computed according to (3.4.6), knowing the relationship between such parameter and the input stage inductor (see for example the expressions reported in Table 3.4.4, referred to the PFC stages of Fig. 3.4.2), the value of the latter can be derived.

As concerns the output stage inductor, it can be computed so as to guarantee continuous conduction, if this is the required operation mode.

Otherwise, if the output stage is supposed to operate in discontinuous mode, given the amount of power processed by this stage (P_B), the inductor value can be easily derived from the expression (e.g. those listed in the second column of Table 3.4.1) of the output stage input resistor (R_B), whose value has been already computed.

TABLE 3.4.4 - EQUIVALENT INPUT RESISTANCE OF PFC STAGES OPERATED IN DCM

PFC STAGE	EQUIVALENT INPUT RESISTANCE R_{eq}	CONDITIONS/DEFINITIONS
Buck	$2L_i f_s / D^2$	$\theta_1 \le \omega t \le \pi - \theta_1$
Boost	$2L_i f_s / D^2$	$V_B \gg V_l$
Buck-Boost	$2L_i f_s / D^2$	---
SEPIC	$2L_e f_s / D^2$	$L_e = L_{i1}L_{i2} / (L_{i1} + L_{i2})$

Finally, as concerns LED load current requirements, the specifications limiting its switching frequency ripple can be complied by properly selecting the output filter capacitor, while, those regarding the twice the line frequency ripple, will actually constrain the BUS capacitance design.

In particular, knowing the maximum LED current ripple ($\hat{I}_{LED}$) that is allowed, the amplitude of the maximum BUS voltage ripple can be computed from (3.3.9), which involves the knowledge of the ripple transformation factor (ν), defined in (3.3.7), corresponding to the topology used to implement the output stage.

So, once the maximum voltage ripple has been computed, the value of the required BUS voltage capacitance can be finally derived by solving for C_B one of the equations reported in (3.3.3) and (3.3.4), depending on whether an "ideal" or a "quasi" power factor corrector is used to implement converter input semi-stage.

As previously discussed in paragraph 3.3, the ripple transformation factor (ν) is actually a key parameter to allow BUS capacitor optimization in integrated topologies. Therefore, for

sake of clearness, an example showing the computation of such factor, in the case of a buck converter operated in DCM, is reported here in the following, for reader convenience. First of all, the well known expression of the voltage conversion ratio of the buck converter in DCM:

$$M_{DCM} = \frac{V_O}{V_B} = \frac{1}{1 + \frac{2 f_{sw} L_O}{D^2 V_B} \cdot I_{LED}} = \frac{1}{1 + \frac{R_B}{V_B} \cdot I_{LED}} \tag{3.4.7}$$

can be rewritten according to (3.4.1), to take into account the features of the LED load:

$$M_{DCM} = \frac{V_O}{V_B} = \frac{1}{1 + \frac{R_B}{R_\gamma}\left(\frac{V_O}{V_B} - \frac{V_\gamma}{V_B}\right)} = \frac{1}{1 + \frac{R_B}{R_\gamma}\left(M_{DCM} - \frac{V_\gamma}{V_B}\right)} \tag{3.4.8}$$

This actually results into a second order equation in the variable M_{DCM}, whose solution is:

$$M_{DCM} = \frac{V_O}{V_B} = \frac{1}{2}\left[\frac{V_\gamma}{V_B} - \frac{R_\gamma}{R_B} + \sqrt{\left(\frac{V_\gamma}{V_B} - \frac{R_\gamma}{R_B}\right)^2 + 4\frac{R_\gamma}{R_B}}\right] \tag{3.4.9}$$

From such expression, the output voltage can be therefore written as:

$$V_O = M_{DCM} \cdot V_B = \frac{1}{2}\left[V_\gamma - \frac{R_\gamma}{R_B}V_B + \sqrt{\left(V_\gamma - \frac{R_\gamma}{R_B}V_B\right)^2 + 4\frac{R_\gamma}{R_B}V_B^2}\right] \tag{3.4.10}$$

so that the desired ripple transformation factor can be finally computed, according to the definition reported in (3.3.7):

$$\nu = \frac{\partial V_O}{\partial V_B} = -\frac{1}{2}\frac{R_\gamma}{R_B} + \frac{1}{4} \cdot \frac{-2\frac{R_\gamma}{R_B}\left(V_\gamma - \frac{R_\gamma}{R_B}V_B\right) + \frac{R_\gamma}{R_B}V_B}{\sqrt{\left(V_\gamma - \frac{R_\gamma}{R_B}V_B\right)^2 + 4\frac{R_\gamma}{R_B}V_B^2}} = -\frac{\Gamma}{2} + \frac{1}{4} \cdot \frac{V_B\left(2\Gamma^2 + 8\Gamma\right) - 2V_\gamma\Gamma}{2V_O + V_B\Gamma - V_\gamma} \tag{3.4.11}$$

where the adimensional parameter Γ has been defined as $\Gamma = R_\gamma / R_B$.

In a very similar way, the expression of the ripple transformation factor can be derived also for the other converters of Fig. 3.4.2, the outcomes are listed in Table 3.4.5.

TABLE 3.4.5 - VOLTAGE RIPPLE TRANSFORMATION FACTOR

DC/DC STAGE TOPOLOGY	$\nu = \partial M\left(v_B\right)/\partial v_B$	
	CCM	DCM
Buck	D	$-\frac{\Gamma}{2}+\frac{1}{4}\cdot\frac{V_B\left(2\Gamma^2+8\Gamma\right)-2V_\gamma\Gamma}{2V_O+V_B\Gamma-V_\gamma}$
Forward	nD	$-\frac{\Gamma}{2}+\frac{n}{4}\cdot\frac{V_B\left(2\Gamma^2+8\Gamma\right)-2V_\gamma\Gamma}{2V_O+V_B\Gamma-V_\gamma}$
Buck-Boost	$\frac{D}{1-D}$	$\frac{2V_BR_\gamma}{\left(2V_O-V_\gamma\right)R_B}$
Flyback	$\frac{nD}{1-D}$	$\frac{2V_BR_\gamma}{\left(2V_O-V_\gamma\right)R_B}$
$\Gamma = R_\gamma / R_B$		

3.5 The Integrated Double Buck Offline Converter

Based on the analysis performed so far, a novel AC/DC LED ballast for offline low power down-lighting applications has been investigated.

The purpose is to get a simple, reliable and low cost power supply, characterized by low voltage operating levels, so as to improve robustness avoiding the use of electrolytic capacitors, and capable of power factor correction, to comply with the harmonic injection and energy saving standards.

In order to reach this goal, the simplest solution seems to be the use of two buck stages.

The first one allows to immediately step-down the input line voltage, reducing voltage stresses and improving functional safety, while the second one provides the proper voltage level to feed the LED lamp placed at load side.

Such two buck conversion stages, connected in cascade, are shown in Fig. 3.5.1, where the power switches have been conveniently repositioned, without altering converters operation principles, in order to share a common node and comply with the grafting technique requirements.

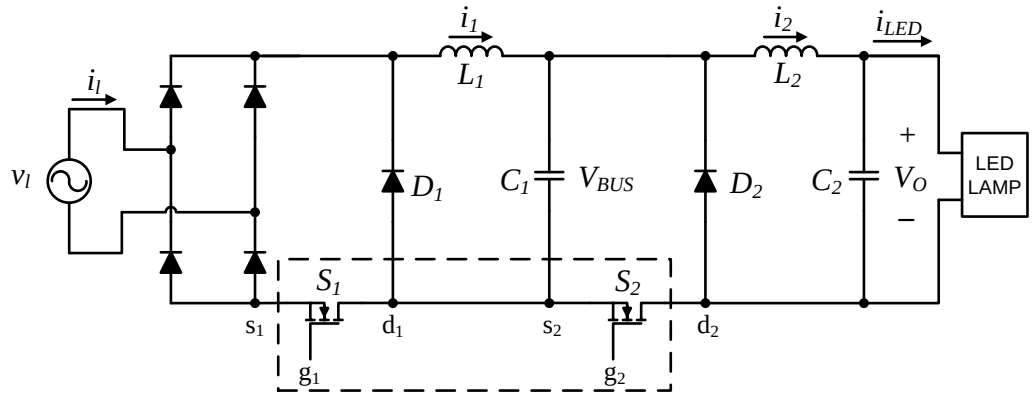


Fig. 3.5.1 - Input PFC and output DC/DC cascaded buck converters.

As it can be noticed, in this way the active switches turn out to be connected according to the typical (drain-source) inverted Π configuration, so that they can be replaced with the I-Π grafted switch, as presented in the analysis of paragraph 3.1.

Due to the integration process, a degree of freedom will be clearly lost in converter design with respect to the conventional two stages configuration.

Sharing the same power switch, indeed, both the obtained semi-stages will be actually operated with the same duty cycle.

Moreover, since such parameter plays a fundamental role in determining both the input semi-stage power factor correction performance and the overall ballast step-down ratio, find out a suitable design trade-off between this needs could not be a trivial task.

So, in order to relax the duty-cycle step-down requirements and compensate for the design degree of freedom lost due to the integration process, the use of a tapped inductor, instead of the standard output filter inductor (L_2), can be investigated, as proposed also in [108]-[113].

Such component, indeed, introducing an additional parameter in the design process, namely its primary to secondary side turns ratio, can actually simplify design procedure and improve converter step-down capability.

The simplified scheme of the resulting integrated double buck (IDB) offline LED lighting power supply, with output filter tapped inductor is shown in Fig. 3.5.2, where the power switches S_1 and S_2 have been replaced with the grafted switch S and a pair of auxiliary diodes D_{A1} and D_{A2}, according to the I-Π GS configuration shown in Fig. 3.1.2 (d).

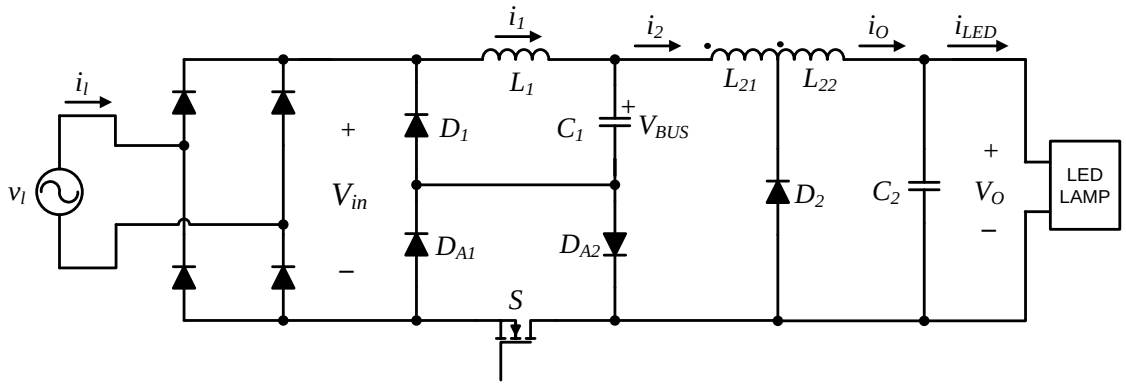


Fig. 3.5.2 - Integrated double buck (IDB) converter with output tapped filter inductor.

In order to understand IDB converter behavior, its operation principles will be analyzed here in the following, in correspondence of a fixed instant within the input full wave rectifier conduction interval (i.e. when $V_{in}=|v_l(t)| > V_{BUS}$).

For sake of simplicity, some preliminary assumption can be done. In particular: all components can be supposed to be ideal, input, BUS and output voltages can be considered (at steady state) to be constant within the whole switching period and, finally, both converter semi-stages can be assumed to operate in discontinuous conduction mode.

Under such hypotheses, in the general case, four different intervals can be identified within converter switching period, involving four of the five topological stages that can possibly occur, as described here in the following.

Interval 1 (Stage 1): [t_0=0, t_1=D/f_{sw}]

When the switch (*S*) is switched-on, both freewheeling diodes (D_1 and D_2) are turned-off, as shown in Fig. 3.5.3, where the conducting paths are highlighted in black and the tapped inductor is modeled through a mutual inductor with series connected windings and magnetizing inductance reported at secondary side.
During such interval, the line energy is partly stored in converter's inductors and partly delivered to the load. The output current results to be:

$$i_O(t) = i_2(t) = i_{L2}(t) - \frac{N_1}{N_2} i_2(t) = \frac{N_2 \cdot i_{L2}(t)}{(N_1 + N_2)} = \frac{i_{L2}(t)}{\Lambda} \tag{3.5.1}$$

where Λ is an adimensional parameter depending on tapped inductor primary and secondary windings number of turns, N_1 and N_2, respectively:

$$\Lambda = \frac{(N_1 + N_2)}{N_2} \tag{3.5.2}$$

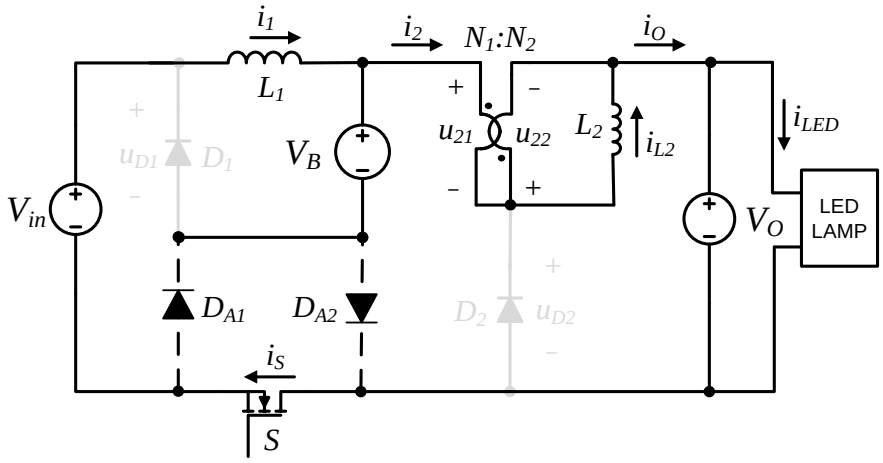


Fig. 3.5.3 - IDB converter equivalent circuit corresponding to the 1st topological stage.

Which one of the two auxiliary diodes is actually conducting depends on BUS current direction, so that, if $i_1 > i_2$ the BUS current will flow through D_{A2}, while being the recycling path otherwise provided by D_{A1} (the two possible paths have been represented in dashed line).

In the former case, the current through the MOSFET will be equal to i_1:

$$i_S(t) = i_1(t) = \frac{V_{in} - V_B}{L_1} \cdot t \tag{3.5.3}$$

while in the latter it will correspond to i_2:

$$i_S(t) = i_2(t) = \frac{i_{L2}(t)}{\Lambda} = \frac{u_{22}}{\Lambda \cdot L_2} \cdot t = \frac{V_B - V_O}{\Lambda^2 \cdot L_2} \cdot t \tag{3.5.4}$$

The voltage stresses on the freewheeling diodes are:

$$u_{D1} = V_{in} \quad \text{and} \quad u_{D2} = V_O + \frac{V_B - V_O}{\Lambda} \tag{3.5.5}$$

Interval 2 (Stage 2): [t_1=D/f_{sw}, t_2]

When the power switch is turned-off, both freewheeling diodes D_1 and D_2 start conducting:

$$i_{D1}(t) = i_{L1}(t) = \frac{V_{in} - V_B}{f_{sw} \cdot L_1} D - \frac{V_B}{L_1}\left(t - \frac{D}{f_{sw}}\right) \tag{3.5.6}$$

$$i_{D2}(t) = i_{L2}(t) = \frac{V_B - V_O}{\Lambda \cdot f_{sw} \cdot L_2} D - \frac{V_O}{L_2}\left(t - \frac{D}{f_{sw}}\right) \tag{3.5.7}$$

(where D is the converter duty-cycle), while the auxiliary diodes D_{A1} and D_{A2} are reverse biased:

$$u_{DA1} = V_{in} \quad \text{and} \quad u_{DA2} = V_O(\Lambda - 1) + V_B \tag{3.5.8}$$

so that the switch voltage stress results to be:

$$u_S = u_{DA1} + u_{DA2} = V_{in} + V_B + V_O(\Lambda - 1) \tag{3.5.9}$$

During this phase the output semi-stage is disconnected from the BUS, which itself is disconnected from the line voltage as shown in Fig. 3.5.4.

Both converter inductors, L_1 and L_2, are thus discharging, delivering their energy respectively to the BUS capacitor and to the paralleled output filter capacitor and LED load.

When the current through one of the inductors reaches zero the just described stage comes to an end. Depending on which of the inductor currents (i_1 and i_{L2}) zeroes first, one of the two intervals, *3A* and *3B*, described here in the following, will occur.

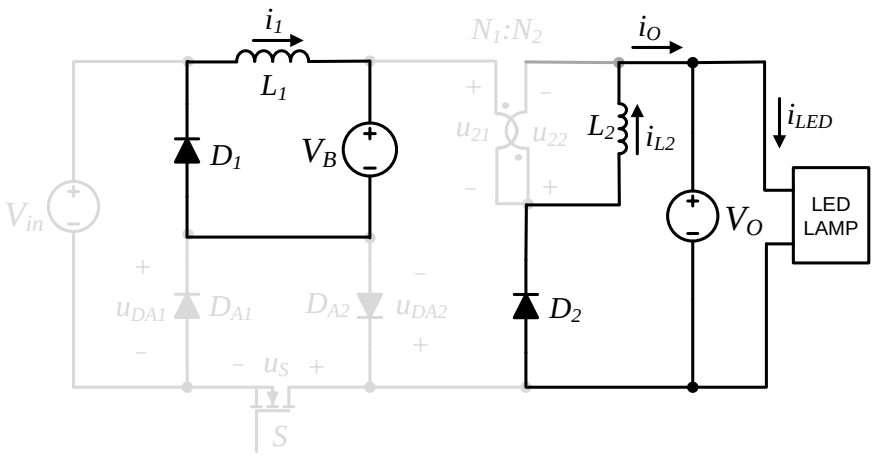


Fig. 3.5.4 - IDB converter equivalent circuit corresponding to the 2nd topological stage.

Interval 3A (Stage 3): [t_2, t_{3A}]

If the current that reaches zero first, is that flowing through the input stage inductor, the corresponding topological stage will be that here shown in Fig. 3.5.5.

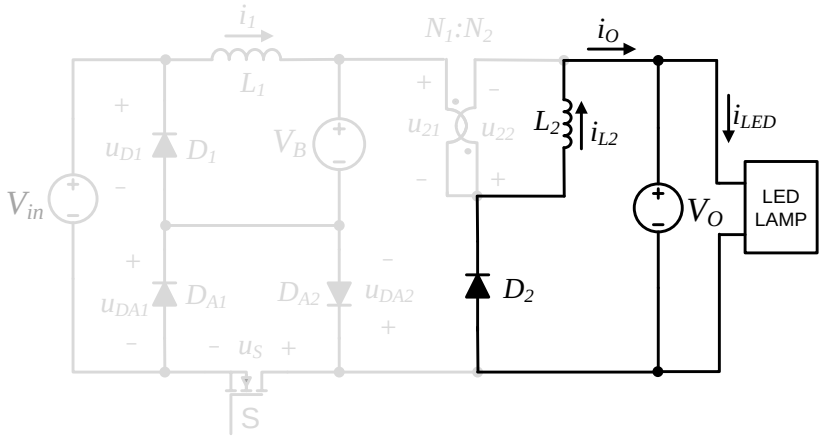


Fig. 3.5.5 - IDB converter equivalent circuit corresponding to the 3rd topological stage.

In such phase the converter is still disconnected from the utility grid, while the output stage freewheeling diode keeps delivering the tapped inductor discharging current to the output filter capacitor and to the LED load, so that the equation (3.5.7) still holds. The voltage stress on the input stage freewheeling diode is equal to the BUS voltage (u_{D1}=V_B), while that on the auxiliary diodes will be:

$$u_{DA1} = V_{in} - V_B \quad \text{and} \quad u_{DA2} = V_O(\Lambda - 1) + V_B \tag{3.5.10}$$

so that the voltage on the main switch will be equal to:

$$u_S = u_{DA1} + u_{DA2} = V_{in} + V_O(\Lambda - 1) \tag{3.5.11}$$

Interval 3B (Stage 4): [t_2, t_{3B}]

If on the other hand, the tapped inductor current reaches zero first, the corresponding topological stage will be that of Fig. 3.5.6.

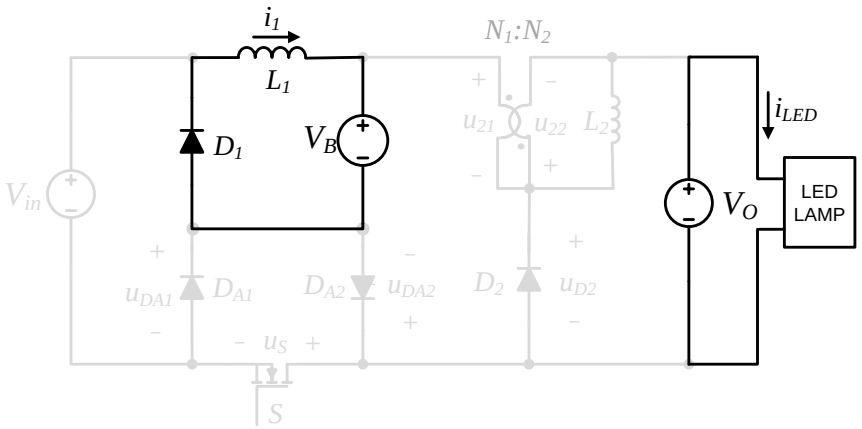


Fig. 3.5.6 - IDB converter equivalent circuit corresponding to the 4th topological stage.

In this case the voltage stresses on the auxiliary diodes and on the main switch will be the same previously computed for the second stage ((3.5.8), (3.5.9)) and also the expression of the input stage freewheeling diode current will be equal to that reported in (3.5.6).
During this interval the converter is still disconnected from the line, the voltage across the second stage freewheeling diode will be equal to the output voltage ($u_{D2}=V_O$) and the LED load will be fed by the output filter capacitor only.

Interval 4 (Stage 5): [t_{3A} or t_{3B}, $T_{sw}=f_{sw}^{-1}$]

The last interval starts when both inductor currents are zero. In this case as it can be noticed by looking at Fig. 3.5.7, all devices are switched off and the only output capacitor is responsible of supplying power to the LED load, until the main switch is turned-on again and another switching period begins.
As concerns the stress levels, the voltages on the auxiliary diodes will be respectively equal to:

$$u_{DA1} = V_{in} - V_B \quad \text{and} \quad u_{DA2} = V_B - V_O \tag{3.5.12}$$

while the voltage stress on the main switch will be that reported in (3.5.11) and, finally, the reverse bias voltages on the input and output semi-stages freewheeling diodes will be equal to the BUS and to the output voltages, respectively.

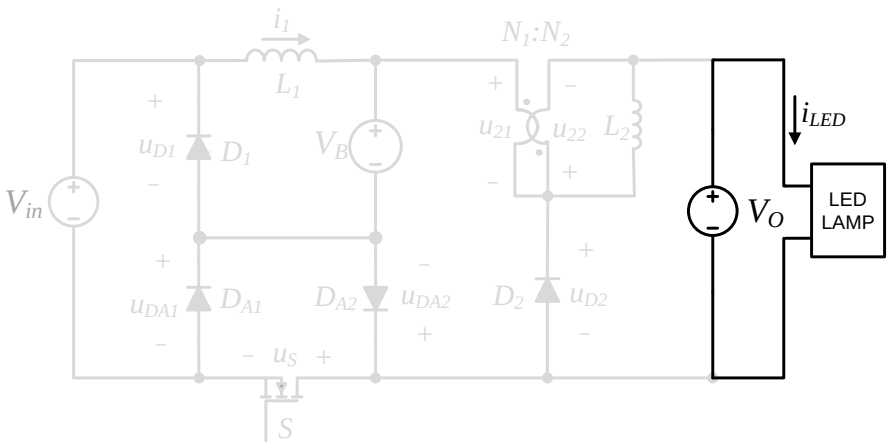


Fig. 3.5.7 - IDB converter equivalent circuit corresponding to the 5th topological stage.

The main current waveforms, characterizing the integrated double buck converter operation within the switching period are shown here in Fig. 3.5.8, where the current through the input semi-stage filter inductor is supposed to reach zero first, so that the resulting topological intervals sequence is: *1, 2, 3A, 4.*

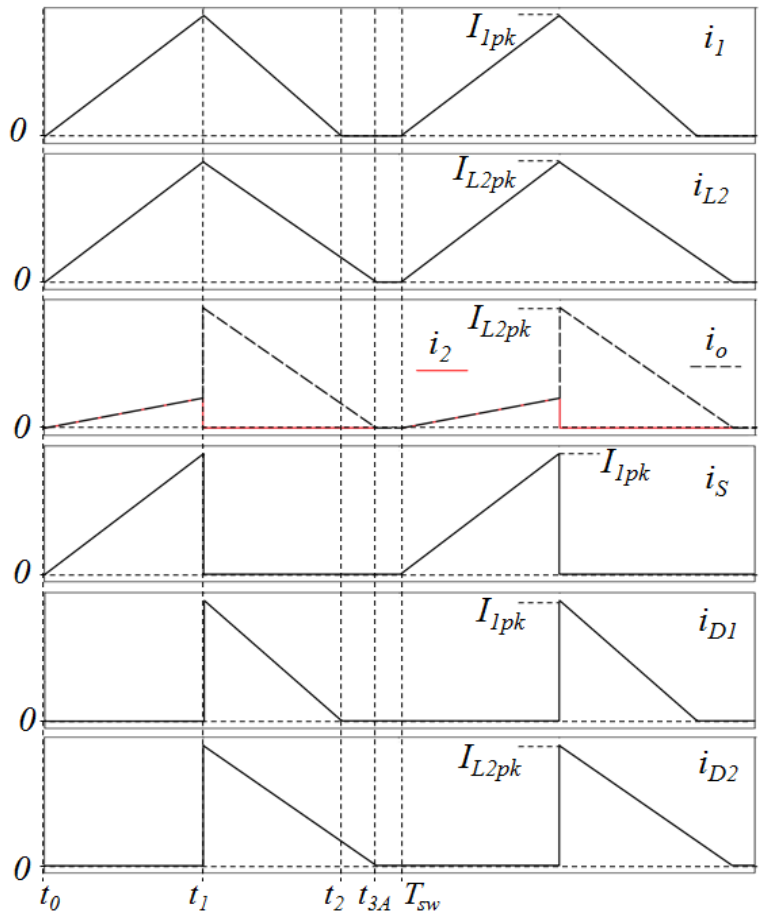


Fig. 3.5.8 - Main IDB converter current waveforms in DCM operation.

3.6 Performance of the Input and Output Semi-Stages

As already discussed in paragraphs 3.2 and 3.3, the main offline integrated converter issues are the respect of harmonic injection and of energy saving standards on one hand and the minimization of the twice the line BUS voltage ripple transferred to the LED lamp on the other.

As concerns the input side, discontinuous conduction mode (DCM) has been considered in the analysis of IDB converter operation principles previously performed in paragraph 3.1.

This mode of operation is, indeed, preferable if compared to the continuous conduction, so as to be able to get good power factor correction performance with a very straightforward control at constant duty-cycle, without the need to perform any kind of input current sensing.

Moreover, it can also be noticed that, in DCM, freewheeling diode reverse recovery results to be a minor issue, so that low cost ultrafast PFC diodes can be used instead of expansive high voltage Schottky diodes like SiC devices.

Obviously, as a drawback, the PFC choke will have to be designed in order to guarantee DCM operation in the whole line half period over the full load, resulting in possibly high input current peaks that require a proper input choke sizing, in order to maintain reasonable flux levels. However, being the converter intended for low power applications with European and not universal AC line range, even this aspect will actually result to be a minor issue.

The waveform of the proposed IDB converter input current, averaged over converter switching period, will resemble the one previously shown in Fig. 3.2.4.

In particular, keeping in mind the relationship between the dead angle (θ_1) and the BUS and line voltage, reported in (3.4.4), the full wave rectifier conduction angle (θ_C) will result to be:

$$\theta_C = \pi - 2\theta_1 = \left[\pi - 2\sin^{-1}\left(\frac{V_B}{\sqrt{2}V_{lRMS}} \right) \right] \tag{3.6.1}$$

Within such interval, in DCM, the inductance current peaks will vary, as a function of the line voltage, according to the law:

$$i_{1pk}(t) = \frac{\sqrt{2}V_{lRMS}\sin(\omega_l t) - V_B}{f_{sw} \cdot L_1} \cdot D \tag{3.6.2}$$

so that the expression of the input current, averaged over converter switching period, will be finally equal to:

$$i_l(t) = i_{1pk} \cdot \frac{D}{2} = \frac{D^2}{2 f_{sw} L_1} \cdot \left(\sqrt{2} V_{lRMS} \sin(\omega_l t) - V_B \right) \tag{3.6.3}$$

as shown in Fig. 3.6.1.

From such expression it can be noticed that a good power factor correction can be achieved if converter duty cycle and switching frequency are kept constant and the voltage conversion ratio in correspondence of line peak:

$$M_{in} = V_B / \sqrt{2} V_{lRMS} \tag{3.6.4}$$

is sufficiently low.

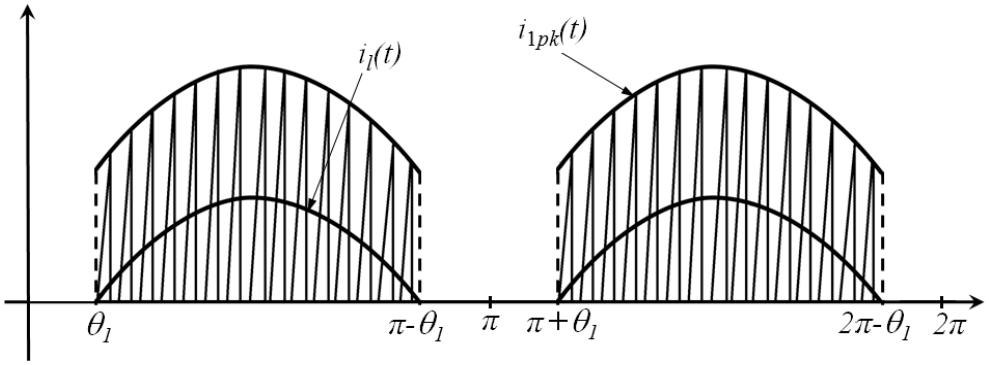


Fig. 3.6.1- Buck PFC instantaneous and average input currents.

As a reference of the achievable converter line side performance, the expression of buck input semi-stage power factor, can be easily derived by substituting (3.6.3) and (3.4.4) in the power factor definition, as follows:

$$PF = \frac{P}{S} = \frac{\int_{\theta_1/\omega_l}^{(\pi-\theta_1)/\omega_l} \left[v_l(t) \cdot i_l(t) \right] dt}{\sqrt{\int_0^{\pi/\omega_l} v_l^{\,2}(t)\, dt} \cdot \sqrt{\int_{\theta_1/\omega_l}^{(\pi-\theta_1)/\omega_l} i_l^{\,2}(t) dt}} =$$

$$= \frac{\frac{V_{lRMS}^{\,2} D^2}{2 f_s L_1} \cdot \left(1 - \frac{2}{\pi} \sin^{-1}\left(\frac{V_B}{\sqrt{2} V_{lRMS}} \right) - \frac{V_B \sqrt{2 V_{lRMS}^{\,2} - V_B^{\,2}}}{\pi V_{lRMS}^{\,2}} \right)}{2 V_{lRMS} \cdot \sqrt{\frac{V_{lRMS}^{\,2} D^4}{4 f_s^{\,2} L_1^{\,2}} \cdot \left[\left(1 + \frac{V_B^{\,2}}{V_{lRMS}^{\,2}} \right) \left(1 - \frac{2}{\pi} \sin^{-1}\left(\frac{V_B}{\sqrt{2} V_{lRMS}} \right) \right) - \frac{3 V_B \sqrt{2 V_{lRMS}^{\,2} - V_B^{\,2}}}{\pi V_{lRMS}^{\,2}} \right]}} =$$

$$= \frac{1-\frac{2}{\pi}\sin^{-1}\left(M_{in}\right)-\frac{2M_{in}\sqrt{1-M_{in}^{\ 2}}}{\pi}}{\sqrt{\left[\left(1+2M_{in}^{\ 2}\right)\left(1-\frac{2}{\pi}\sin^{-1}\left(M_{in}\right)\right)-\frac{6M_{in}\sqrt{1-M_{in}^{\ 2}}}{\pi}\right]}} \tag{3.6.5}$$

whose variation, as a function of the voltage conversion ratio at the line peak is shown in Fig. 3.6.2.

For the considered application, the minimum requirements to be complied are those imposed by the EN61000-3-2 class D standard for equipments of power lower than 25W, that regulates all input current odd harmonics up to the 39th, to prevent harmful interactions among different devices connected to the power distribution system.

Although any specific constraint regarding power factor is not explicitly provided from this standard, some kind of relationship, between the minimum acceptable value of such parameter and the given harmonic specifications, can be found.

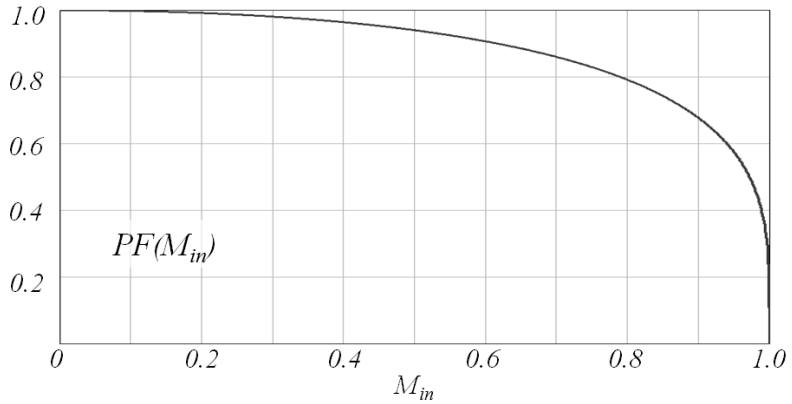


Fig. 3.6.2 - Power factor guaranteed by buck converter operated in DCM at constant switching frequency and duty cycle, as a function of the BUS/line peak voltage conversion ratio.

Considering an input current waveform complying with the minimum requirements fixed by the standard, the associated power factor value can be computed, according to the definition given in (3.2.12), as the product of the displacement and distortion factors. Assuming, in general, the effect of the EMI filter reactive current, that is responsible of the input current displacement, to be negligible at full load (cos(Φ)=1), the power factor will reduce to:

$$PF = \frac{I_1}{I_{lRMS}} = \frac{I_1}{\sqrt{\sum_{n=0}^{19} i_{(2n+1)}^{\ 2}}} \tag{3.6.6}$$

Therefore, considering the current harmonic constraints imposed by the standard, listed in Table 2.1.1, the corresponding power value can be computed as:

$$PF = \frac{P/V_{IRMS}}{\sqrt{\left(\frac{P}{V_{IRMS}}\right)^2 + \sum_{n=1}^{19}\left(P \cdot \beta_{2n+1}\right)^2}} = \frac{1}{\sqrt{1 + V_{IRMS}^2 \sum_{n=1}^{19}\left(\beta_{2n+1}\right)^2}} = 0.726 \qquad (3.6.7)$$

where β_{2n+1} $(=i_{2n+1}/P)$ are the maximum permissible current harmonics per unit of power and a $230V_{RMS}$ line voltage has been considered.

It should be noticed that guaranteeing this minimum PF value is clearly only a necessary condition, not being itself sufficient to guarantee the compliance with the EN 61000-3-2 specificatons. Nevertheless, the performed computation provides an useful hints of the fact that very high power factor values are not actually required in order to comply with the constraints imposed by such harmonic standard.

This therefore effectively reveals that, as concerns the application under study, buck converter can be confidently considered as a suitable solution for the input PFC stage implementation, despite its inherent input current crossover distortion, as shown also in [114]-[124].

Moreover, Fig. 3.6.2 clearly shows that also more restrictive energy saving requirements, like for example the Energy Star® (that calls for a PF higher than 0.9), can be taken into account, since they can be easily complied with reasonable step-down ratios.

As still concerns line side behavior, it should be also observed that, from EMC perspective, buck PFC is usually considered a quite problematic solution, because of the position of the active controlled switch, that is placed in series with the input path, while being the filter inductor on the output side.

However, in practice, the resulting pulsating input current will be quite similar to that deriving from the use of other kinds of topologies, like boost or flyback PFC, operated in discontinuous or transition mode, in which the inductor current is allowed to reach zero or to go fully discontinuous.

As a result, filtering requirements will not actually result to be much more demanding with respect to these solutions at the same power level.

Once clarified the main aspects related to the integrated double buck converter PFC issue, it is therefore, possible to move to the discussion of the output semi-stage behavior.

In this regards, several different aspects, like the freewheeling diode recovery issue, the inductance current design complexity, the peak current levels, the conduction and

switching losses, etc..., can be taken into account, in order to identify the most convenient operation mode.

However, despite the many contrasting considerations that can be done, there is a major issue that could significantly favor the choice of the one or of the other, between the two possible operation modes, that is the value of the BUS voltage ripple conversion factor, defined in (3.3.7).

Indeed, given a specific LED current variation range, the lower such factor results to be, the larger will be the allowed BUS voltage ripple (ΔV_B), giving the possibility to reduce the BUS capacitor value (C_B) and, therefore, to avoid the use of low lifetime electrolytic capacitors, that is namely one of the main goals of the proposed converter.

Now, in order to be able to properly evaluate converter performance in this regards, it is worth to make some further effort, addressing the analysis of the voltage conversion ratio, in both the continuous and the discontinuous case.

A. Continuous Conduction Operating Mode

When the output semi-stage is operated in CCM, neither the interval 3B nor the interval 4, previously described in paragraph 3.1, will take place.

In such condition, indeed, the operation of load side buck converter will be characterized by the occurrence of only two different topological stages. A first one corresponding to the conduction interval of the main power switch, during a time $T_{ON}=D/f_{sw}$, and a second one characterized by the forward biasing of the freewheeling diode, during the remaining part of the switching period ($T_{OFF}=(1-D)/f_{sw}$).

So, imposing the flux balance on the tapped inductor:

$$\frac{V_B - V_O}{\Lambda} \cdot T_{ON} = V_O \cdot T_{OFF} \tag{3.6.8}$$

the following voltage conversion ratio can be derived for the output semi-stage:

$$M_{outCCM} = \frac{D}{D + (1-D)\Lambda} \tag{3.6.9}$$

that clearly reduces to the typical expression, relative to a buck converter operating in continuous operation mode, if a standard inductor is used instead of the tapped inductor ($\Lambda=1$, i.e. $N_1=0$).

Now, being the voltage conversion ratio in CCM independent of the load, the BUS voltage ripple transformation factor can easily be derived and written as:

$$\nu_{CCM} = \frac{\partial\left(M_{outCCM} \cdot V_B\right)}{\partial V_B} = M_{outCCM} = \frac{D}{D + \left(1 - D\right)\Lambda} \tag{3.6.10}$$

Moreover, since in continuous conduction mode the relation between the output current (i_O) and the current through the tapped inductor inductance (i_{L2}) can be summarized as follows:

$$i_O(t) = \begin{cases} i_{L2}(t) / \Lambda, & \text{during } \mathrm{T_{ON}} \text{ interval (Stage 1)} \\ i_{L2}(t), & \text{during } \mathrm{T_{OFF}} \text{ interval (Stage 2 and 3)} \end{cases} \tag{3.6.11}$$

the relationship between their average values will actually result to be:

$$I_O = I_{L2}\left(1 + D \cdot \frac{1 - \Lambda}{\Lambda}\right) \tag{3.6.12}$$

B. Discontinuous Conduction Operating Mode

As known, in discontinuous conduction mode, the filter inductance discharge current reaches zero before the end of the switching period, so that the output buck converter operation is characterized by the occurrence of three different topological phases ($\mathrm{T_{ON}}$, $\mathrm{T_{OFF1}}$ and $\mathrm{T_{OFF2}}$) within the switching period.
In such situation, the output current can be expressed as:

$$i_O(t) = \begin{cases} i_{L2}(t) / \Lambda, & \text{during the } \mathrm{T_{ON}} \text{ interval (Stage 1)} \\ i_{L2}(\mathrm{t}), & \text{during the } \mathrm{T_{OFF1}} \text{ interval (Stage 2 and 3)} \\ 0, & \text{during the } \mathrm{T_{OFF2}} \text{ interval (Stage 4 and 5)} \end{cases} \tag{3.6.13}$$

so that the relation between the output and tapped inductance averaged currents will result to be:

$$I_O = \frac{I_{L2pk}}{2\Lambda} \cdot \frac{T_{ON} + \Lambda \cdot T_{OFF1}}{T_{sw}} \tag{3.6.14}$$

where I_{L2pk} is the peak value of the current through $\mathrm{L_2}$:

$$I_{L2pk} = \frac{V_B - V_O}{\Lambda L_2} T_{ON} \tag{3.6.15}$$

Now, keeping in mind also the flux balance on the tapped inductor, that is:

$$\frac{V_B - V_O}{\Lambda} T_{ON} = V_O T_{OFF1} \tag{3.6.16}$$

and solving the system of (3.6.14), (3.6.15) and (3.6.16) for V_O, the following expression of voltage conversion ratio can be found:

$$M_{outDCM} = \frac{V_O}{V_B} = \frac{D^2}{D^2 + \frac{2 f_{sw} L_2}{V_B} I_O \Lambda^2} = \frac{1}{1 + I_{ON} \Lambda^2} \tag{3.6.17}$$

in which the average output current I_O has been normalized through the current:

$$I_N = \frac{V_B}{R_N} \tag{3.6.18}$$

where the base resistance (R_N) is defined as:

$$R_N = \frac{2 f_{sw} L_2}{D^2} \tag{3.6.19}$$

In presence of a LED load, like in the case of the target application here considered, the output voltage can be written as in (3.3.8), so that the expression (3.6.17) can be adjusted as follows:

$$M_{outDCM} = \frac{1}{2}\left(\frac{V_\gamma}{V_B} - \frac{\Gamma}{\Lambda^2}\right) + \sqrt{\left(\frac{V_\gamma}{2V_B} - \frac{\Gamma}{2\Lambda^2}\right)^2 + \frac{\Gamma}{\Lambda^2}} \tag{3.6.20}$$

where $\Gamma = R_\gamma / R_N$.

By taking the derivative of the output voltage with respect to the BUS voltage, the expression of the BUS voltage ripple transformation factor can be finally found also in discontinuous conduction mode:

$$\nu_{DCM} = \frac{\partial\left(M_{DCM} V_B\right)}{\partial V_B} = -\frac{\Gamma}{2\Lambda^2} + \frac{V_B\left(\frac{\Gamma^2}{2\Lambda^2} + 2\Gamma\right) - \frac{\Gamma V_\gamma}{2}}{2\Lambda^2 V_O - \Lambda^2 V_\gamma - \Gamma V_B} \tag{3.6.21}$$

Therefore, once the parameters characterizing the target application have been determined, it will be possible to estimate the output semi-stage voltage ripple attenuation performance in both conduction modes, by simply computing the values of (3.6.10) and (3.6.21).

As it will be shown in the next paragraph, this is a very useful information, since it actually provide a suitable tool to select the most appropriate conduction mode between the continuous and discontinuous options.

3.7 Integrated Double Buck Converter Design

Once that the main aspects related to converter behavior, PFC issue and ripple attenuation performance have been discussed, it is now possible to address the converter design concern. From this perspective, the main aim is to define a proper design procedure in order to realize an integrated double buck converter complying with the target application specifications, that are reported in Table 3.7.1.

First of all, the selection of a proper switching frequency value is, as usual, a non trivial trade-off among conflicting constraints like converter efficiency, electromagnetic interference issues, compactness, etc..., so that its actual value will depend on which of such aspects is supposed to have the priority.
From the EMC perspective, the typical requirements on conducted emission apply from 150kHz upwards so that the maximum switching frequency should be limited below such boundary value. Therefore, being also switching losses and converter compactness both fundamental issues, a converter switching frequency of 100kHz can actually be considered as a reasonable compromise among EMC, power density and efficiency constraints.

Once the switching frequency has been selected, it is possible to focus on the PFC semi-stage design. From this standpoint, given the analysis performed in paragraph 3.4, the most important design parameter turns out to be the BUS voltage level.

TABLE 3.7.1 - TARGET APPLICATION SPECIFICATIONS

MAIN CONVERTER PARAMETERS		
NAME	SYMBOL	VALUE
Line input RMS voltage	V_{lRMS}	230V ± 20%
Line frequency	f_l	50Hz
Power Factor	PF	0.9
LED load current mean value	I_{LED}	0.5A
Maximum LED current ripple @2 f_l	Δi_{LED}	±10%
Maximum LED current ripple @2 f_{sw}	Δi_O	±1%
LED lamp threshold voltage	V_γ	27V
LED lamp series resistance	R_γ	5Ω
Overall converter efficiency	η	> 85%

A minimum PF value of 0.9 can be considered, so as to comply with Energy Star® requirements, that, according to the graph of Fig. 3.7.1(corresponding to the equation (3.6.5)), actually results in the following maximum line peak to BUS voltage conversion ratio:

$$M_{inMAX} = 0.6 \tag{3.7.1}$$

So, assuming a tolerance margin of more or less the 20% on the European line nominal RMS value, as shown in Table 3.7.1, the nominal BUS voltage turns out to be:

$$V_B = 80\% \cdot \sqrt{2} V_{lRMS} \cdot M_{inMAX} \tag{3.7.2}$$

that, in nominal conditions, will result in a dead angle:

$$\theta_1 = \omega_l t_1 = \sin^{-1}\left(\frac{V_B}{\sqrt{2} V_{lRMS}} \right) \tag{3.7.3}$$

corresponding to a conduction interval equal to more or less the 70% of the half line period.

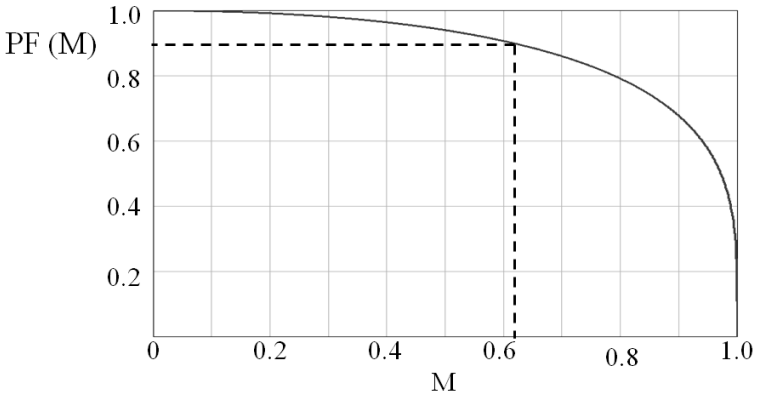


Fig. 3.7.1 - Maximum line peak to BUS voltage conversion ratio allowed to comply with the Energy Star® requirements.

Once fixed the dead angle and the BUS voltage level, as concerns the input semi-stage, the remaining parameters to be determined are the converter duty ratio (D), the BUS capacitance (C_B) and the input choke (L_1) values.

Being BUS capacitor value dependent on issues regarding the output LED current ripple, that will be discussed later, it is worth now to focus on the design of the other two mentioned parameters, that, thanks to the degree of freedom introduced by the use of an output tapped inductor filter, can be designed independently from load side specifications.

In particular, as concern the input choke, the goal is to guarantee the discontinuous conduction mode in the whole input line voltage variation range.

Looking at the waveforms reported in Fig. 3.7.2, it can be noticed that, within the conduction interval, the line current (averaged over the switching period) can be written as:

$$i_l(\theta) = \hat{I}_{pk}\left[\sin(\theta) - \sin(\theta_1)\right], \qquad \theta_1 < \theta < \pi - \theta_1 \tag{3.7.4}$$

(where $\theta = \omega_l t$) so that the average input power can be computed:

$$P_{in} = \frac{2}{\pi}\int_0^{\pi/2} v_l(\theta)\cdot i_l(\theta)\, d\theta = \frac{\sqrt{2}V_{lRMS}\hat{I}_{pk}}{\pi}\left[\frac{\pi}{2} - \theta_1 - \sin(\theta_1)\cos(\theta_1)\right] \tag{3.7.5}$$

and the line current peak can be expressed as:

$$I_{lpk} = i_l(\frac{\pi}{2}) = \hat{I}_{pk}\cdot\left[1-\sin(\theta_1)\right] = \frac{P_{in}}{\sqrt{2}V_{lRMS}}\cdot\frac{\pi\left(1-\sin(\theta_1)\right)}{\frac{\pi}{2} - \theta_1 - \sin(\theta_1)\cos(\theta_1)} \tag{3.7.6}$$

Now, in order to guarantee DCM operation in the whole line half period, the PFC choke maximum value can be computed so as to guarantee border line operation between continuous and discontinuous conduction mode to occur in correspondence of the worst case condition (i.e. for $\theta = \pi/2$).

Keeping in mind that, at the boundary between CCM and DCM, the mean current through the inductor is equal to a half of the peak value and that the mean value of the current through the switch is equal to the inductance current mean value multiplied by the converter duty cycle, it can be written:

$$\frac{1}{2}\cdot\left[\frac{V_B}{L_1}\frac{\left(1-D\right)}{f_{sw}}\right]\cdot D = I_{lpk} \tag{3.7.7}$$

So, being at boundary condition, the duty cycle equal to the voltage conversion ratio ($M_{in} = V_B / \sqrt{2}V_{lRMS} = D$), substituting (3.7.6) in (3.7.7) and solving for L_1, the maximum PFC choke limit value can be derived:

$$L_{1\max} = \frac{V_B}{2I_{ipk}f_{sw}}\left(1-D\right)D = \frac{{V_B}^2}{2\pi f_{sw}P_{in}}\frac{\left[\frac{\pi}{2} - \theta_1 - \cos(\theta_1)\sin(\theta_1)\right]}{\left(1-\sin(\theta_1)\right)}\left(1-\frac{V_B}{\sqrt{2}V_{lRMS}}\right) \tag{3.7.8}$$

where under the assumptions of ideally unity converter efficiency and low LED current ripple the input power can be approximated as:

$$P_{in} \simeq P_O \simeq V_\gamma I_{LED} + R_\gamma I_{LED}^2 \tag{3.7.9}$$

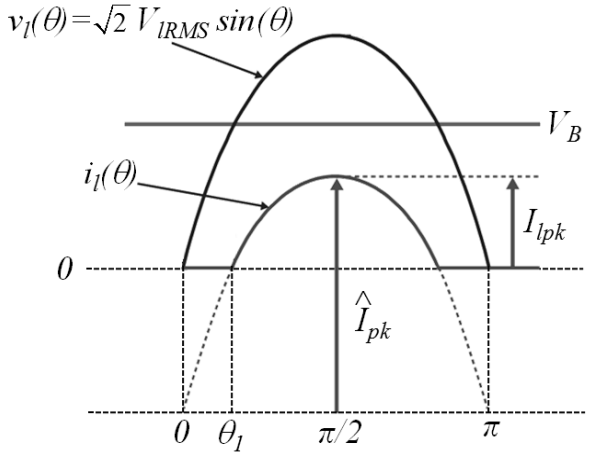


Fig. 3.7.2 - IDB converter input current and voltage waveforms within the line half period.

Once a proper filter inductance has been selected, converter duty cycle value can be computed, so as to deliver the desired amount of power ($P_O \sim P_{in}$) to the load.

To this end, keeping in mind the expressions (3.6.3) and (3.7.3), during the line conduction angle [θ_1,π-θ_1] the line current, averaged over converter switching period, can be written as:

$$i_l(\theta) = \frac{D^2}{2L_1 f_{sw}} \cdot \sqrt{2} V_{lRMS} \left(\sin(\theta) - \sin(\theta_1)\right), \qquad \theta_1 < \theta < \pi - \theta_1 \tag{3.7.10}$$

so that the expression of converter input average power can written as:

$$P_{in} = \frac{2}{\pi} \int_0^{\pi/2} v_l(\theta) \cdot i_l(\theta)\, d\theta = \frac{2D^2}{\pi L_1 f_{sw}} \cdot V_{lRMS}^2 \cdot \int_0^{\pi/2} \left(\sin^2(\theta) - \sin(\theta)\sin(\theta_1)\sin(\theta_1)\right) d\theta$$

$$= \frac{D^2 V_{lRMS}^2}{\pi L_1 f_{sw}} \cdot \left[\frac{\pi}{2} - \theta_1 - \sin(\theta_1)\cos(\theta_1)\right] \tag{3.7.11}$$

from which the value of the required converter duty cycle can be actually computed:

$$D = \sqrt{\frac{\pi L_1 f_{sw} P_{in}}{V_{lRMS}^2 \cdot \left[\frac{\pi}{2} - \theta_1 - \sin(\theta_1)\cos(\theta_1)\right]}} \tag{3.7.12}$$

As concerns the output semi-stage, the boundary value of the output filter inductance, corresponding to border line operation between continuous and discontinuous conduction mode (L_{2BL}) can be derived, as usual, by imposing the peak to peak value of the current ripple on L_2 to be equal to twice the average current value.

At the boundary between continuous and discontinuous conduction mode, the value of the parameter Λ, defined in (3.5.2), can be derived from the expression (3.6.9) of the output semi-stage voltage conversion ratio in continuous conduction mode:

$$\Lambda_{CCM} = \left(\frac{1}{M_{outCCM}} - 1 \right) \cdot \frac{D}{(1-D)} \tag{3.7.13}$$

where $M_{outCCM}=V_o/V_B$.

So, since in steady state condition the peak to peak ripple of the tapped inductor magnetizing current is equal to:

$$\Delta i_{L2} = \frac{(V_B - V_O) \cdot D}{L_2 f_{sw}} \ , \tag{3.7.14}$$

imposing the previously mentioned condition:

$$\Delta i_{L2} = 2 \cdot I_O \tag{3.7.15}$$

and keeping in mind the average output current expression reported in (3.6.12), the desired boundary value of the tapped inductor magnetizing inductance can be finally found as:

$$L_{2BL} = \frac{(V_B - V_O) D}{2 f_{sw} I_O} = \frac{(V_B - V_O) D}{2 f_{sw} I_{L2} \left(1 + D \cdot \frac{1-\Lambda_{CCM}}{\Lambda_{CCM}} \right)} \tag{3.7.16}$$

Now, the expression (3.7.16) will actually correspond to the minimum acceptable tapped inductor magnetizing inductance, if the output semi-stage is supposed to operate in CCM, while indicating, instead, the the maximum of such parameter, if discontinuous conduction is desired.

In the latter case, once a proper magnetizing inductance (L_2), lower than (3.7.16), has been selected, the value of the parameter Λ can be recalculated from (3.6.17), so as to guarantee the desired input output voltage conversion ratio (M_{outDCM}) of the output semi-stage:

$$\Lambda_{DCM} = \sqrt{\left(\frac{D^2}{M_{outDCM}} - D^2 \right) \frac{V_B}{2 f_{sw} L_2 I_{LED}}} \tag{3.7.17}$$

Given the characteristics of the target application, keeping in mind the expressions of BUS voltage ripple transformation factor, reported in (3.6.10) and (3.6.21), the ripple attenuation provided by the output semi-stage turns out to be much stronger in DCM if compared to CCM operation.

In particular, to have a rough idea of the significance of this issue, if the values listed in Table 3.7.1 and Table 3.7.2 are considered, it can be computed that DCM operation will allow the selection of a six times smaller BUS capacitance, with respect to CCM.
Therefore, given the LED current twice the line frequency ripple specification (Δi_{LED}), this will consequently allow to tolerate a significantly larger BUS voltage variation:

$$\Delta V_B = \frac{R_\gamma \cdot \Delta i_{LED}}{\nu} \tag{3.7.18}$$

thus considerably relaxing the constraint on BUS filter capacitance value:

$$C_B = \frac{2\theta_1 \cdot P_O}{2 f_l V_B \Delta V_B} = \frac{2\theta_1 \cdot I_{LED}(R_\gamma I_{LED} + V_\gamma)}{2 f_l V_B \Delta V_B} \tag{3.7.19}$$

where the assumption of small LED current ripple has been exploited in order to compute the output power (P_O) approximating LED current RMS value with its mean value.
This actually gives the possibility to avoid the use of low lifetime electrolytic capacitors, sensibly improving converter robustness so that, for the considered application, discontinuous operation effectively turns out to be the most suitable conduction mode also for converter output semi-stage, as considered in the analysis of paragraph 3.5.
Moreover, it is worth to mention another relevant drawback, reported in literature [125], deriving from the choice of operating the output semi-stage in CCM when using integrated PFC topologies. Namely, the increase of BUS voltage stress in light load conditions with constant voltage loads.

TABLE 3.7.2 - CONVERTER DESIGN OUTCOMES

MAIN CONVERTER PARAMETERS		
NAME	SYMBOL	VALUE
Switching frequency	f_{sw}	100 kHz
BUS voltage nominal value	V_B	156V
Nominal conduction angle	$\theta_C = (\pi - 2\theta_1)$	0.68 π
PFC choke	L_1	1 mH
Minimum BUS capacitor	C_B	27 μF
Duty Cycle	D	0.42
Tapped inductor secondary side inductance	L_2	90 μH
Tapped inductor ratio	Λ	3.85
Ripple transformation factor	ν	0.038
Output Capacitor	C_O	50 μF

This problem, indeed, although less critical, applies also to the case of LED loads, in which slight voltage changes actually produce large current variations.
In order to understand such issue, it can be just considered the case in which the control reference is varied to perform LED light dimming.
If the output semi-stage operates in CCM, its voltage conversion ratio will be independent of the load current level, while being a function of converter duty cycle.
To meet the new reference, the regulator will consequently change the duty cycle value, so as to adjust the load voltage an get the desired output current.
However, due to the different dependence of converter input and of the output power on the duty cycle value, this variation will actually turn into a power unbalance between the input and the output semi-stages, that has to be compensated by the BUS capacitor.
In particular, considering the typical LED load voltage-current characteristic, a converter duty-cycle reduction will actually cause the input power to exceed the value of the load power.
The unbalanced power will be, therefore, stored in the BUS capacitor (C_B), actually causing the increase of the BUS voltage. Consequently, the feedback loop will further decrease converter duty cycle, so as to regulate the output and keep the LED current constant. As a result, the input power will also decrease correspondingly, due to the combined effect of duty ratio reduction and of line conduction angle shrinking, caused by the increasing BUS voltage.
The just described dynamic process will clearly continue until the input power matches the output power, and a new power equilibrium is reached. However, for large load current changes, this will obviously come at the cost of significant variations of the BUS voltage stress.

Once clarified this non negligible issue, the output filter capacitor (C_O) can be, at last, selected so as to guarantee the switching frequency ripple on the LED current (Δi_O) to be a given percentage of the nominal output current:

$$C_O = \frac{I_{LED}(1-D)}{f_{sw} R_\gamma \Delta i_O} \tag{3.7.20}$$

As concerns closed loop operation, the simplest solution is to adjust converter duty cycle by regulating to zero the error between the sensed LED current and a proper reference signal, in order to respond to line voltage variations (with respect to the nominal condition) or to perform lamp light dimming.

The error amplifier should be designed for very slow response, to get a low overall feedback control loop bandwidth, so as to filter the output current twice the line frequency ripple, thus maintaining converter duty-cycle close to its DC value, guaranteeing good power factor correction performance.

For sake of completeness, it is worth to remember that, in the analysis performed so far, converter devices non idealities have been neglected. However, it should be observed that, when realizing the output filter tapped inductor, the minimization of its parasitic leakage inductance will be a major issue, in order to minimize the voltage peak stress on the power switch and improve converter efficiency and reliability.

3.8 Converter Simulation Outcomes

The effectiveness of the converter design procedure, presented in the previous paragraph 3.7, can be tested by simulating the integrated double buck converter behavior in PLECS®. To this end a converter model has therefore been built in such software platform, as shown in Fig. 3.8.1, according to the design outcomes listed in Table 3.7.2.

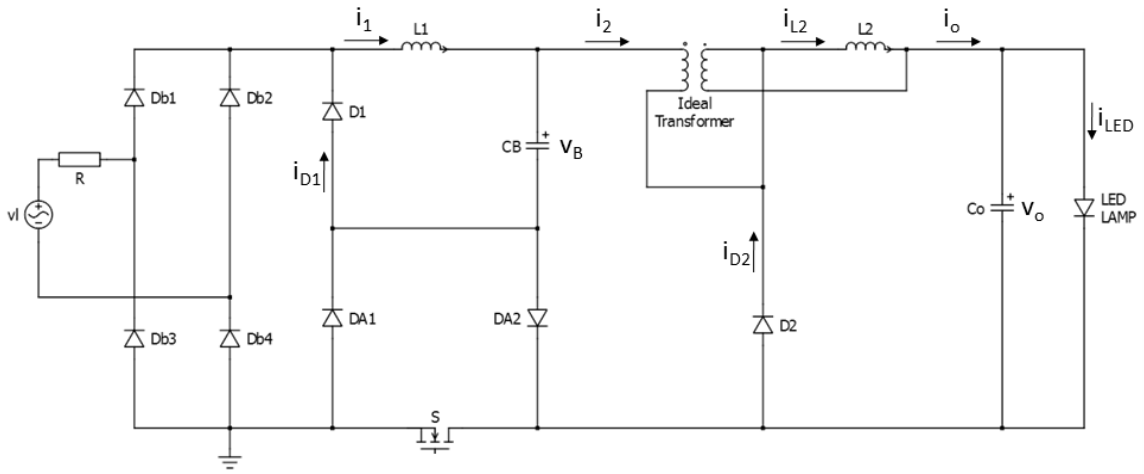


Fig. 3.8.1 - PLECS® model of the IDB converter.

As concerns the IDB converter behavior within the switching period, Fig. 3.8.2 shows the waveforms of the currents through the first filter inductor, the tapped inductor primary winding, secondary winding and magnetizing inductance, the active controlled switch and the freewheeling diodes, in correspondence of the line voltage peak. As it can be noticed, the current through both inductors is allowed to go fully discontinuous also in this condition, thus proving the effectiveness of the performed design in guaranteeing DCM operation of the input and output semi-stages in the whole line period.

On the other hand, as concerns converter behavior in the line period the simulated waveforms of line voltage and filtered current, BUS voltage, output voltage and LED current are shown in Fig. 3.8.3. As it can be observed, converter behavior effectively meets the design specification, being the resulting actual power factor equal to 0.92 and the LED current peak to peak ripple equal to ±10% of the nominal value, as required.

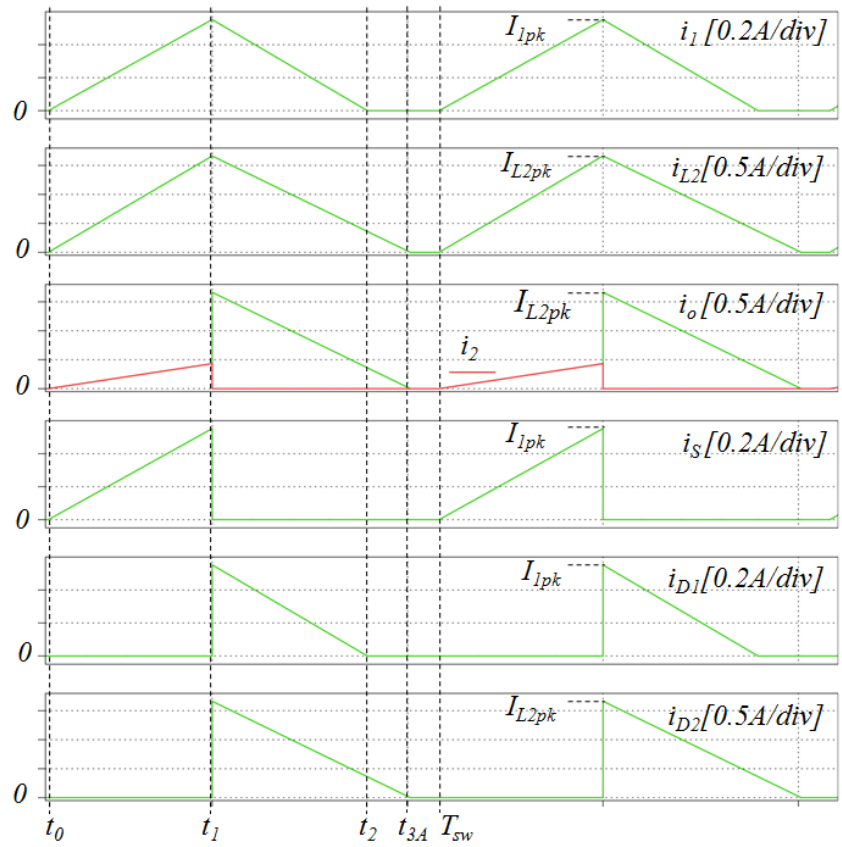


Fig. 3.8.2 - Main DIB converter current waveforms (@ f_{sw}) in correspondence of the line peak

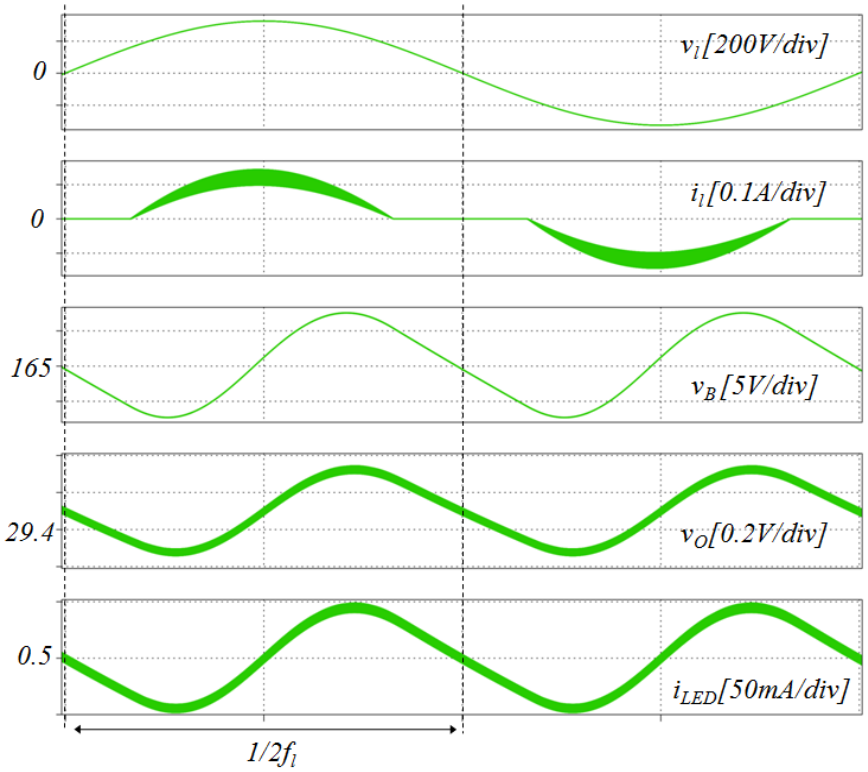


Fig. 3.8.3 - Main DIB converter waveforms within the line period.

On the basis of converter design outcomes (Table 3.7.2), the actual need to employ either or both the grafted switch auxiliary diodes can be also briefly discussed.

In this perspective, it should be noticed at first that the current flowing through each buck converter power switch in the original cascaded configuration (Fig. 3.5.1) is unidirectional, so that the considered issue can be addressed by simply evaluating the relationship between the magnitudes of the currents i_1 and i_2 (with reference to Fig. 3.8.1).

In particular, it can be observed that, being the input current zero outside the conduction interval, the current through the first semi stage inductor (i_1) cannot be constantly equal and neither constantly greater than the tapped inductor primary side current (i_2), so that the auxiliary diode D_{A1} (with reference to Fig. 3.8.1) will consequently result to be necessary.

On the other hand, as concerns the other extra diode, the condition that has to be verified, in order to be allowed to remove D_{A2}, is that i_1 is constantly lower than i_2.

Keeping in mind (3.5.1), (3.5.3) and (3.5.4), such condition can be rewritten as:

$$v_I(t) < \frac{L_1}{\Lambda^2 \cdot L_2}\left[v_B(t) - v_O(t)\right] + v_B(t) \tag{3.8.1}$$

that, according to the values of Table 3.7.2, does not result to be verified in the whole line period.

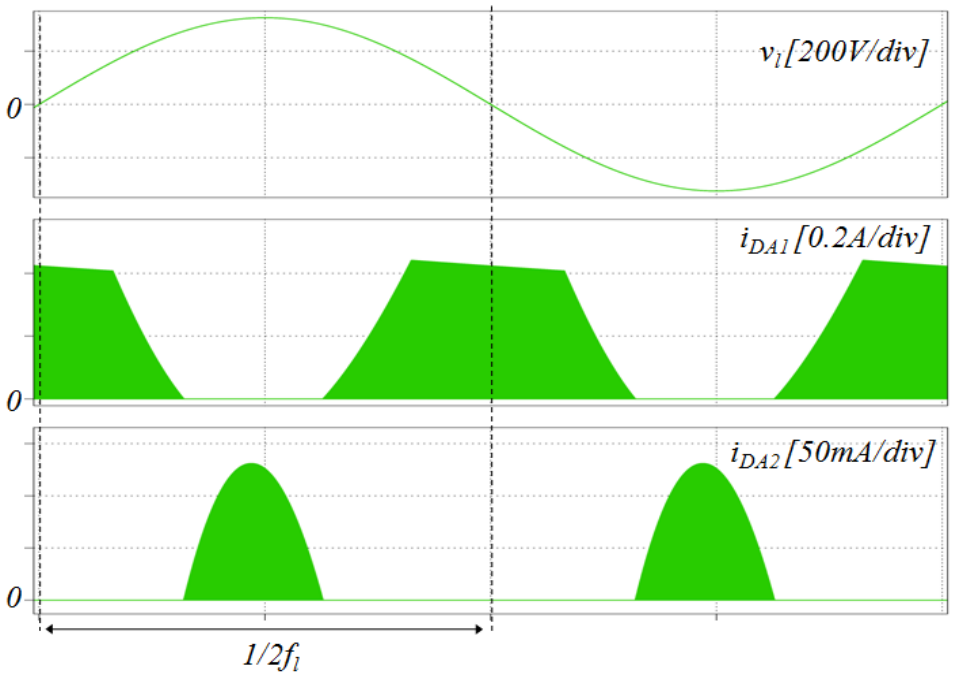


Fig. 3.8.4 - Waveforms of the auxiliary diodes current envelopes.

Consequently, it can be finally concluded that both auxiliary diodes will be needed, as also confirmed by the envelope waveforms of their currents reported in Fig. 3.8.4, so that none of the degenerated grafted switch forms, discussed at the end of paragraph 3.1, will actually suit the considered application.

Chapter 4

The Multiple Stage Approach

4.1 Introduction

In the previous chapters 2 and 3 have been investigated two different kinds of approach to address the offline driving of solid state technology based lamps.

The first one makes use of a very compact single stage structure, capable of guaranteeing compliance with the EN61000-3-2 standard while providing galvanic isolation and fine output current regulation. This kind of solution turns out to be very suitable in low power, cost effective applications, like for example the bulb replacement case, in which cost minimization and the obtainment of high power density levels are considered a major issue.

The second kind of solution investigated relies, instead, on the integration of two different conversion stages, obtained by grafting their main active controlled switches. The result is a simple, compact and reliable single stage topology, capable of guaranteeing power factor correction and output regulation while avoiding the use of electrolytic capacitors. This kind of approach results to be particularly suitable in low/medium power applications where good line side performance and high robustness of the overall driving system are mainly required, as for example in down lighting applications.

However, despite their simplicity, both the studied approaches appear to be unsuitable if high power levels applications are considered.
In this case, indeed, the suboptimal converter's design, characterizing the use of single stage topologies in offline applications, due to the large variation of converter's operating conditions, would strongly affect the electronic ballast behavior, with significant detrimental effects on converter efficiency, line side and load side performance.

4.1.1 Multi-Stage Power Supply Features

For high power applications (>60W), as in the case of street lighting, a multiple stage topology ([126]-[131]), seems therefore to be the best option, among all the suitable candidate configurations, thanks to the high flexibility guaranteed by the use of optimized topology both on line and on load side.
Moreover, galvanic isolation can also be provided, either by the input or by the output stage. In the former case, the PFC stage can be implemented through an isolated converter (e.g. a flyback topology), resulting in a standard two stage configuration. Alternatively, a non isolated converter (e.g. a boost topology) can be used in combination with an isolated DC-DC stage, operating in open loop with constant input/output voltage conversion ratio, in order to adjust the DC-link voltage to the level required by the output stage, as shown in Fig. 4.1.1.

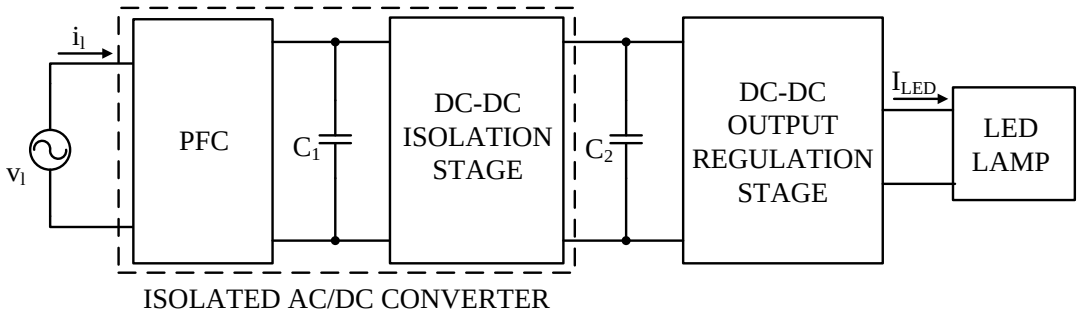


Fig. 4.1.1 - Offline LED lighting power supply configuration according to the multiple stage approach.

As it will be here discussed in the following paragraphs, such latter kind of structure, although characterized by a triple energy processing, actually turns out to be a very suitable solution, to match the considered application guidelines listed in Table 4.1.1, thanks to the high performance level guaranteed by each optimized stage.

Once a suitable overall converter configuration has been identified, it is worth making some considerations about the main issues concerning each different conversion stage, consequently discussing the most suitable solution for its implementation.
In particular, from line side perspective, the main goal is to achieve an almost unity power factor value, so that an ideal power factor correction stage, whose main features have been previously discussed in paragraph 3.2, can be used to effectively suit this purpose.
Such a solution can be easily implemented through the use of a non isolated step-up topology, such as a boost converter, preferably operated at constant switching frequency, with average current control and in continuous conduction mode, so as to be able to freely adjust the input current ripple in order to minimize its RMS value and guarantee excellent efficiency levels.

TABLE 4.1.1 - CONSIDERED APPLICATION'S SPECIFICATIONS

MAIN CONVERTER PARAMETERS		
NAME	SYMBOL	VALUE
Line input RMS voltage	V_{lRMS}	230V ± 20%
Line frequency	f_l	50Hz
Power Factor	PF	> 0.98
LED load current minimum value	I_{LEDmin}	0.75A
LED load current maximum value	I_{LEDmax}	1.5A
LED lamp threshold voltage	V_γ	120V
LED lamp series resistance	R_γ	12Ω
Overall converter efficiency	η	> 90%

With this solution, whose operation is utterly conventional, it is indeed possible to get an almost sinusoidal input current, by properly regulating the boost converter duty cycle, even without any input filter. As shown in Fig. 4.1.2, the sinusoidal reference for the input current is derived by multiplying a signal proportional to the rectified line voltage with a signal depending on the error between the boost output voltage and a proper reference, so as to guarantee the balance between the input and the output power.
As regards converter load side, output current regulation is required in order to guarantee a current level through the LEDs as close as possible to DC and provide light dimming capability, by varying the average level of the current supplied to the LED lamp. A DC-DC

converter can be therefore used to suit the objective of adjusting the output voltage of the transformer stage to the level required to properly feed the load.

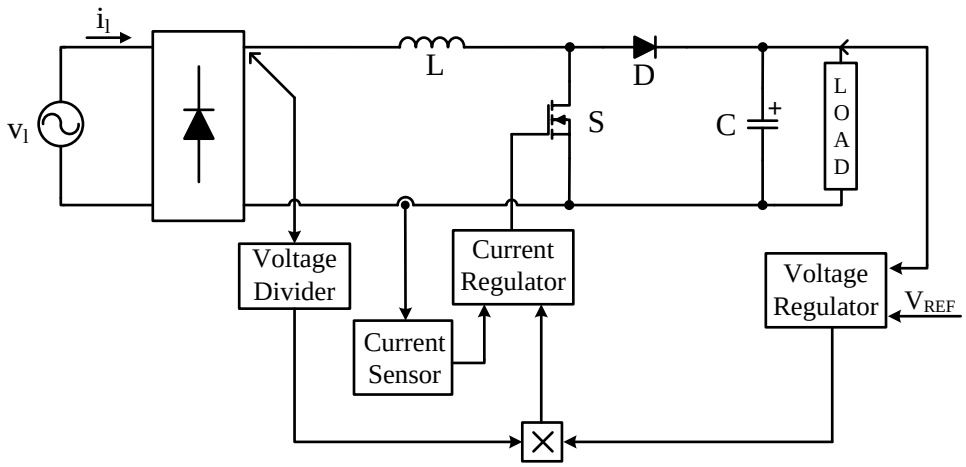


Fig. 4.1.2 - Basic scheme of a PFC boost with average current control.

For sake of compactness, the switching frequency of this stage should be kept conveniently high, namely in the range of the hundreds of kHz. As a consequence, in order to reduce switching losses and guarantee a high overall converter efficiency, the minimization of devices voltage stress will turn out to be a key aspect.

From this perspective, the most suitable option to perform LED current regulation, seems to be the use of a buck converter in the twin bus configuration ([132]), as shown in Fig. 4.1.3.

Such solution, indeed, significantly reduces the voltage stress on the active controlled switch and the freewheeling diode, allowing the use of optimized components, designed for lower nominal voltage levels and therefore offering better performance in terms of parasitic elements.

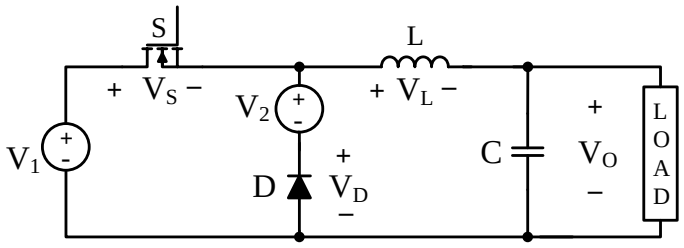


Fig. 4.1.3 - Basic scheme of the twin bus buck converter.

Continuous conduction can be assumed as operation mode, in order to minimize conduction losses. In such condition, as usual, two different intervals can be identified within the buck converter switching period.

Interval I

During the first phase the switch is turned-on, while the freewheeling diode is reverse biased:

$$V_D = V_1 - V_2 \tag{4.1.1}$$

so that the voltage across the filter inductance results to be:

$$V_L = V_1 - V_O \tag{4.1.2}$$

Interval II

When the switch is turned-off, the output filter inductor current recycles through the freewheeling diode, The voltage across the active switch will therefore be equal to:

$$V_S = V_1 - V_2 \tag{4.1.3}$$

while the voltage applied to the filter inductance results to be:

$$V_L = V_2 - V_O \tag{4.1.4}$$

Therefore, imposing, at steady state, the flux balance on the output filter inductor, the twin BUS buck input-output voltage relationship can be actually derived:

$$V_O = V_2 + (V_1 - V_2)\delta = V_1\delta + V_2(1-\delta) \tag{4.1.5}$$

where δ is the buck converter duty-cycle, so that LED current can be finally expressed as:

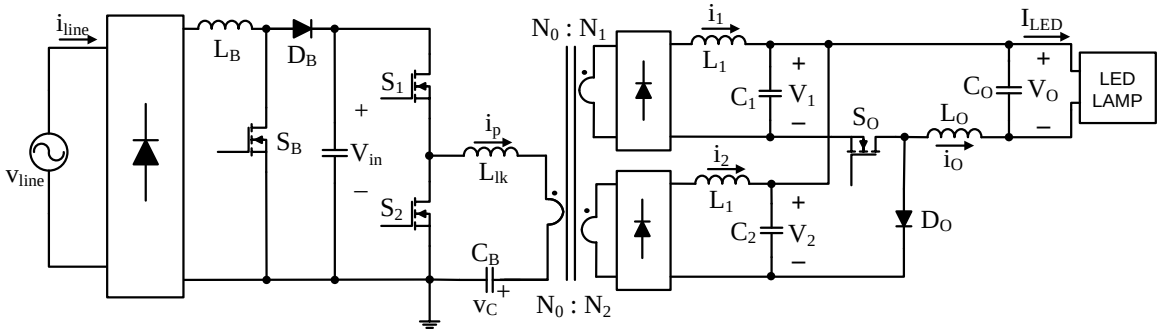
$$I_{LED} = \frac{V_O - V_\gamma}{R_\gamma} = \frac{V_2 - V_\gamma + (V_1 - V_2)\delta}{R_\gamma} \tag{4.1.6}$$

As it can be noticed from (4.1.1) and (4.1.3), thanks to the presence of a double input, the maximum voltage stress on the buck converter's switch and diode turns out to be equal to the difference between the two BUS voltage levels, that is inferior to that of a standard buck converter.

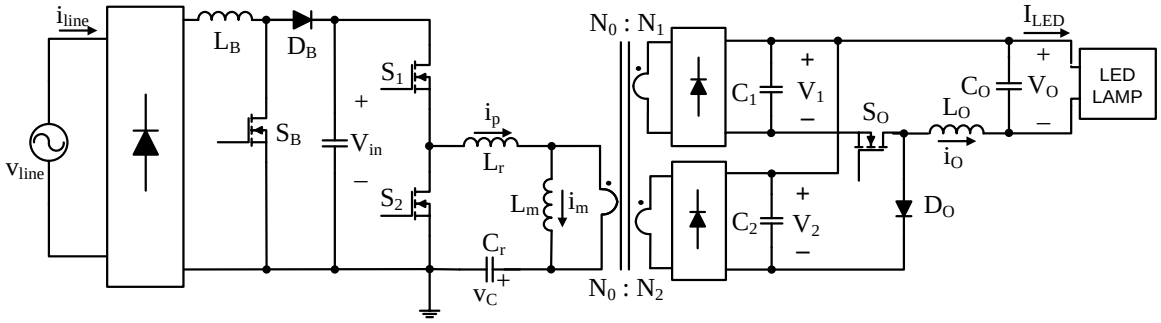
Finally, as concerns the DC-DC transformer stage, the purpose is to guarantee isolation and to adjust and split the DC-link voltage level, in order to feed the downstream placed twin BUS buck converter.

To this end, two different solutions can be taken into account: one involves the use of a half bridge converter ([133]-[137]), as shown in Fig. 4.1.4 (a), while the other relies on the use of a LLC resonant converter ([138]-[148]), as shown in Fig. 4.1.4 (b). In both cases, the half bridge switches are operated symmetrically with constant duty-cycle D=0.5,

except for a suitable dead time (Δt_d) introduced to prevent cross conduction and to allow soft switching operation.



(a)



(b)

Fig. 4.1.4 - Multiple stage electronic ballast implementation with (a) half bridge converter based isolation stage, (b) LCC resonant converter based isolation stage.

It is worth to note that the latter concern will be a major issue for this intermediate conversion stage. Indeed, due to the high BUS voltage level provided by the step-up input PFC stage, the achievement of zero voltage switching in the cascaded isolation stage actually results to be fundamentally important to get transformer volume minimization, through high frequency operation, while preventing detrimental effects on conversion efficiency.

The operation principles and the main aspects related to the soft switching issue of the DC-DC isolation stage will be carefully analyzed in the following for each solution, in order to highlight strengths and weaknesses of both options, namely the main goal of the research activity performed in this concern.

4.2 Half Bridge Converter

As previously mentioned, in order to understand pros and cons of the two different proposed solutions, it is worth to analyze first the operational principles of the DC-DC isolation stage in either case.

In particular, as concerns the solution represented in Fig. 4.1.4 (a), the behavior of the half bridge converter can be easily examined considering some simplifying preliminary assumptions.

Namely, all devices will be considered to be ideal, except for transformer leakage inductance (L_r); the magnetizing inductance value will be, instead, assumed ideally infinite and its effects will be neglected.

Moreover, the DC blocking capacitor (C_B) will be considered large enough so as to neglect its voltage ripple, as also any kind of resonance effect with the transformer's leakage inductance (i.e.: $v_C(t)=V_C=V_{in}/2$).

In addition, the leakage inductance will be assumed to be much smaller than the outputs' filter inductors (L_1 and L_2), which are supposed to continuously conduct the output currents.

Finally, the voltage on the input and output filter capacitors (C_{in}, C_1 and C_2) will be considered almost constant within the whole switching period while the half bridge MOSFETs switching transients will be neglected, postponing the discussion of the zero voltage switching issue to the next paragraphs.

The simplified scheme of the half bridge converter, obtained under such assumption, is reported in Fig. 4.2.1 (a), together with its equivalent single output circuit of Fig. 4.2.1 (b), in which the two outputs have been paralleled.

In particular, if the second output is paralleled to the first one, the following relations will hold:

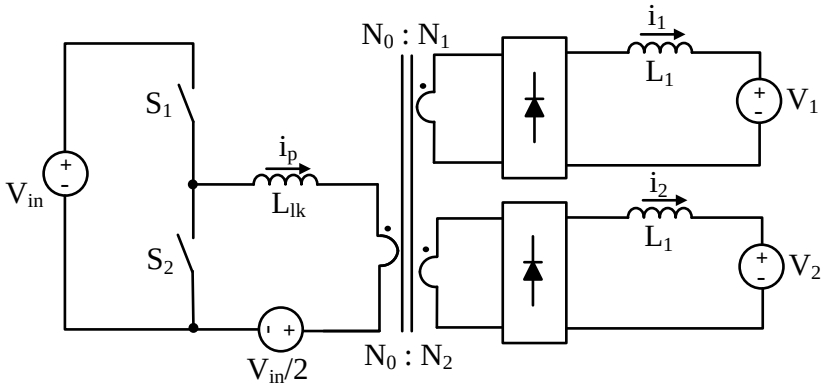
$$N_{eq} = N_1 \tag{4.2.1}$$

$$V_{eq} = V_1 = V_2 \frac{N_1}{N_2} \tag{4.2.2}$$

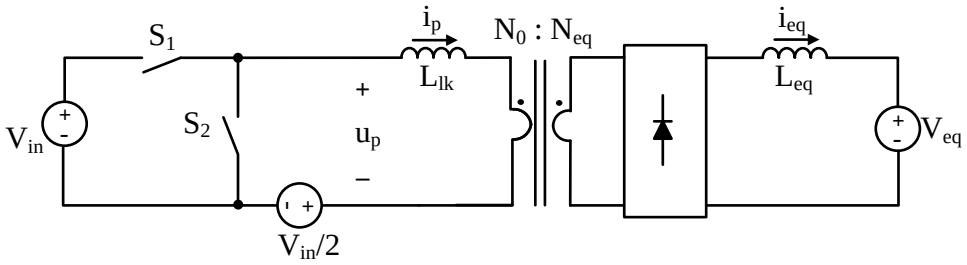
$$L_{eq} = \frac{L_1 L_2 (N_1 / N_2)^2}{L_1 + L_2 (N_1 / N_2)^2} \tag{4.2.3}$$

$$i_{eq}(t) = i_1(t) + i_2(t) \frac{N_2}{N_1} \tag{4.2.4}$$

where N_1 and N_2 are the numbers of turns of the first and of the second transformer secondary winding, respectively.



(a)



(b)

Fig. 4.2.1 - Half bridge converter simplified scheme: (a) with double output BUS voltages (b) equivalent single output scheme.

With reference to the equivalent circuit of Fig. 4.2.1 (b), keeping in mind the assumptions made, the half bridge converter operation can be divided into four different intervals within the switching period, depending on the state of the half bridge switches and of the secondary side rectifier diodes.

Interval I [t_0, t_1]

During the first interval the switch S_1 is turned-on while the ground switch S_2 is turned-off, so that the equivalent circuit reported at transformer's primary side will be that of Fig. 4.2.2 (a).

In such situation the primary voltage results to be equal to half the input voltage:

$$u_p(t) = V_{in} - V_c = \frac{V_{in}}{2} \tag{4.2.5}$$

while transformer primary side current is linearly increasing:

$$i_p(t) = \frac{N_{eq}}{N_0} i_{eq}(t) = \frac{N_{eq}}{N_0} I_{eq\min} + \frac{u_p(t) - V'_{eq}}{L_{lk} + L'_{eq}} t \tag{4.2.6}$$

where $I_{eq\min}$ is the valley value of the output current i_{eq} (with reference to Fig. 4.2.3) and:

$$V'_{eq} = V_{eq} \cdot \frac{N_0}{N_{eq}}, \qquad L'_{eq} = L_{eq} \cdot \left(\frac{N_0}{N_{eq}} \right)^2 \tag{4.2.7}$$

Interval II [t_1, t_2]

As soon as S_1 is turned-off and S_2 is turned-on the voltage applied to transformer primary side inverts polarity:

$$u_p(t) = -V_C = -\frac{V_{in}}{2} \tag{4.2.8}$$

however the inductive current at primary side cannot abruptly change its direction.
As a results, all secondary side full wave rectifier diodes will be simultaneously forward biased, producing a short circuit at transformer's secondary side, as shown in Fig. 4.2.2 (b), and a mismatch between the output filter inductor current (i_{eq}) and the rectified primary current reflected to the secondary side ($|i_p| \cdot N_0/N_{eq}$):

$$i_{eq}(t) = I_{eq\max} - \frac{V_{eq}}{L_{eq}} (t - t_1) \tag{4.2.9}$$

$$i_p(t) = \frac{N_{eq}}{N_0} I_{eq\max} - \frac{V_{in}}{2L_{lk}} (t - t_1) \tag{4.2.10}$$

where $I_{eq\ max}$ is the peak value of the output current (i_{eq}), as shown Fig. 4.2.3.
A detailed description of the switching transient will be provided in the following in paragraph 4.4, in which the issues related to the achievement of soft switching operation will be carefully analyzed.
The consequence of transformer windings short circuit is an idle interval, whose duration depends on the input voltage level (V_{in}), the transformer design (N_0, N_1, N_2, L_{lk}) and the average value of the output current (I_{eq}):

$$T_{idle} = \frac{N_{eq}}{N_0} \frac{(I_{eq\max} + I_{eq\min}) L_{lk}}{V_C} = \frac{N_{eq}}{N_0} \cdot \frac{4 L_{lk} I_{eq}}{V_{in}} \tag{4.2.11}$$

From (4.2.11), the peak to peak ripple of the equivalent output current can be therefore computed as:

$$\Delta i_{eq} = \frac{V_{eq}}{L_{eq}} T_{idle} = \frac{V_{eq}}{L_{eq}} \cdot \frac{N_{eq}}{N_0} \cdot \frac{4 L_{lk} I_{eq}}{V_{in}} \tag{4.2.12}$$

so that its boundary values result to be:

$$i_{eq}(t_1) = I_{eq\max} = I_{eq} + \frac{\Delta i_{eq}}{2} = I_{eq} \cdot \left[1 + 2 \cdot \frac{N_{eq}}{N_0} \cdot \frac{V_{eq}}{V_{in}} \cdot \frac{L_{lk}}{L_{eq}} \right] \tag{4.2.13}$$

$$i_{eq}(t_2) = I_{eq\min} = I_{eq} - \frac{\Delta i_{eq}}{2} = I_{eq} \cdot \left[1 - 2 \cdot \frac{N_{eq}}{N_0} \cdot \frac{V_{eq}}{V_{in}} \cdot \frac{L_{lk}}{L_{eq}} \right] \tag{4.2.14}$$

and, consequently, the peak value of the primary current will be:

$$i_p(t_1) = I_{p\max} = \frac{N_{eq}}{N_0} I_{eq\max} = \frac{N_{eq}}{N_0} \cdot I_{eq} \cdot \left[1 + 2 \cdot \frac{N_{eq}}{N_0} \cdot \frac{V_{eq}}{V_{in}} \cdot \frac{L_{lk}}{L_{eq}} \right] \tag{4.2.15}$$

Interval III [t_2, t_3]

When, in $t_2 = t_1 + T_{idle}$, the condition:

$$i_{eq}(t_2) = \left| i_p(t_2) \right| \frac{N_0}{N_{eq}} \tag{4.2.16}$$

is verified, the idle interval ends and the input power restarts to be transferred to transformer secondary side.

As it can be noticed, observing the corresponding topological stage reported shown in Fig. 4.2.2 (c) and the waveforms reported in Fig. 4.2.3, during this phase the primary current results to be totally symmetrical to that of the first interval previously analyzed:

$$i_p(t) = -\frac{N_{eq}}{N_0} i_{eq}(t) = -\frac{N_{eq}}{N_0} I_{eq\min} - \frac{u_p(t) - V'_{eq}}{L_{lk} + L'_{eq}} \left(t - t_2 \right) \tag{4.2.17}$$

where L'_{eq} and V'_{eq} have been defined in (4.2.7).

Interval IV[t_3, t_4]

When S_1 is turned-on and S_2 is turned-off, the voltage applied to transformer primary side inverts polarity once again (Fig. 4.2.2 (d)):

$$u_p(t) = V_C = \frac{V_{in}}{2} \tag{4.2.18}$$

so that, for the same reasons previously mentioned, another idle interval will occur.

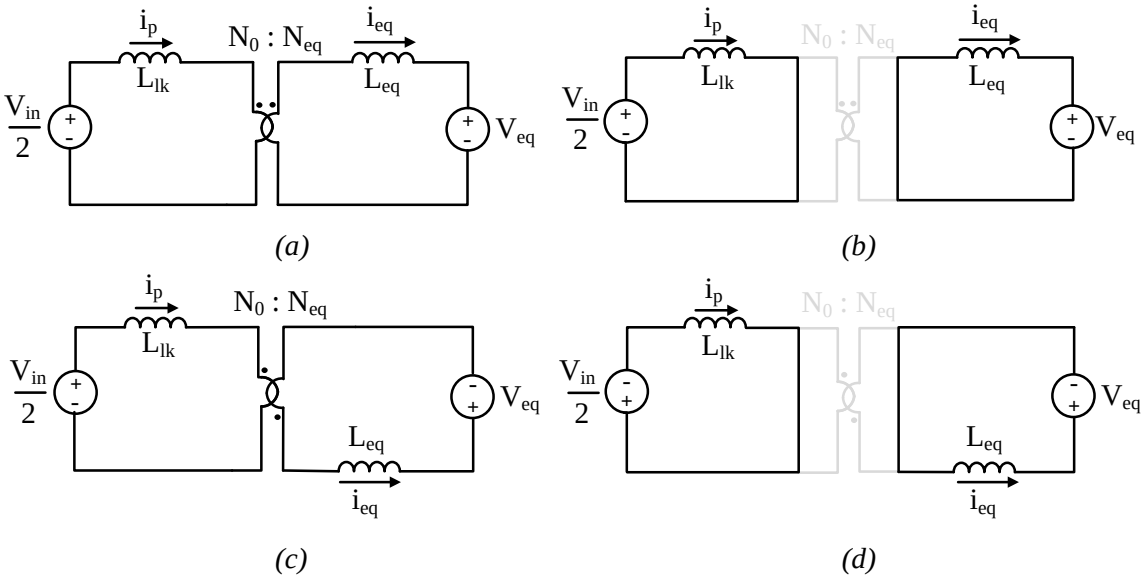


Fig. 4.2.2 - Half bridge converter simplified schemes corresponding to the topological intervals: (a) I, (b) II, (c) III, (d) IV, occurring within the switching period.

During such interval, symmetrically to the formerly analyzed idle time, the primary side current linearly increases and changes its direction:

$$i_p(t) = -\frac{N_{eq}}{N_0} I_{eq\max} + \frac{V_{in}}{2L_{lk}}(t - t_3) \tag{4.2.19}$$

while the output current linearly decreases, under to the effect of the output voltage:

$$i_{eq}(t) = I_{eq\max} - \frac{V_{eq}}{L_{eq}}(t - t_3) \tag{4.2.20}$$

until, in $t_4 = t_1 + T_{sw}$, the primary current reflected to the secondary side ($|i_p| N_0/N_{eq}$) matches the output current once again and another switching period can start.

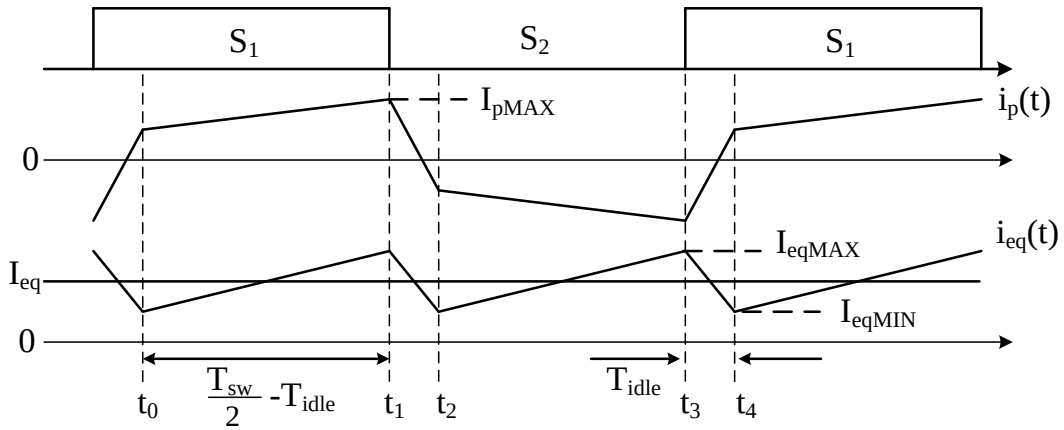


Fig. 4.2.3 - Single output half bridge converter primary side and output current waveforms.

From (4.2.6) and (4.2.17), the expression of the output equivalent current ripple, in correspondence of the first and third intervals, can be written as:

$$\Delta i_{eq} = I_{eqMAX} - I_{eqMIN} = \frac{\left(\frac{V_{in}}{2}\cdot\frac{N_{eq}}{N_0} - V_{eq}\right)}{L_{lk}\frac{N_{eq}^2}{N_0^2} + L_{eq}}\cdot\left(\frac{T_{sw}}{2} - T_{idle}\right) \simeq \frac{\left(\frac{V_{in}}{2}\cdot\frac{N_{eq}}{N_0} - V_{eq}\right)}{L_{eq}}\cdot\left(\frac{T_{sw}}{2} - T_{idle}\right) \tag{4.2.21}$$

where the value of the leakage inductance, reported at transformer secondary side, has been considered negligible if compared to the output equivalent inductance.

Now, keeping in mind the expression (4.2.12), related to the same ripple, but derived in correspondence of the idle intervals, the flux balance across the output equivalent filter inductance (L_{eq}) can be written as:

$$\left(\frac{V_{in}}{2}\cdot\frac{N_{eq}}{N_0} - V_{eq}\right)\cdot\left(\frac{T_{sw}}{2} - T_{idle}\right) = V_{eq}\cdot T_{idle} \tag{4.2.22}$$

So, imposing (4.2.22) to be verified in steady state conditions, the expression of the input-output voltage conversion ratio of the converter under study can be derived:

$$M = \frac{V_O}{V_{in}} = \frac{1}{2}\cdot\frac{N_{eq}}{N_0}\cdot\left(1 - 2\frac{T_{idle}}{T_{sw}}\right) = \frac{1}{2}\cdot\frac{N_{eq}}{N_0}\cdot\left(1 - \frac{N_{eq}}{N_0}\cdot\frac{8 f_{sw} L_{lk}}{V_{in}} I_{eq}\right) \tag{4.2.23}$$

As it can be noticed, once fixed by design all converter parameters involved in the formula, given the input voltage level, converter output voltage will actually result to be load dependent.

4.3 LLC Resonant Converter

As concerns the solution involving the use of the LLC topology to implement the DC-DC isolation stage, the resonant converter is supposed to operate in open loop with fixed switching frequency, in order to provide a constant conversion ratio between the DC-link and the two output voltage levels.

Also in this case, for sake of simplicity, all converter devices will be assumed to be ideal except for transformer leakage and magnetizing inductances, that in the LLC converter play both a fundamental role, as it will be discussed in the following paragraphs.

Moreover, the ripple on the input and output voltages will be neglected, as well as the switching transients of the half bridge switches.

The resulting simplified circuit is shown in Fig. 4.3.1, together with the equivalent single output scheme where the second output has been paralleled to the first one, so that the relations (4.2.1), (4.2.2) and (4.2.4) still hold.

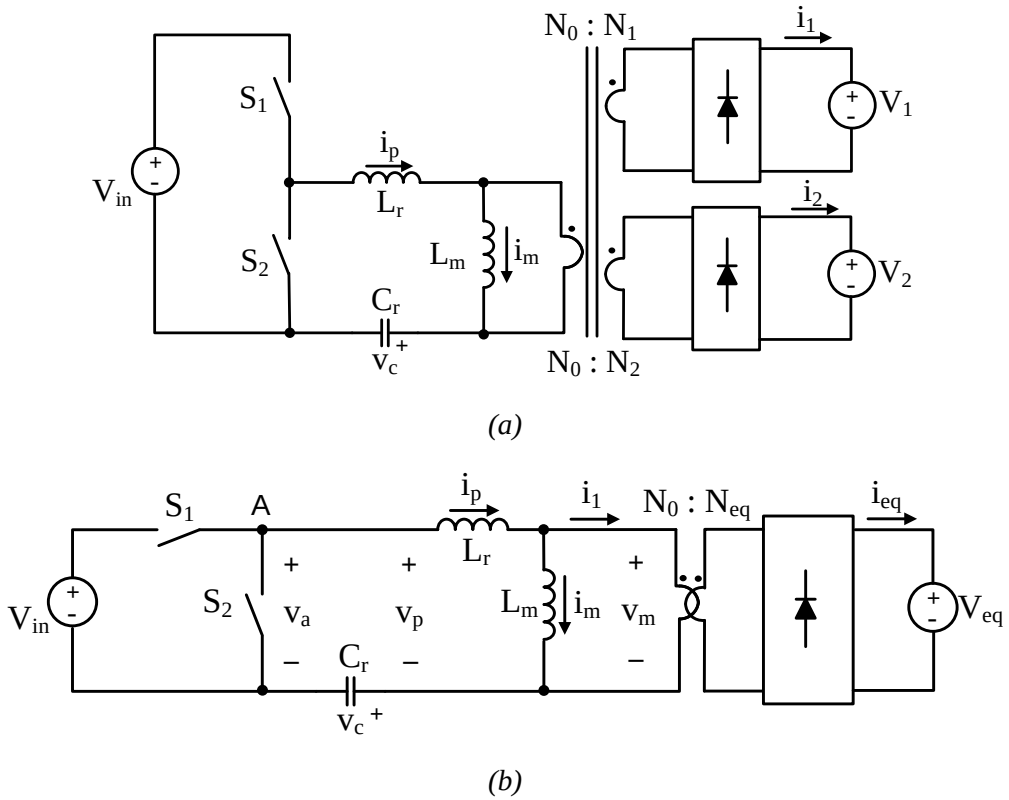


Fig. 4.3.1 - LLC resonant converter simplified scheme: (a) with double output BUS voltages (b) equivalent single output scheme.

In order to maximize the transformer's primary to secondary side energy transfer interval, avoid any rectifier diode recovery issue and prevent load dependence of the input-output voltage transfer function, the switching frequency value can be conveniently chosen to be equal to the resonant tank's series resonance frequency:

$$f_{sw} = f_r = (2\pi\sqrt{L_r C_r})^{-1} \tag{4.3.1}$$

In such situation, the main component of the current circulating at transformer primary side will be exactly at this frequency so that the resonant current will be almost purely sinusoidal (Fig. 4.3.4). Therefore, an approximation, involving the fundamental harmonic of the input square wave voltage, while ignoring all higher order harmonics, can be done. Through the analysis performed according to this approximation method, known as the First Harmonic Approximation (FHA) technique ([149]), it is indeed possible to get very accurate results, as long as the converter is operated at resonance.

The equivalent circuit of the LLC resonant converter, that is obtained according to the first harmonic approximation, is shown in Fig. 4.3.2. The following relations (4.3.2)-(4.3.5), with the electrical variables of the original converter, shown in Fig. 4.3.1 (b), hold.
In particular: as concerns voltage approximations, the fundamental components, of the input square voltage and of the output equivalent voltage reflected at primary side, can be written respectively as:

$$v_{aFH}(t) = \frac{4}{\pi} \cdot \frac{V_{in}}{2} \cdot \sin(2\pi f_{sw} t) = \frac{2}{\pi} V_{in} \cdot \sin(2\pi f_{sw} t) \tag{4.3.2}$$

$$v_{oFH}(t) = \frac{4}{\pi} \cdot V_{eq} \cdot \frac{N_0}{N_{eq}} \cdot \sin(2\pi f_{sw} t - \phi) \tag{4.3.3}$$

where ϕ represents the phase shift of the output voltage fundamental harmonic with respect to that of the input square voltage.

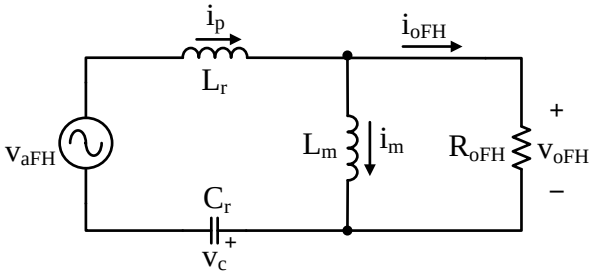


Fig. 4.3.2 - Equivalent circuit, according to first harmonic approximation, of the LLC resonant converter.

Moreover, being the fundamental harmonic of the square wave voltage on transformer magnetizing inductance (v_m Fig. 4.3.1) in phase with the fundamental of the equivalent output current, reflected at transformer primary side, (i_1 in Fig. 4.3.1), the latter can be can be actually expressed as:

$$i_{oFH}(t) = \frac{\pi}{2} \cdot \frac{N_{eq}}{N_0} \cdot I_{eq} \cdot \sin(2\pi f_{sw} t - \phi) \tag{4.3.4}$$

where I_{eq} is the average value of the equivalent output current.

As a consequence, the output equivalent load (R_{oFH} in Fig. 4.3.2) results to be purely resistive and its expression can be finally derived as the ratio between the RMS values of load voltage (4.3.3) and current (4.3.4) sinusoids:

$$R_{oFH} = \frac{\frac{2\sqrt{2}}{\pi} \cdot V_{eq} \cdot \frac{N_0}{N_{eq}}}{\frac{\pi}{2\sqrt{2}} \cdot \frac{N_{eq}}{N_0} \cdot I_{eq}} = \frac{8}{\pi^2} \cdot \frac{V_{eq}}{I_{eq}} \cdot \left(\frac{N_0}{N_{eq}} \right)^2 \tag{4.3.5}$$

By observing Fig. 4.3.2, considering the normalized quantities $f_n=f_{sw}/f_r$ and $L_n=L_m/L_r$, the voltage conversion ratio can be expressed as:

$$M_g = \frac{V_{oFH}}{V_{aFH}} = \left| \frac{f_n^{\,2} L_n}{[(L_n+1) f_n^{\,2} - 1] + j[(f_n^{\,2} - 1) f_n Q_e L_n]} \right| \tag{4.3.6}$$

in which V_{pFH} and V_{oFH} are the RMS values of (4.3.2) and (4.3.3), respectively, while

$$Q_e = \frac{\sqrt{(L_r / C_r)}}{R_{oFH}} \tag{4.3.7}$$

is the quality factor of the resonant tank.

As reference, the plot of the magnitude of the input-output voltage transfer function (M_g), (computed for typical values of L_n and Q_e, related to the application under study) is reported in Fig. 4.3.3 as a function of the normalized frequency in correspondence of three different load conditions, within the lamp dimming range. Namely: 100% (continuous red trace), 75% (dotted blue trace) and 50% (dashed black trace) of the nominal load.

As it can be noticed, at resonance (i.e. f_n=1), the gain of the resonant tank is unity independently of the load level.

Consequently, also the voltage conversion ratio (M) between the DC-link voltage (V_{in}) and the equivalent output voltage level (V_{eq}):

$$M = \frac{V_{eq}}{V_{in}} = \frac{1}{2}\frac{N_{eq}}{N_0} M_g(f_n)\Big|_{f_n=1} = \frac{N_{eq}}{2N_0} \tag{4.3.8}$$

will result to be load independent.

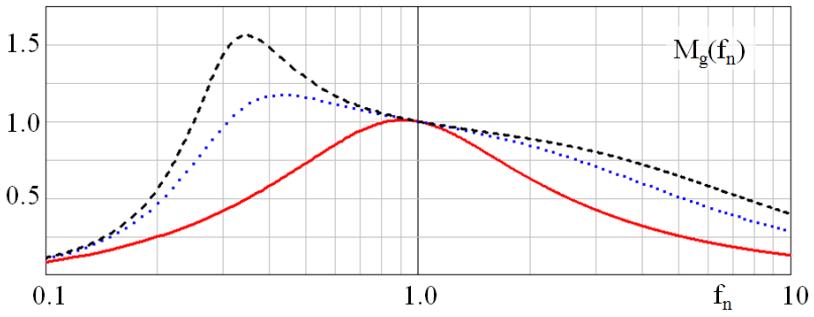


Fig. 4.3.3 - Magnitude of the resonant tank input-output voltage transfer function for three different load conditions; i.e. 100% (continuous trace), 75% (dotted trace) and 50% (dashed trace) of the maximum load current.

Keeping in mind the results of the analysis performed according to the FHA, it is worth to focus on another important electrical variable that has been so far left aside and that, however, plays a relevant role, as it will be explained in the following paragraph, namely the magnetizing current.

To this end, the analysis in the time domain of the LLC resonant converter can be easily performed in correspondence of the selected operating frequency.

At resonance, the secondary side rectifier diodes operate at the boundary between continuous and discontinuous conduction mode and their commutations result to be in phase with those of the half bridge.

In such condition, if switching transients are neglected, two different intervals can be identified within the switching period, respectively corresponding to the conduction time of one or the other of the half bridge switches. The corresponding equivalent topological stages are reported in Fig. 4.3.4 (a) and (b).

Interval I [0,T_{sw}/2]

During the first interval the switch S_1 is turned-on while S_2 is turned-off, so that the voltage applied to the transformer primary side will be positive and equal to:

$$v_p(t) = \left(V_{in} - v_C(t)\right) \tag{4.3.9}$$

In such condition, the voltage across the magnetizing inductance is clamped at the level corresponding to the output equivalent voltage reflected to transformer primary side, so that the current that is recycling through it will be linearly rising:

$$i_m(t) = \frac{N_0}{N_{eq}} \frac{V_{eq}}{L_m} (t - \frac{T_{sw}}{4}) = \frac{V_{in}}{2L_m} (t - \frac{T_{sw}}{4}) \tag{4.3.10}$$

Interval II [$T_{sw}/2$, T_{sw}]

When S_1 is switched-off and S_2 is switched-on, the converter input is disconnected from the DC-link, so that the voltage applied to transformer primary side results to be:

$$v_p(t) = -v_C(t) \tag{4.3.11}$$

During this second interval, the voltage across the magnetizing inductance will be clamped at the opposite of the converter output equivalent voltage value reflected at transformer's primary side. The resulting magnetizing current will be therefore linearly decreasing, as shown in the waveforms of Fig. 4.3.4 (c), according to the following expression:

$$i_m(t) = -\frac{N_0}{N_{eq}} \frac{V_{eq}}{L_m} (t - \frac{3T_{sw}}{4}) = \frac{V_{in}}{2L_m} (\frac{3T_{sw}}{4} - t) \tag{4.3.12}$$

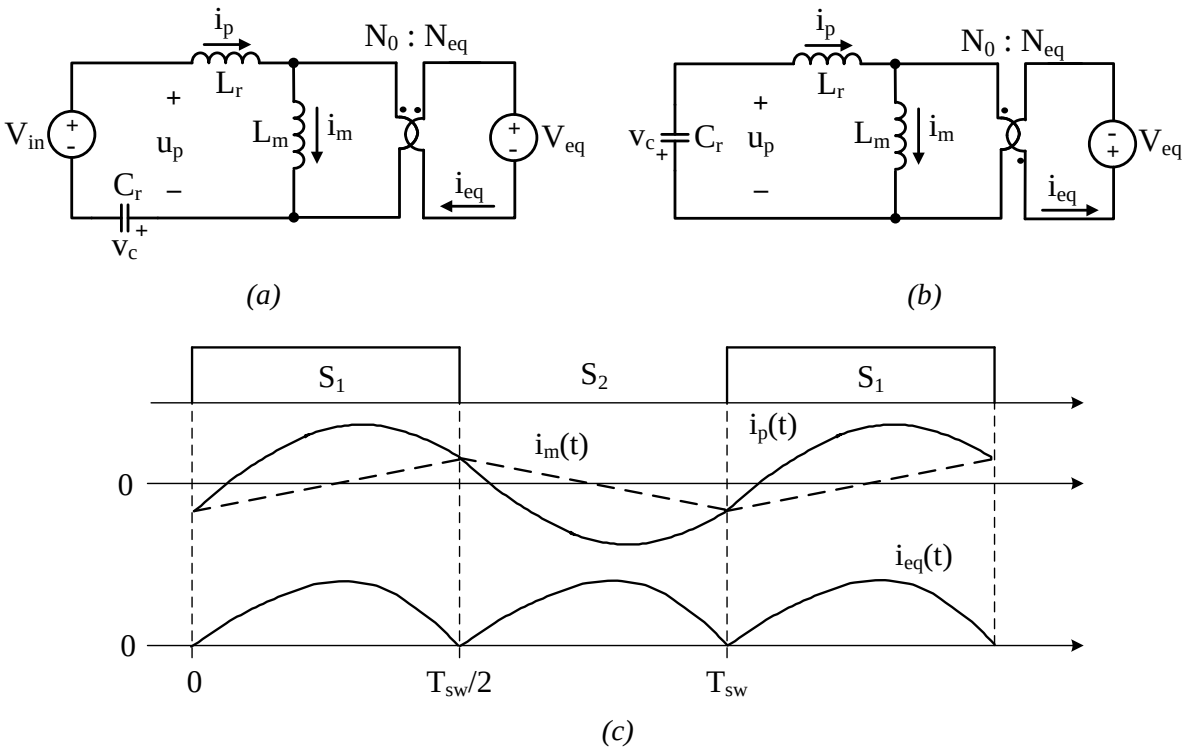


Fig. 4.3.4 - LLC converter topological stages corresponding to the (a) first and (b) second interval; (c) primary side and output current waveforms.

It is worth to note that, in order to derive the second equalities in (4.3.10) and (4.3.12), it has been exploited the relation (4.3.8), that was computed through the FHA analysis.
However the time domain analysis of the original converter (Fig. 4.3.1) performed in correspondence of the resonance frequency actually reveals that this relation still exactly holds as far as the operation at resonant frequency is considered.
The role of the magnetizing current in favoring soft switching transients of the half bridge switches will be investigated in the next paragraph that is entirely dedicated to the analysis of such issue.

4.4 The Soft Switching Issue

As previously discussed, due to the high voltage BUS level provided by the input power factor correction stage, the achievement of zero voltage switching is a fundamental concern for the cascaded DC-DC isolation stage, in order to allow transformer volume minimization through high switching frequency operation, without significantly affecting converter efficiency.

In order to understand the main design issues deriving from the need of guaranteeing soft commutations of the half bridge switches, it is worth to carefully analyze the behavior of both the topologies proposed to implement the isolation stage, during the switching transients dead times.

Half Bridge Converter

As concerns the implementation involving the use of the half bridge converter, considering the transient interval elapsing between the turn-off of the DC-link connected switch (S_1) and the turn-on of the ground switch (S_2), three different intervals can be identified.

It is worth to note that, as previously assumed in the analysis performed in paragraph 4.2, also in this case converter DC- blocking and output capacitors will be considered large enough so as to neglect their voltage ripple. For sake of simplicity, in the upcoming analysis, they will be therefore modeled as constant voltage sources.

Interval A [t_A, t_B]

As soon as the switch S_1 is turned-off, the equivalent output current, reflected to transformer primary side, starts charging the output parasitic capacitance of the DC-link connected switch and discharging that of the ground switch, as shown in Fig. 4.4.1.

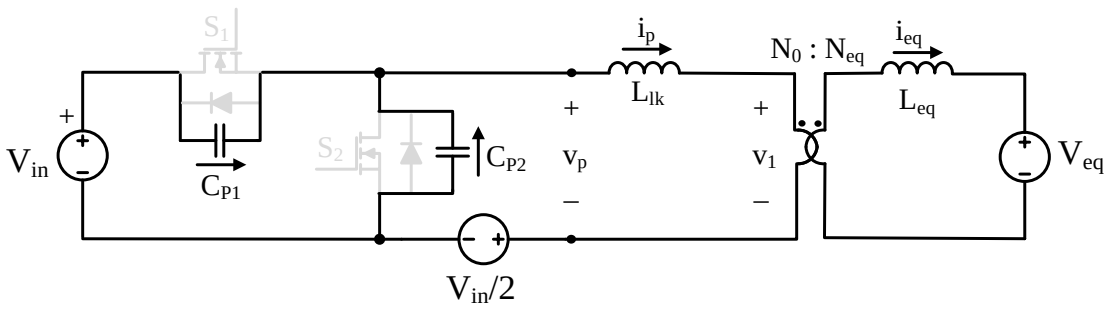


Fig. 4.4.1 - HB converter: first topological stage characterizing the ground switch soft turn-on transient.

As it can be noticed, this phase is characterized by a resonant network involving the series between transformer leakage inductance and output equivalent filter inductance (reflected at transformer primary side) and the parallel of the half bridge switches parasitic capacitances.

Considering the typical values of such parameters characterizing the application under study, the resulting resonance period:

$$T_{rA} = 2\pi\sqrt{\left[L_{lk} + L_{eq}\left(\frac{N_0}{N_{eq}}\right)^2\right]\cdot\left(C_{P1} + C_{P2}\right)} \tag{4.4.1}$$

can be reasonably supposed to be much longer than the transient dead time elapsing between the switches conduction intervals (Δt_d).

Under such hypothesis, the charge/discharge process during this phase can be therefore assumed to be performed at almost constant current, as shown in Fig. 4.4.4:

$$i_p(t) \simeq i_p(t_A) \simeq I_{p\max} \tag{4.4.2}$$

where the peak value of the primary current can be accurately approximated with that computed in (4.2.15).

When, at the instant t_B, the transformer secondary side voltage reaches zero, that is:

$$v_p(t_B) = L_{lk}\left.\frac{\partial i_p(t)}{\partial t}\right|_{t_B} \simeq 0 \tag{4.4.3}$$

where the simplifying assumption of almost constant primary current has been exploited, the non conducting diodes of the output rectifier become forward biased.

However, being the inductive primary side current direction still the same, as a result all rectifier diodes will be consequently forced to simultaneous conduction, so that transformer windings will result to be short circuited.

The same non linear model, already used in chapter 2 for the analysis of the asymmetrical half bridge flyback converter, can be considered for both MOSFETs' parasitic capacitances:

$$C_{P1}(v) = C_{P2}(v) = C_P(v) = C_{Px}\sqrt{\frac{V_x}{v}} \tag{4.4.4}$$

(where C_{Px} is the MOSFET's output capacitance, measured at the voltage V_x provided by the device datasheet). In such condition, the total amount of energy involved in the voltage

transition of switches output parasitic capacitances, during this first phase, actually results to be:

$$\Delta E_1 = \int_0^{V_{in}/2} C_{P1}(v) \cdot v \; dv + \left| \int_{V_{in}}^{V_{in}/2} C_{P2}(v) \cdot v \; dv \right| = \frac{2}{3} \cdot C_P(V_{in}) \cdot V_{in}^2 \qquad (4.4.5)$$

Interval B [t_B, t_C]

Due to transformer windings short circuit, during the second phase, converter primary and output currents recycle at transformer primary and secondary side, respectively, as shown in Fig. 4.4.2.

In particular, while the output current is linearly decreasing under the effect of the output voltage on the output filter inductor, at primary side, the leakage inductance resonates with the half bridge switches parasitic capacitances with a resonance frequency:

$$f_{rB} = \frac{1}{2\pi\sqrt{L_{lk}\left(C_{P1} + C_{P2}\right)}} \qquad (4.4.6)$$

much higher than that characterizing the previous interval (keeping in mind the assumptions $L_1 >> L_{lk}$ and $L_2 >> L_{lk}$ previously made at the beginning of the analysis of paragraph 4.2).

In such phase the primary current reflected to transformer secondary side and the output current result to be mismatched, being the current difference carried by the rectifier diodes.

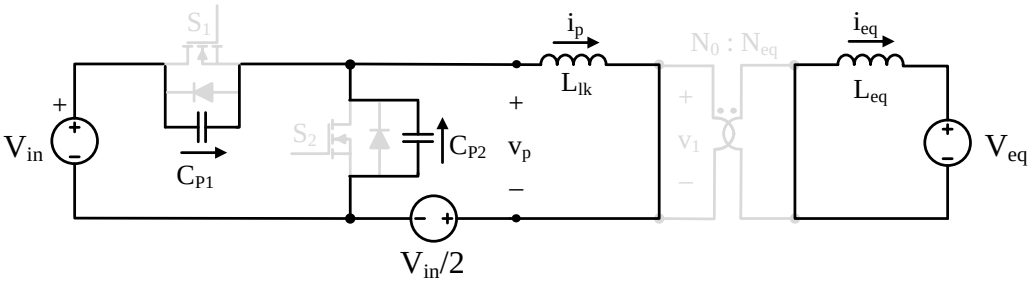


Fig. 4.4.2 - HB converter: second topological stage characterizing the ground switch soft turn-on transient.

In order to allow the primary resonant current to accomplish the soft switching process, the energy stored in the transformer leakage inductance, at the beginning of this interval, must be greater or equal than that necessary to complete the voltage transition of switches output parasitic capacitances:

$$\Delta E_2 = \frac{1}{2} L_{lk} i_p^2(t_B) \simeq \frac{1}{2} L_{lk} I_{p\max}^2 > \int_{V_{in}/2}^{V_{in}} C_{P1}(v) \cdot v \; dv + \left| \int_{Vin/2}^{0} C_{P2}(v) \cdot v \; dv \right| = \frac{2}{3} \cdot C_p(V_{in}) \cdot V_{in}^2 \qquad (4.4.7)$$

Interval C [t_C, t_D]

If (4.4.7) is verified, the voltage across the ground switch will be effectively taken to zero, forward biasing its body diode that will therefore start conducting the whole converter primary current. In such situation, whose corresponding topological stage is shown in Fig. 4.4.3, the primary current decreases linearly, while the primary voltage is clamped at zero. So, at the instant t_D, the ground switch can be turned-on at zero voltage, before the primary current reverses its direction, as shown in Fig. 4.4.4.

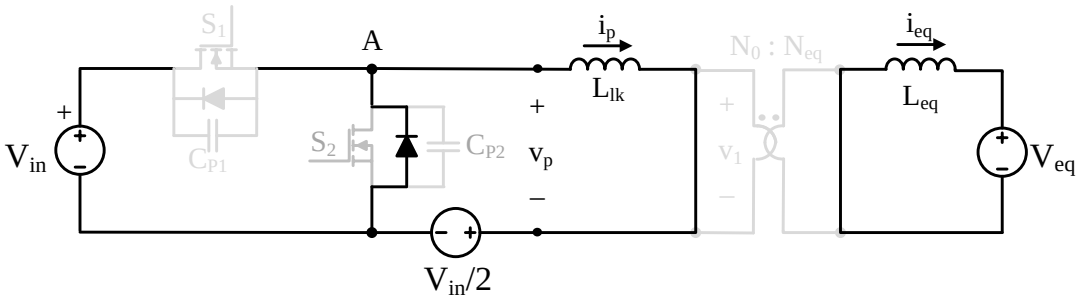


Fig. 4.4.3 - HB converter: third topological stage characterizing the ground switch soft turn-on transient.

As it can be noticed, substituting (4.2.15) in (4.4.7) the condition for zero voltage switching can be rewritten as:

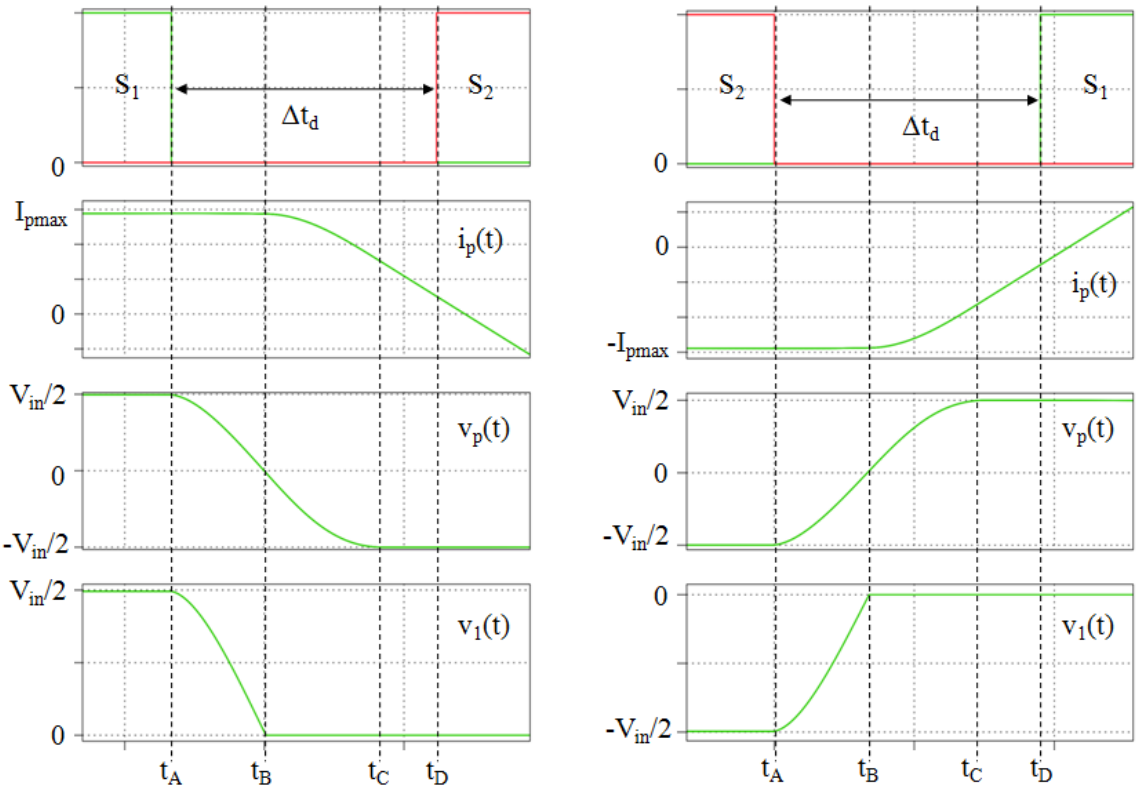
$$I_{eq} > \sqrt{\frac{\frac{4}{3}\cdot C_p(V_{in})\cdot V_{in}^2}{L_{lk}\cdot\left(\frac{N_{eq}}{N_0}\right)^2\cdot\left[1+2\cdot\frac{N_{eq}}{N_0}\cdot\frac{V_{eq}}{V_{in}}\cdot\frac{L_{lk}}{L_{eq}}\right]^2}} \tag{4.4.8}$$

from which, it can be finally concluded that, once fixed all converter parameters by design, the half bridge topology can be operated in soft switching only above a given load current level.

In the analysis performed, the discussion has been focused on the turn-on transient of the half bridge ground connected switch. However, the other switching interval, involving the turn-on of the DC-link connected switch, will be exactly symmetrical to the one just described.

As reference can be considered the current and voltage waveforms shown in Fig. 4.4.4, obtained simulating the half bridge converter behavior in PLECS® software platform, assuming for the switches parasitic capacitances the non linear model described by (4.4.4).

It is worth to note that the maximum dead time value is actually constrained by the need of guaranteeing that the switch is effectively turned-on before the primary current reverses its direction.



(a) *(b)*

Fig. 4.4.4 - Waveforms characterizing the soft turn-on of the half bridge's (a) ground connected and (b) DC-link connected switch.

LLC Resonant Converter

As concerns the LLC resonant converter, focusing on the turn-on transient of the ground switch S_2, four different topological intervals can be identified.

Interval A [t_A, t_B]

When the DC-link connected switch (S_1) is turned-off, the LLC converter resonant current starts discharging the output parasitic capacitances of the half bridge MOSFETs. The corresponding topological stage is represented in Fig. 4.4.5. As it can be noticed, the magnetizing inductance voltage is clamped at the output equivalent voltage level reflected to transformer primary side.

In the resulting resonant network the LLC resonant capacitor (C_r) is in series with the parallel (according to Thévenin equivalent circuit) of the parasitic capacitances, so that, being in general $(C_{p1}+C_{p2})<<C_r$, the actual resonance frequency:

$$f_{rA} = \sqrt{\frac{C_{P1} + C_{P2} + C_r}{L_r \cdot C_r \cdot (C_{P1} + C_{P2})}} \tag{4.4.9}$$

turns out to be typically much higher than the series resonance frequency of the LLC converter.

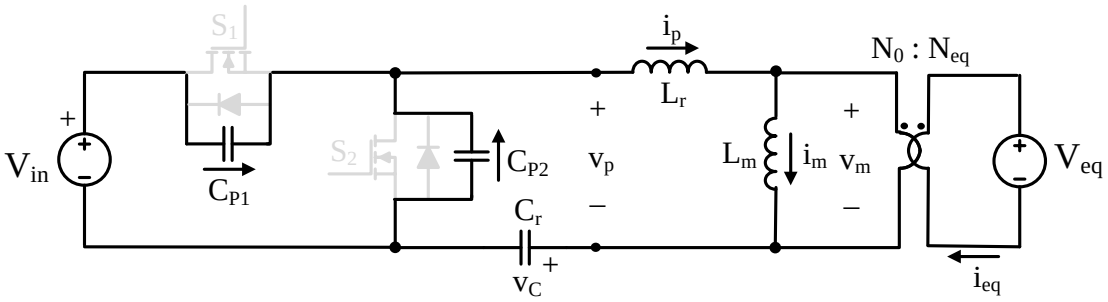


Fig. 4.4.5 - LLC converter: first topological stage characterizing the ground switch soft turn-on transient.

Interval B [t_B, t_C]

The next interval starts when, as shown in Fig. 4.4.9, the resonant current matches the magnetizing current and the output full wave rectifier current zeroes.

In such situation, being the primary voltage still positive the rectifier, diodes will keep the same biasing of the previous interval, so that the secondary side winding current cannot invert its direction and remains null. Consequently, transformer secondary winding will result to be open and the primary resonant current will coincide with the magnetizing current recycling at transformer primary side.

The new resonant network will therefore involve also the magnetizing inductance, whose voltage results to be no more clamped, as shown in Fig. 4.4.6, and start decreasing according to the derivative of the primary resonant current.

Being in general the magnetizing inductance value much greater than that of the leakage inductance ($L_m>>L_r$), the resonance frequency characterizing this phase:

$$f_{rB} = \sqrt{\frac{C_{P1} + C_{P2} + C_r}{(L_r + L_m) \cdot C_r \cdot (C_{P1} + C_{P2})}} \tag{4.4.10}$$

will typically turn out to be much lower than that of the previous interval.

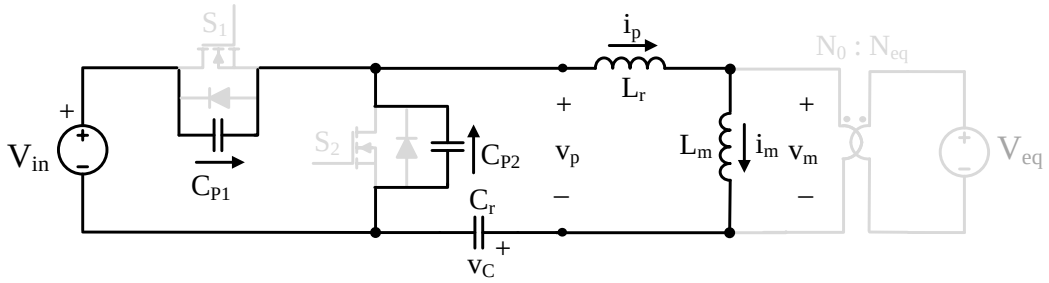


Fig. 4.4.6 - LLC converter: second topological stage characterizing the ground switch soft turn-on transient.

Interval C [t_C, t_D]

When, at the instant t_C, the value of the decreasing voltage across the magnetizing inductance matches the opposite of the output equivalent voltage reflected at transformer primary side:

$$v_m(t_C) = -\frac{N_0}{N_{eq}} V_{eq} = -V_{eq}' \tag{4.4.11}$$

as shown in Fig. 4.4.9 the full wave rectifier restarts conducting and the magnetizing voltage value is clamped again, as shown in Fig. 4.4.7.

The resonant network involved in this stage is the same described in the interval A, so that the expression of the resonance frequency will be equal to that reported in (4.4.9).

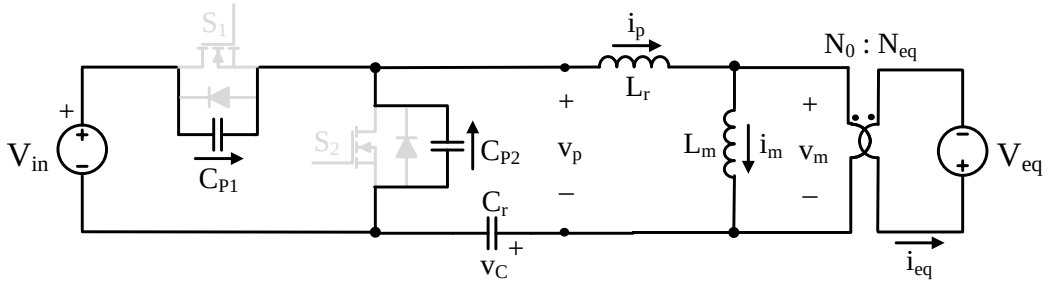


Fig. 4.4.7 - LLC converter: third topological stage characterizing the ground switch soft turn-on transient.

Interval D [t_D, t_E]

When, at the instant t_D, the drain-source voltage of the half bridge ground connected switch reaches zero, the MOSFET body diode is forward biased and starts conducting the primary current, as shown in Fig. 4.4.8.

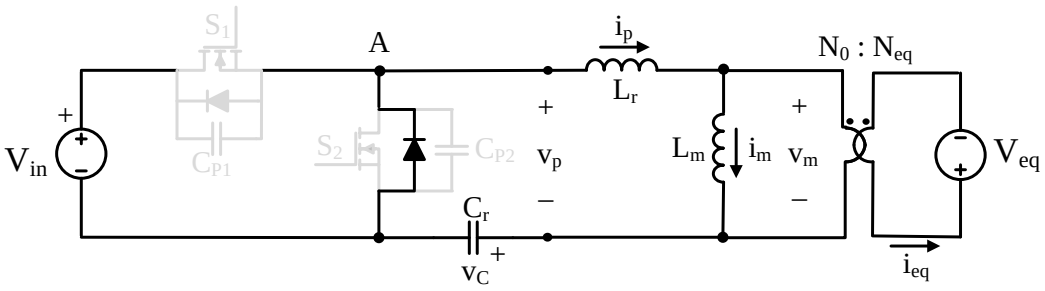


Fig. 4.4.8 - LLC converter: fourth topological stage characterizing the ground switch soft turn-on transient.

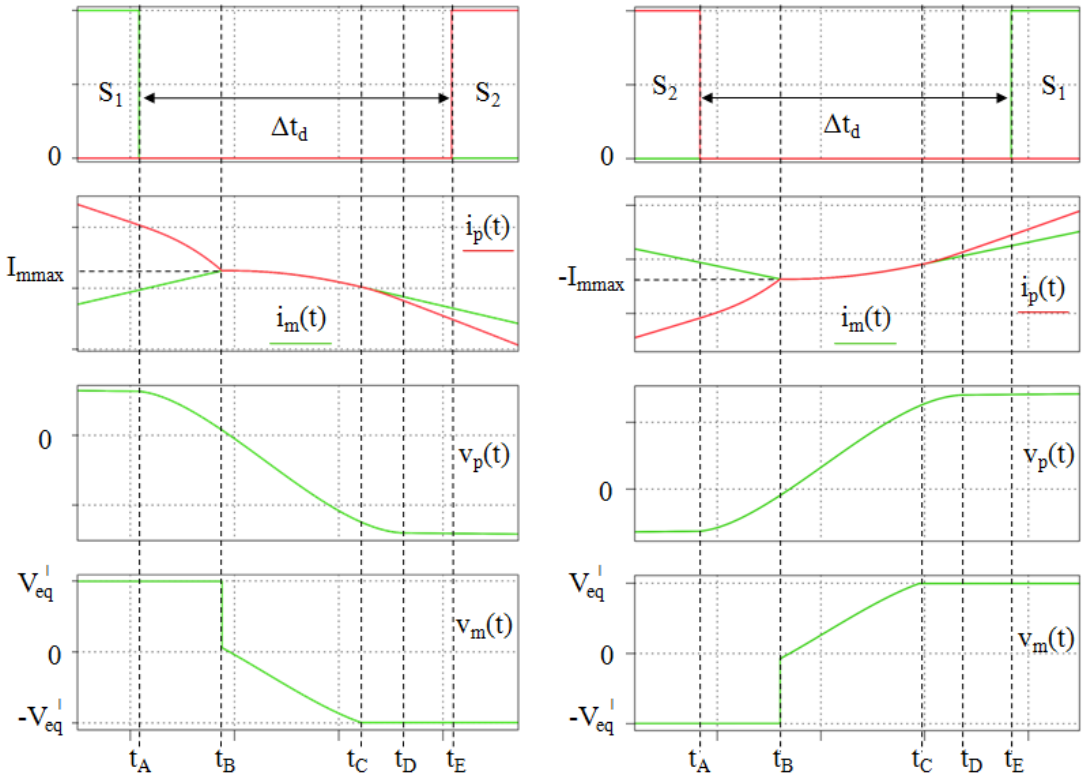
During this phase the drain-source voltage of the ground switch is clamped at zero so that, at the instant t_E, it can be turned-on in a non dissipative way.

As it can be noticed, unlike the previously described case, involving the use of the half bridge converter, the LLC is capable of providing zero voltage switching operation despite the load current level.
According to the analysis performed, indeed, being the parasitic capacitances charge and discharge currents mostly related to the magnetizing current level within the switching transient, the achievement of soft commutation will actually results to be a matter of properly design magnetizing inductance and dead time values, as it will be discussed in the next paragraph 4.5.

It is worth to note that, as already done for the study of the half bridge converter switching transients, also in this case only the soft turn-on commutation of the ground switch has been investigated.

However, as it can be inferred from the resonant converter analysis, the LLC behavior, during the turn-on transient of the DC-link connected switch, will actually result to be exactly symmetrical with respect to the analyzed interval.

As an evidence, can also be considered the waveforms reported in Fig. 4.4.9, derived by simulating, in PLECS® software platform, the LLC converter behavior, assuming the non linear model (4.4.4) for the switches parasitic capacitances.



(a) *(b)*

Fig. 4.4.9 - Waveforms characterizing the soft turn-on of LLC resonant converter's (a) ground connected and (b) DC-link connected switch.

4.5 Multi-Stage Power Supply Design

Once analyzed the converter behavior for both kinds of DC-DC transformer stage implementations and discussed the issues related to the need of guaranteeing zero voltage switching of the isolation stage, it is now possible to focus on converter design. The aim, as usual, is to determine a design procedure so as to actually get a converter compliant to the specifications of the target application, reported in Table 4.1.1.
However, as it can be observed, the input PFC stage design will be utterly conventional. Namely, once the switching frequency is chosen, as usual, the input current ripple specification determines the inductor value, while the output voltage ripple specification imposes the minimum output capacitor value.
Therefore, more interesting and challenging issues, i.e. the main design concerns deriving from the combined use of the DC-DC isolation stage with the output twin BUS buck converter, will be focused and discussed in the following.

Twin BUS Buck Converter

To this end, it is worth to focus at first on converter output stage, considering as a starting point the requirements regarding the minimum and maximum values of the output current dimming interval (I_{LEDmin} and I_{LEDmax}).
From such parameters, knowing the characteristics of the load, namely the threshold voltage and the equivalent resistance of the LED lamp (V_γ, R_γ), the output voltage boundaries to be guaranteed can be derived as:

$$V_{O\min} = V_\gamma + R_\gamma I_{LED\min} \tag{4.5.1}$$

$$V_{O\max} = V_\gamma + R_\gamma I_{LED\max} \tag{4.5.2}$$

Now, as previously explained in paragraph 4.1, the buck converter is supposed to operate in continuous conduction mode (CCM) in order to minimize the conduction losses in the output filter inductor and reduce the switching frequency current ripple through the LEDs.
So, once that a suitable buck converter's duty-cycle (δ) variation range [δ_{min}, δ_{max}] has been fixed, the values of the two buck input voltage levels, actually required to guarantee the desired load current variation can be computed from (4.1.5):

$$V_1 = \frac{V_{O\max}(1-\delta_{\min}) - V_{O\min}(1-\delta_{\max})}{(\delta_{\max} - \delta_{\min})} \tag{4.5.3}$$

$$V_2 = \frac{V_{O\min}\delta_{\max} - V_{O\max}\delta_{\min}}{(\delta_{\max} - \delta_{\min})} \tag{4.5.4}$$

As a result, the expression of the voltage stress on the twin BUS buck converter's controlled switch and freewheeling diode can be therefore expressed, as a function of the output voltage and converter duty-cycle boundary values, as:

$$\Delta V = (V_1 - V_2) = \frac{V_{O\max} - V_{O\min}}{(\delta_{\max} - \delta_{\min})} \tag{4.5.5}$$

Observing (4.5.5), it is worth to note that, given the load range specifications, the maximization of the duty-cycle operating range will turn in minimizing converter devices voltage stress, feature that should be taken into account as a suitable design hint.
In order to guarantee CCM operation, once buck switching frequency (f_{swb}) has been selected on the basis of considerations relating to converter compactness and switching losses, the minimum admissible value for the output filter inductor can be found as:

$$L_O = \frac{(V_1 - V_O)\delta}{2I_{LED}f_{swb}} = \frac{R_\gamma(V_1 - V_2)\delta(1-\delta)}{2f_{swb}\left[V_2 + (V_1 - V_2)\delta - V_\gamma\right]} \tag{4.5.6}$$

where the expressions (4.1.5) and (4.1.6) have been exploited to derive the second equality. Moreover, given the value of the maximum acceptable peak to peak LED current ripple (ΔI_{LEDpp}), also the minimum value required for the output capacitor can be computed:

$$C_O = \frac{(V_1 - V_O)\delta}{8R_\gamma\Delta I_{LEDpp}f_{swb}^2 L_O} = \frac{(V_1 - V_2)\delta(1-\delta)}{8R_\gamma\Delta I_{LEDpp}f_{swb}^2 L_O} \tag{4.5.7}$$

LLC Resonant Converter

As concerns the LLC resonant converter based implementation of the DC-DC transformer stage, on the basis of the analysis performed in paragraph 4.3, keeping in mind the voltage gain expression (4.3.8) and the definitions (4.2.1) and (4.2.2), the transformer's turns ratio values can be computed as:

$$n_{01} = \frac{N_0}{N_1} = \frac{V_{in}}{2V_1}, \qquad n_{02} = \frac{N_0}{N_2} = \frac{V_{in}}{2V_2} \tag{4.5.8}$$

As previously discussed during the analysis of the soft switching issue, as concerns the LLC converter the achievement of zero voltage switching operation is a matter of properly

design the magnetizing current and the dead time elapsing between the half bridge switches conduction intervals.

From a design perspective, in order to simplify the project procedure (keeping in mind the resonant current waveform within the switching transient interval, $i_p(t)$ in Fig. 4.4.9), the simplest way to accomplish this task is to assume transformer primary current to be almost constant within the whole dead time and approximately equal to the magnetizing inductance current peak:

$$\mathrm{I}_{\mathrm{m\,max}} \simeq i_m(\frac{T_{sw}}{2}) \simeq \frac{N_0}{N_{eq}}\frac{V_{eq}}{L_m}(\frac{T_{sw}}{4}) = \frac{V_{in}}{2L_m}(\frac{T_{sw}}{4}) \tag{4.5.9}$$

Now, considering the capacitance non linear model defined in (4.4.4), the total amount of charge to be drained by the primary current, within each switching transient dead time, in order to achieve zero voltage commutations, will be equal to:

$$Q = 2\cdot\int_0^{V_{in}} C_P(v)\;\partial v = 4\cdot C_p(V_{in})\cdot V_{in} \tag{4.5.10}$$

Therefore, under the assumption of constant commutated current, the need for a minimum peak level of the magnetizing current, to guarantee the complete charge and discharge process within the dead time interval Δt_d:

$$\mathrm{I}_{\mathrm{m\,max}} > \frac{Q}{\Delta t_d} = \frac{4\cdot C_p(V_{in})\cdot V_{in}}{\Delta t_d} \tag{4.5.11}$$

will actually turn into a requirement constraining transformer magnetizing inductance.

So, keeping in mind (4.3.10) and (4.3.12), and considering that a suitable dead time should not exceed a few percent of the LLC switching period, that is, for instance:

$$\Delta t_d = \frac{0.04}{f_{sw}} \tag{4.5.12}$$

the maximum value of the magnetizing inductance can be easily computed as:

$$L_{m\mathrm{max}} = \frac{V_{in}}{8 f_{sw} I_{m\mathrm{max}}} = \frac{\Delta t_d}{8 f_{sw} 4\cdot C_p(V_{in})} = \frac{1}{8\cdot 10^2}\cdot\frac{1}{f_{sw}^2\cdot C_p(V_{in})} \tag{4.5.13}$$

Now, with the aim of integrating the resonance inductance (L_r) and the magnetizing inductance (L_m) in the same magnetic component, that is to exploit the leakage inductance of a mutual inductor, a reasonable value of the resonance inductance should be selected to be equal to a few percent of the magnetizing inductance.

In practice, a transformer complying with the design requirements just derived can be implemented and its leakage inductance can be measured and considered as reference in the computation of the resonance capacitor:

$$C_r = \frac{1}{(2\pi f_{sw})^2 L_r} \tag{4.5.14}$$

Once that a suitable commercial capacitor, with capacitance value the closest possible to the outcome of (4.5.14), has been selected, the switching frequency can be finally adjusted so as to guarantee the LLC resonant converter to effectively operate at resonance.

Half Bridge Converter

As stated at the end of paragraph 4.1, the half bridge switches are supposed to operate at fixed switching frequency and constant duty-cycle D=0.5, except for the introduction of a suitable dead time, Δt_d, during switching transients, in order to avoid cross conduction and allow ZVS achievement.

Nevertheless the analysis of converter operation revealed the presence of two idle intervals, within the switching period, whose duration depends on transformer's design as well as on LEDs' average current level.

Indeed, keeping in mind the definitions (4.2.1) and (4.2.4) and being I_1 and I_2 the average values of the current through the buck converter switch and freewheeling diode, respectively equal to:

$$I_1 = I_{LED} \cdot \delta \quad \text{and} \quad I_2 = I_{LED} \cdot (1-\delta) \tag{4.5.15}$$

the average output equivalent current can be written as a function of the LED average current (I_{LED}) and of the buck converter duty-cycle (δ) as:

$$I_{eq} = I_{LED} \cdot \left(\delta + \frac{N_2}{N_1}(1-\delta) \right) \tag{4.5.16}$$

so that the idle time expression (4.2.11) can be finally rewritten as:

$$T_{idle} = \frac{N_{eq}}{N_0} \cdot \frac{4L_{lk} I_{eq}}{V_{in}} = \frac{4L_{lk} I_{LED}}{V_{in}} \left(\frac{N_1}{N_0}\delta + \frac{N_2}{N_0}(1-\delta) \right) \tag{4.5.17}$$

As already observed, the presence of such idle intervals actually affects converter input-output voltage conversion ratio.

From (4.2.23), its output voltage levels can be respectively written as:

$$V_1 = \frac{V_{in}}{2} \cdot \frac{N_1}{N_0} \cdot \left(1 - \frac{N_1}{N_0} \cdot \frac{8 f_{sw} L_{lk}}{V_{in}} \cdot I_{LED} \cdot \left(\delta + \frac{N_2}{N_1} (1 - \delta) \right) \right) \tag{4.5.18}$$

$$V_2 = \frac{V_{in}}{2} \cdot \frac{N_2}{N_0} \cdot \left(1 - \frac{N_1}{N_0} \cdot \frac{8 f_{sw} L_{lk}}{V_{in}} \cdot I_{LED} \cdot \left(\delta + \frac{N_2}{N_1} (1 - \delta) \right) \right) \tag{4.5.19}$$

As it can be noticed, the BUS voltages, provided as inputs to the cascaded twin-BUS buck converter, result to be load dependent, significantly complicating converter's design and forcing the twin BUS buck switch and freewheeling diode towards higher voltage stress levels, as will be better explained in the following paragraph 4.6.

On the basis of these considerations and of the analysis performed in paragraphs 4.2 and 4.4, it is possible now to proceed with converter design. In particular, the value of the leakage inductance can be computed at first, so as to guarantee zero voltage switching operation. According to the analysis performed, to reach this aim the inequality (4.4.8) must be satisfied, from which, knowing the light load level characterizing the target application, the following minimum boundary value of transformer leakage inductance can be derived:

$$L_{lk\min} = \frac{\frac{4}{3} \cdot C_p(V_{in}) \cdot V_{in}^2}{I_{eq}^2 \cdot \left(\frac{N_{eq}}{N_0} \right)^2 \cdot \left[1 + 2 \cdot \frac{N_{eq}}{N_0} \cdot \frac{V_{eq}}{V_{in}} \cdot \frac{L_{lk}}{L_{eq}} \right]^2} \tag{4.5.20}$$

where the equivalent output inductance (L_{eq}) and average current (I_{eq}) can be computed according to (4.2.3) and (4.5.16), respectively.

Now, before moving forward with converter design procedure, it is worth to note that, according to the analysis performed, the selection of transformer leakage inductance calls for a proper trade-off between contrasting requirements.

On one hand, indeed, (2.4.7) clearly shows the need of keeping the leakage inductance parameter value sufficiently high, so as to guarantee the achievement of zero voltage switching operation for the whole load range.

However, on the other hand, observing (4.5.17), (4.5.18) and (4.5.19) it can be inferred that, in order to maximize the input to output energy transfer interval and minimize the sensitivity of converter's voltage gain to the load, the leakage inductance should be minimized.

Which aspect has to be actually prioritized depends on which of such distinct needs represent the major concern according to the constraints imposed by the specification characterizing the target application.

Once the leakage inductance has been chosen, the next design step is the computation of the transformer's turns ratios:

$$n_{01} = \frac{N_0}{N_1} \quad \text{and} \quad n_{02} = \frac{N_0}{N_2} \tag{4.5.21}$$

The matter in this regard is to guarantee the desired load voltage variation range, according to (4.5.1) and (4.5.2), despite the change of the half bridge output voltages (V_1, V_2) with the load.

In order to find the desired parameters that allow to achieve this goal, it is convenient to start defining the variable:

$$x = \left[\frac{\delta}{n_{01}} + \frac{1-\delta}{n_{02}} \right] \tag{4.5.22}$$

Now, once the following base voltage and current have been defined:

$$V_N = \frac{V_{in}}{2} \quad \text{and} \quad I_N = \frac{V_{in}}{8 f_{sw} L_r} = \frac{V_N}{4 f_{sw} L_{lk}} \tag{4.5.23}$$

according to (4.1.5), (4.2.2), (4.2.23) and (4.5.22), the normalized expression of the output voltage can be derived as:

$$\begin{aligned} V_{O\_N} &= \frac{V_O}{V_N} = \frac{1}{V_N} \cdot V_1 \cdot [\delta + (1-\delta) \cdot \frac{N_2}{N_1}] \\ &= \left(1 - 2\frac{T_{idle}}{T_{sw}}\right) x = \left(1 - 2 \cdot \frac{4 L_{lk} f_{sw}}{V_{in}} x\right) x = \left(1 - \frac{I_{LED}}{I_N} x\right) x \end{aligned} \tag{4.5.24}$$

The resulting equation can be therefore uniquely solved in the previously defined variable x, since, given the design constraints, only one of the two possible second order equation's solutions will have physical meaning.

So, imposing (4.5.24) to be satisfied for both light load (V_{Omin}, δ_{min}, I_{LEDmin}) and heavy load (V_{Omax}, δ_{max}, I_{LEDmax}) conditions, the following system is obtained:

$$\begin{cases} V_{O\min} = V_N \cdot \left(1 - \dfrac{I_{LED\min}}{I_N} x_{LL}\right) x_{LL} \\ V_{O\max} = V_N \cdot \left(1 - \dfrac{I_{LED\max}}{I_N} x_{HL}\right) x_{HL} \end{cases} \tag{4.5.25}$$

from which the value of the previously defined variable (x) can be computed, in correspondence of both load boundary conditions (x_{LL} and x_{HL}).

Consequently, rewriting also (4.5.22) in correspondence of such load levels and solving the resulting system in the variables corresponding to the transformer turns ratios (n_{01} and n_{02}), the values of such parameters can be finally found:

$$n_{01} = \left\lfloor \frac{\delta_{\max} - \delta_{\min}}{\delta_{\max} x_{LL} - \delta_{\min} x_{HL}} \right\rfloor \tag{4.5.26}$$

$$n_{02} = \left\lfloor \frac{\delta_{\max} - \delta_{\min}}{\delta_{\max} x_{HL} - \delta_{\min} x_{LL}} \right\rfloor \tag{4.5.27}$$

After that transformer design has been completed, the idle intervals duration can be computed in correspondence of load boundary conditions, so that the values of the isolation stage output voltages can be actually derived according to (4.2.23) and (4.2.2).

As a result, once all the most relevant converter quantities are known, the minimum values of the output filter inductors, required to guarantee CCM operation with the aim of reducing conduction losses, can be finally calculated through the following equations:

$$L_1 = \frac{V_1 T_{idle}}{2 I_1} = \frac{V_1 T_{idle}}{2 I_{LED} \delta} \tag{4.5.28}$$

$$L_2 = \frac{V_2 T_{idle}}{2 I_2} = \frac{V_2 T_{idle}}{2 I_{LED} (1 - \delta)} \tag{4.5.29}$$

Concluding, it is worth to remember that, unlike in the LLC converter case, in the half bridge converter, the capacitor placed in series with the transformer primary winding plays the role of blocking the DC component of the half bridge square voltage only.

As a consequence its value can be simply selected so as to limit the voltage ripple at its terminals to a few percent of the DC voltage level.

The main outcomes of the design procedure presented so far, with reference to both kinds of topology considered for the implementation of the isolation stage, are listed here in the following in Table 4.5.1.

TABLE 4.5.1 - MAIN DESIGN OUTCOMES

MAIN CONVERTER PARAMETERS		
NAME	SYMBOL	VALUE
LLC RESONANT SOFT SWITCHED CONVERTER		
Switching Frequency	f_{sw}	300kHz
Duty cycle	D	0.5
Transformer leakage inductance	L_r	28µH
Transformer magnetizing inductance	L_m	200µH
Transformer primary to first secondary turns ratio	n_{01}	1.35
Transformer primary to second secondary turns ratio	n_{02}	1.63
Resonant Capacitor	C_r	10nF
HALF BRIDGE SOFT SWITCHED CONVERTER		
Switching Frequency	f_{sw}	300kHz
Duty cycle	D	0.5
Transformer leakage inductance	L_r	20µH
Transformer primary to first secondary turns ratio	n_{01}	0.92
Transformer primary to second secondary turns ratio	n_{02}	1.85
DC blocking Capacitor	C_B	470nF
First output filter inductor	L_1	55µH
Second output filter inductor	L_2	35µH
TWIN BUS BUCK CONVERTER		
Switching Frequency	f_{swb}	400kHz
Duty cycle variation range	δ	0.3÷0.7
Output filter inductor (LLC transformer stage implementation)	L_O	18µH
Output filter inductor (HB transformer stage implementation)	L_O	39µH
Output filter capacitor	C_O	1µF

4.6 Main Converter Implementation Issues

On the basis of the analysis performed so far, keeping in mind the design issues highlighted in paragraph 4.5, it is worth making some further considerations concerning the pros and cons of the two different solutions proposed for the implementation of the intermediate conversion stage.
If, indeed, at first glance both converters may seem to have more or less equivalent strengths and weaknesses, some useful hints can be derived from the analysis carried out in the previous paragraphs, so as to determine the most suitable topology relating to the application under study.

In particular, as concerns the LLC resonant converter based solution, one of the most evident advantages is the possibility of guaranteeing soft switching operation, through a proper magnetizing inductance design, independently of the load conditions.
However, this will obviously come at the cost of a non negligible amount of current continuously recycling at transformer primary side and, consequently, of higher conduction losses affecting converter's efficiency.

On the other hand, observing the description of the half bridge converter design procedure, it can be noticed that the need of guaranteeing zero voltage switching operation, even at light load, forces to keep transformer leakage inductance (L_{lk}) an primary current peak (I_{pmax}) conveniently high.
This distinctive feature, characterizing the solution involving the use of the half bridge converter, will actually result in longer idle intervals, according to (4.5.17), and, consequently, in larger output filter inductances, as shown in (4.5.28) and (4.5.29).
Moreover, as previously explained, a further negative consequence, due to the presence of load dependent idle times within the switching period, is the sensitivity of the twin-bus buck input voltages to the LED load current level.
As concerns the application under study, indeed, this effect produces a variability of converter operation conditions that significantly complicates the design procedure, compared to the case of the LLC resonant converter.
Furthermore, it is worth to note that such variation of the input voltages not only affects converter design procedure, but also forces the output stage switch and freewheeling diode towards higher voltage stress levels.

In order to understand this latter concern, first of all, the expressions (4.2.2) and (4.2.23) should be considered, according to which the half bridge output voltages in light and heavy load conditions can be respectively expressed as:

$$\begin{cases} V_{1LL} = \frac{1}{2} V_{in} n_{10} \left(1 - \frac{2T_{idleLL}}{T_{sw}} \right) \\ V_{2LL} = \frac{1}{2} V_{in} n_{20} \left(1 - \frac{2T_{idleLL}}{T_{sw}} \right) \end{cases} \quad \text{in light load condition} \tag{4.6.1}$$

$$\begin{cases} V_{1HL} = \frac{1}{2} V_{in} n_{10} \left(1 - \frac{2T_{idleHL}}{T_{sw}} \right) \\ V_{2HL} = \frac{1}{2} V_{in} n_{20} \left(1 - \frac{2T_{idleHL}}{T_{sw}} \right) \end{cases} \quad \text{in heavy load condition} \tag{4.6.2}$$

As it can be observed, with the varying load, both the input voltages will be shifted so that their ratio turns out to be constantly equal to the fraction of the corresponding transformer windings' turns:

$$\frac{V_{1HL}}{V_{2HL}} = \frac{V_{1LL}}{V_{2LL}} = \frac{n_{02}}{n_{01}} = \frac{N_1}{N_2} \tag{4.6.3}$$

However, being the voltage stress of the buck converter controlled switch and freewheeling diode (4.5.5) dependent on the difference between the two BUS voltage levels and not on their proportion, such quantity will actually result to be sensitive to the load level:

$$\Delta V_{LL} = V_{1LL} - V_{2LL} = \frac{1}{2} V_{in} \left(1 - \frac{2T_{idleLL}}{T_{sw}} \right) \left(n_{10} - n_{20} \right) \tag{4.6.4}$$

$$\Delta V_{HL} = V_{1HL} - V_{2HL} = \frac{1}{2} V_{in} \left(1 - \frac{2T_{idleHL}}{T_{sw}} \right) \left(n_{10} - n_{20} \right) \tag{4.6.5}$$

From (4.6.4) and (4.6.5), the relation between the voltage stress levels in light and heavy load conditions can be therefore written as:

$$\Delta V_{LL} = \frac{T_{sw} - 2T_{idle\,LL}}{T_{sw} - 2T_{idle\,HL}} \Delta V_{HL} = \Gamma \Delta V_{HL} \tag{4.6.6}$$

where, being the idle time at the minimum load lower than that corresponding to full load conditions $\left(T_{idleLL} < T_{idleHL} \right)$, the adimensional parameter:

$$\Gamma = \frac{T_{sw} - 2T_{idleLL}}{T_{sw} - 2T_{idleHL}} \tag{4.6.7}$$

turns out to be greater than unity, indicating a stronger voltage stress at light load with respect to nominal load conditions.

Moreover, imposing the desired whole load voltage range to be effectively guaranteed, despite twin BUS buck converter input voltages variation, it can be written:

$$\begin{cases} V_{O\min} = V_{1LL}\delta_{\min} + V_{2LL}\left(1-\delta_{\min}\right) \\ V_{O\max} = V_{1HL}\delta_{\max} + V_{2HL}\left(1-\delta_{\max}\right) \end{cases} \tag{4.6.8}$$

so that the BUS voltage levels in nominal load conditions can be derived, as a function of the parameter defined in (4.6.7) and of the load voltage and duty-cycle boundary values, as follows:

$$V_{1HL} = \frac{V_{O\max}\Gamma(1-\delta_{\min}) - V_{O\min}(1-\delta_{\max})}{\Gamma(\delta_{\max} - \delta_{\min})} \tag{4.6.9}$$

$$V_{2HL} = \frac{V_{O\min}\delta_{\max} - \Gamma V_{O\max}\delta_{\min}}{\Gamma(\delta_{\max} - \delta_{\min})} \tag{4.6.10}$$

The corresponding expression of the voltage stress on the output buck stage devices can be therefore written, with reference to that applying to the case of the LLC resonant converter (ΔV defined in (4.5.5)), as:

$$\Delta V_{HL} = (V_{1HL} - V_{2HL}) = \Delta V + \left(\frac{\Gamma - 1}{\Gamma}\right)\left(\frac{V_{O\min}}{\delta_{\max} - \delta_{\min}}\right) \tag{4.6.11}$$

As it can be observed, being the parameter Γ greater than unity, the voltage stress level actually results to be lower if an LLC converter, instead of an half bridge converter, is used to implement the intermediate DC-DC transformer stage.

In particular, keeping in mind also (4.6.6) the actual relationship between the voltage stress in correspondence of the use of an LLC converter (despite of the load level) and of an half bridge converter (in heavy and light load conditions, respectively) can be written as:

$$\Delta V \;<\; \Delta V_{HL} = \Delta V + \left(\frac{\Gamma - 1}{\Gamma}\right)\cdot\left(\frac{V_{O\min}}{\delta_{\max} - \delta_{\min}}\right) \;<\; \Delta V_{LL} = \Gamma \cdot \Delta V_{HL} \tag{4.6.12}$$

For sake of completeness, it is worth to mention that the variability of the two BUS voltage levels that characterizes the solution involving the use the half bridge converter, will

actually influence also the duty cycle to load current transfer function of the twin BUS buck output stage, that is used to design output current feedback control.
Under the assumption of almost DC input and output voltages, writing the equation of the average input current and of the average voltage across the output filter inductor:

$$\begin{cases} i_1 = i_O \delta \\ v_L = (v_1 - v_O)\delta + (v_2 - v_O)(1-\delta) \end{cases} \tag{4.6.13}$$

the equivalent circuit of Fig. 4.6.1, representing the converter averaged model in continuous conduction mode, can be easily derived.

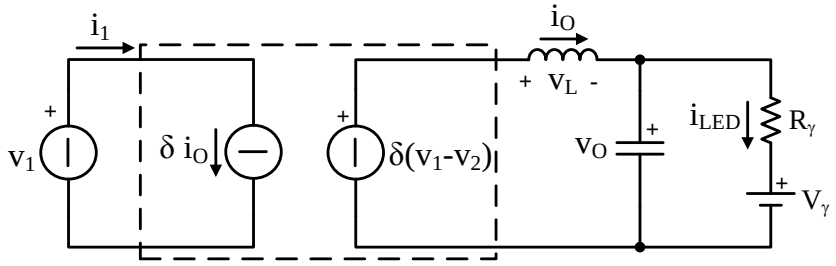


Fig. 4.6.1 - Model of the twin BUS buck in CCM, relative to the quantities averaged over converter switching period.

Now, distinguishing for each variable a constant term and a perturbation term as follows:

$$\begin{cases} I_1 + \hat{i}_1 = \left(I_O + \hat{i}_O\right)\left(D + \hat{\delta}\right) \\ V_L + \hat{v}_L = \left(V_1 + \hat{v}_1 - V_2 - \hat{v}_2\right)\left(D + \hat{\delta}\right) + \left(V_2 + \hat{v}_2 - V_O - \hat{v}_O\right) \end{cases} \tag{4.6.14}$$

the small signal model, relative to perturbation quantities, can be finally found, neglecting the product of both constant terms (that are related to steady state conditions) and of perturbations (according to the small signal assumption), as shown in Fig. 4.6.2.

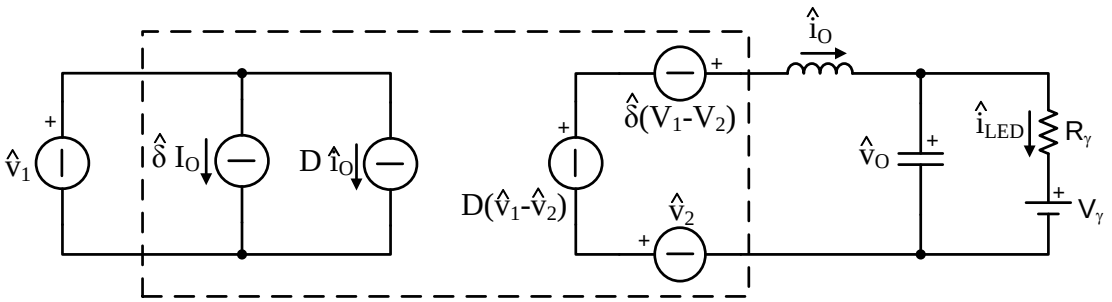


Fig. 4.6.2 - Average model of the twin BUS buck in CCM, relative to the perturbation quantities.

By taking the Laplace transform of the corresponding small signal equations, relative to the voltage across the output filter inductor and the current through the output capacitor, it can be written:

$$\begin{cases} \mathrm{sL}_O \hat{\mathrm{i}}_O(s) = [V_1 - V_2]\hat{\delta}(s) + D[\hat{v}_1(s) - \hat{v}_2(s)] - \hat{v}_O(s) \\ \mathrm{sC}_O \hat{v}_O(s) = \hat{i}_O(s) - \dfrac{1}{R_\gamma}\hat{v}_O(s) \end{cases} \tag{4.6.15}$$

From (4.6.15), solving the first equation for $\hat{\mathrm{i}}_O(s)$ and substituting in the second equation, the output voltage can be actually expressed as a function of the input voltage levels and of the control variable as follows:

$$\hat{v}_O(s) = \frac{V_1 - V_2}{\left(\mathrm{s}^2 \mathrm{L}_O \mathrm{C}_O + \mathrm{s}\dfrac{\mathrm{L}_O}{R_\gamma} + 1\right)} \cdot \hat{\delta}(s) + \frac{D}{\left(\mathrm{s}^2 \mathrm{L}_O \mathrm{C}_O + \mathrm{s}\dfrac{\mathrm{L}_O}{R_\gamma} + 1\right)} \cdot \hat{v}_1(s) + \frac{1-D}{\left(\mathrm{s}^2 \mathrm{L}_O \mathrm{C}_O + \mathrm{s}\dfrac{\mathrm{L}_O}{R_\gamma} + 1\right)} \cdot \hat{v}_2(s) \tag{4.6.16}$$

As a result, the transfer function of interest finally turns out to be:

$$G_{i\delta}(s) = \left.\frac{\hat{i}_{LED}(s)}{\hat{\delta}(s)}\right|_{\substack{\hat{v}_1(s)=0 \\ \hat{v}_2(s)=0}} = \frac{V_1 - V_2}{R_\gamma} \cdot \frac{1}{\left(\mathrm{s}^2 \mathrm{L}_O \mathrm{C}_O + \mathrm{s}\dfrac{\mathrm{L}_O}{R_\gamma} + 1\right)} \tag{4.6.17}$$

that is similar to the conventional second order function characterizing the standard buck converter in CCM, except for the value of the DC gain, that in this case clearly depends on the difference between the two input BUS voltage levels.

On the basis of such information, for the application under study, converter control can be simply implemented in order to regulate to zero the error between the sensed LED current and a proper reference signal.

To this end a PI or PID controller can be used so as to adjust converter duty-cycle to compensate for the load changes (e.g. due to LED thermal drift), or the reference signal variation, aimed at performing lamp light dimming.

The target application does not actually requires any particular performance in this regards, so that control design results to be quite straightforward, however there is an implementation issue that may be worth to briefly report.

In order to simplify buck converter controlled switch driving, indeed, the standard buck configuration is usually inverted so as to connect MOSFET source to the ground reference

voltage. Nevertheless this will consequently complicate the LED current sensing, being the load voltage floating with respect to the ground reference potential.
A simple way to address such issue can be the implementation of a PNP transistor current mirror, as shown in Fig. 4.6.3, so as to reflect the load current and provide a sensing signal proportional to load current and referred to ground potential.

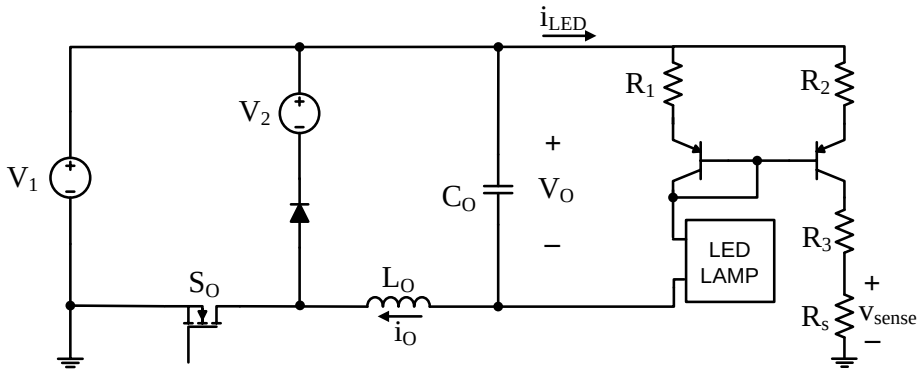


Fig. 4.6.3 - Twin BUS buck converter inverted configuration with load current sensing network.

Concluding, on the basis of the analysis performed so far, it is possible to say that, for the application under study, the LLC resonant converter actually seems to be the most suitable solution for the implementation of the DC transformer isolation stage.
The load independence of the input to output voltage transfer function, characterizing such converter, when operated at the resonance frequency, indeed, allows to get stable BUS voltage input levels for the cascaded twin BUS buck output stage. This consequently facilitates converter design and control and reduces the voltage stress level on the output stage devices.
Moreover, the absence of the two output filter inductors, which are instead necessary in the solution involving the use of the soft switched half bridge converter, actually simplify the topology, reduces costs and improves the overall efficiency.
Finally, the capability of the LLC resonant converter to guarantee zero voltage switching operation, despite the load current level, definitely makes the LLC converter based solution the best option, as concerns the considered application.

4.7 Simulation Outcomes and Experimental Results

The effectiveness of the analysis performed so far and of the design procedure presented in paragraph 4.5 has been finally tested.

To this end, a first verification has been performed at software level, using the PLECS® platform in order to simulate the behavior of the converter, realized according to the design outcomes listed in Table 4.5.1, for both the proposed kinds of DC-DC transformer stage implementation.

In this way it has been possible to verify the main aspects revealing the effective compliance of converter operation with the design specifications.

In particular, as concerns the half bridge converter and twin BUS buck converter output filter inductances, the achievement of continuous conduction mode operation in the whole load range has been checked.

Moreover, the voltage stress levels on buck devices, with the varying load current, has been monitored, as also the achievement of zero voltage switching operation of both the LLC and the Half bridge converters.

It is worth to remember that, with respect to the twin BUS buck converter voltage stress, the analysis of paragraph 4.6 has revealed the beneficial effects of the LLC based isolation stage implementation, compared to the solution involving the use of the half bridge converter.

As it can be observed, the simulated waveforms of Fig. 4.7.1 and Fig. 4.7.2, showing the buck stage input voltage levels in correspondence of three different load current levels (namely 50%, 75% and 100% of nominal load current) actually confirm the analytical inferences.

Indeed, as can be noticed the LLC isolation stage, as expected, not only provides stable input BUS voltages to the cascaded stage, but also guarantees lower voltage stresses on buck devices, so that the relation reported in(4.6.12) actually results to be confirmed.

As concerns the soft switching issue, from the analysis of switching transients performed in paragraph 4.4, it resulted that, for the LLC converter, given the dead time length, the achievement of zero voltage switching operation is only a matter of properly designing transformer magnetizing inductance.

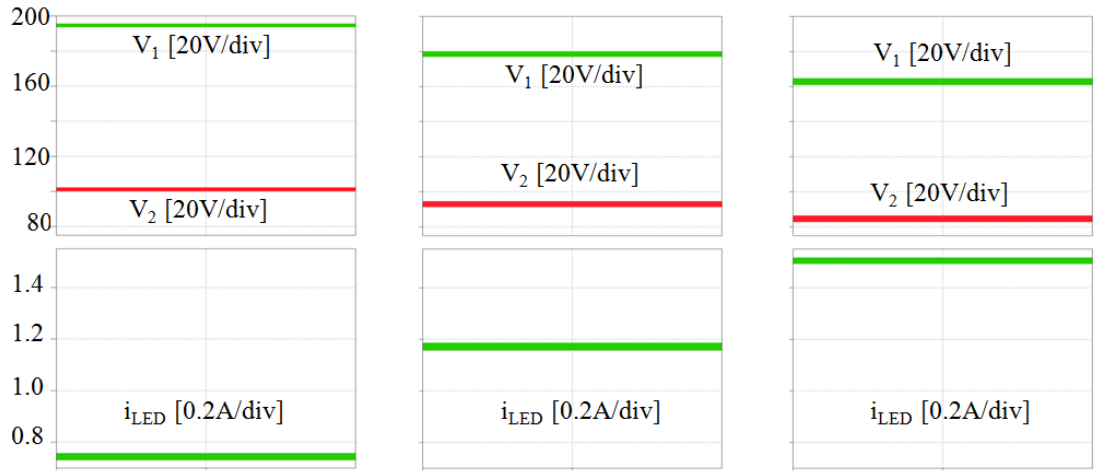


Fig. 4.7.1 - Simulated twin BUS buck input voltage levels and load current, in correspondence of an HB converter based implementation of the DC-DC transformer isolation stage. (a) Light load, (b) intermediate load and (c) full load conditions.

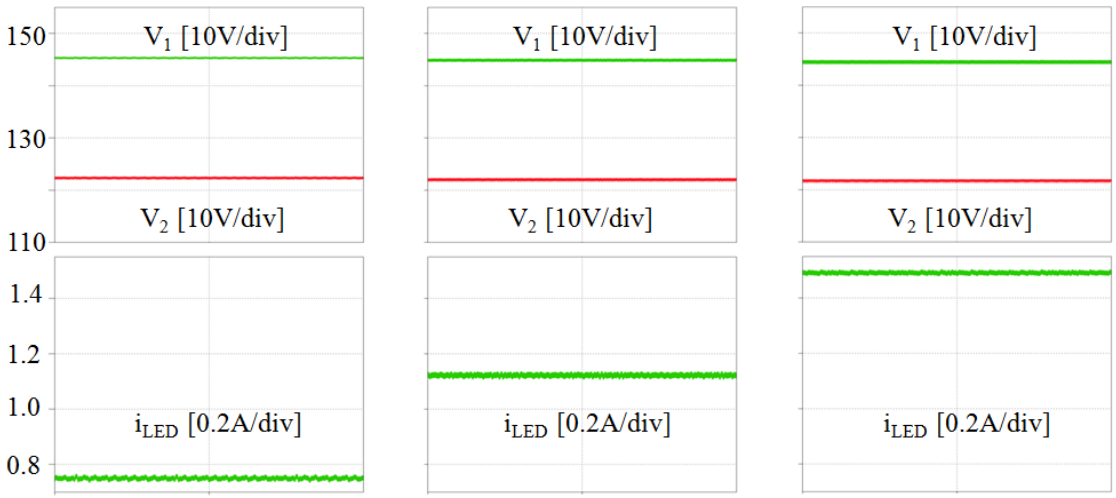


Fig. 4.7.2 - Simulated twin BUS buck input voltage levels and load current, in correspondence of an LLC resonant converter based implementation of the DC-DC transformer isolation stage. (a) Light load, (b) intermediate load and (c) full load conditions.

On the other hand, in the half bridge converter the MOSFETs' parasitic capacitances charge and discharge process results to be completed by the charge contained in the transformer leakage inductance. So, being the latter a parameter of difficult manipulation, zero voltage switching can be effectively accomplished only above a given minimum load level.

Looking at Fig. 4.7.3, showing the primary side current and half bridge voltage simulated waveforms in light load condition, it can be noticed that the designed converter is effectively capable to achieve soft switching operation, even at the minimum load.

As it can be observed, indeed, the half bridge voltage gradually varies between ground and DC-link voltage, within the transient dead time, since it is not abruptly forced from one voltage level to the other by the turn-on of either one or the other half bridge switch.

Finally, from the half bridge voltage and primary current simulated waveforms, shown in Fig. 4.7.4 and Fig. 4.7.5 (a), related to the half bridge and the LLC resonant converter respectively, it can be noticed that in both cases converter behavior, exactly corresponds to that described by the analysis of paragraphs 4.2 and 4.3, respectively.

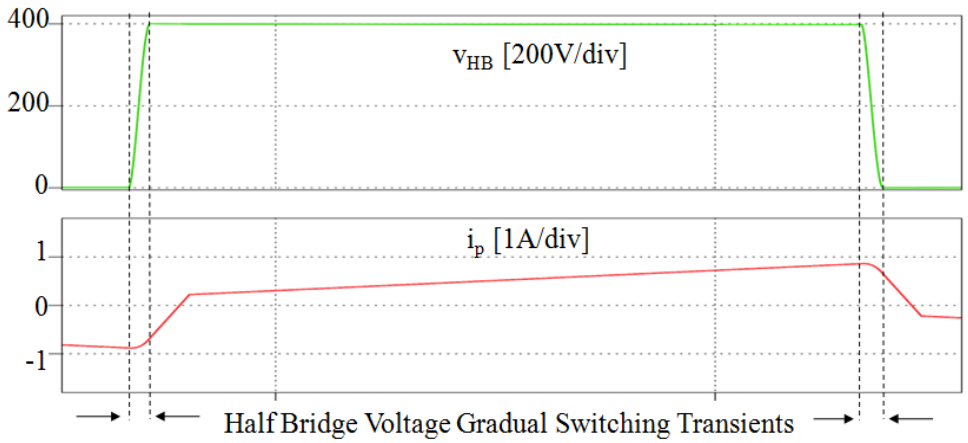
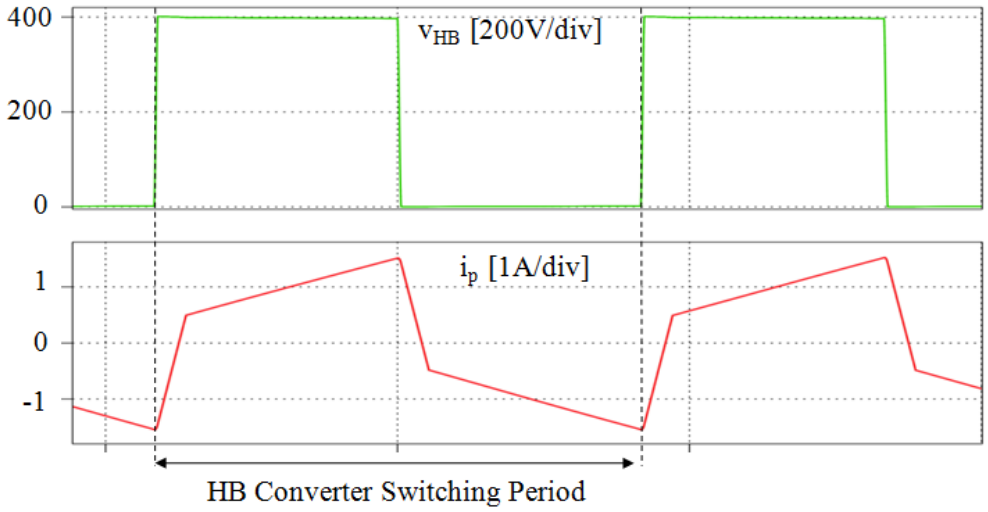


Fig. 4.7.3 - Simulated waveforms of the half bridge converter: primary side current and half bridge voltage, in light load condition.



ig. 4.7.4 - Simulated waveforms of the half bridge converter: primary side current and half bridge voltage, in correspondence of the load variation range midpoint.

In particular, as concerns the LLC converter, from the sinusoidal waveform of the primary resonant current, the suitability of the selected resonance capacitor and inductance values is actually confirmed.

Moreover, from the zoom focusing on the half bridge voltage edges, shown in Fig. 4.7.5 (b), it can be observed the effectiveness of the designed magnetizing inductance value in guaranteeing zero voltage switching operation.

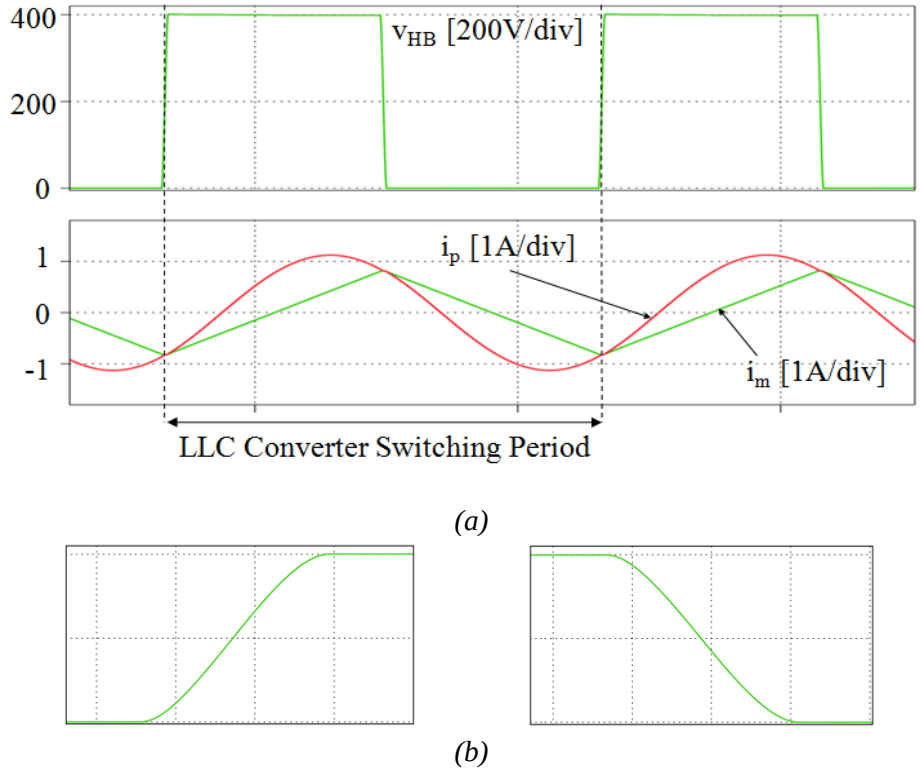


Fig. 4.7.5 - (a) Simulated waveforms of the LLC converter: half bridge voltage, primary side resonant current and magnetizing current, in correspondence of the load variation range midpoint; (b) zoom of the positive and negative edges of the half bridge voltage.

Since the simulation outcomes turned out to be effectively consistent with the given converter specifications, the next step has been the verification of converter performance at experimental level.

To this end an AC/DC converter prototype has been built, according to the design outcomes reported in Table 4.5.1, for both kinds of DC transformer stage implementation.

As concerns the input power factor correction stage, the boost converter is operated in CCM at constant frequency equal to 65kHz. The average current control is performed by the Texas Instruments UCC28019 controller. The input current and line voltage waveforms, in the line half period, are shown in Fig. 4.7.6, in correspondence of the load range midpoint. The resulting power factor is almost unity.

As regards the half bridge based implementation of the isolation stage, the gradual variation of the half bridge voltage edges, shown in Fig. 4.7.7, confirms the effective achievement of zero voltage switching operation, even at the minimum load as already verified also at simulation level (Fig. 4.7.3).

Moreover, by observing the current and voltage experimental waveforms, shown in Fig. 4.7.8 in correspondence of the load variation range midpoint, the good agreement with the analytically derived waveforms of Fig. 4.2.3 and the simulated ones, reported in Fig. 4.7.5,can be appreciated.

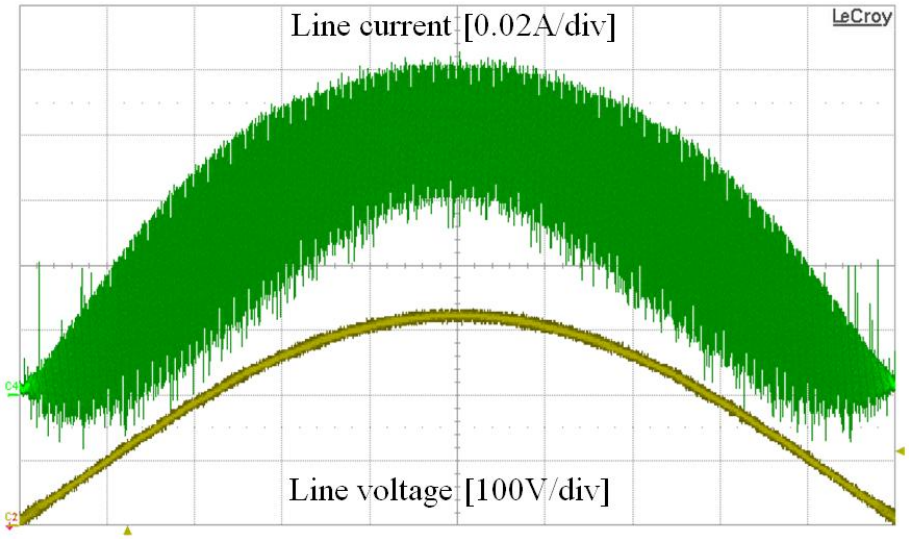


Fig. 4.7.6 - AC/DC converter input current and line voltage waveforms in the line half period.

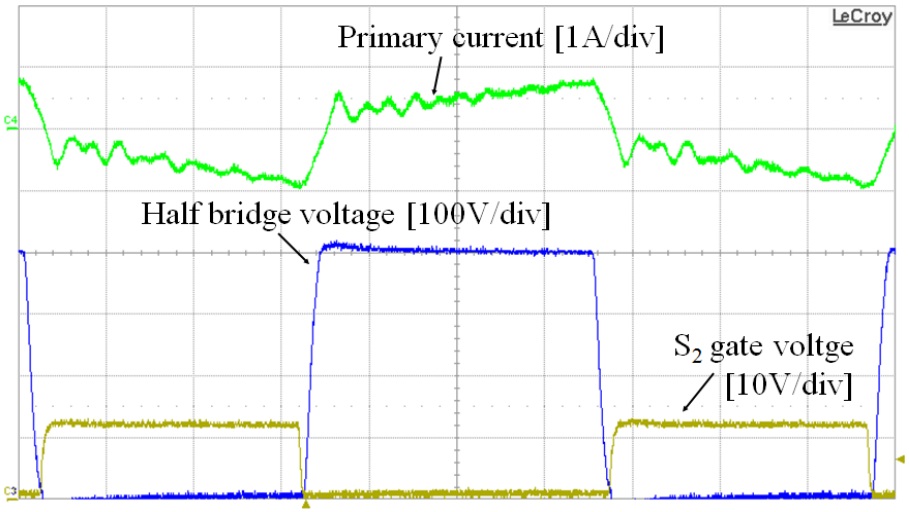


Fig. 4.7.7 - Half bridge converter. Primary side current, half bridge voltage and ground switch gate-source voltage experimental waveforms at light load.

As regards the LLC resonant converter based implementation of the isolation stage, from the experimental waveforms reported in Fig. 4.7.9 it can be noticed that the resonant current is almost purely sinusoidal, proving that the converter is effectively working at resonance. Furthermore, focusing on the half bridge voltage waveform, the absence of any abrupt change in the voltage level, on both positive and negative edges, actually provides a valuable evidence of the achievement of zero voltage switching operation.

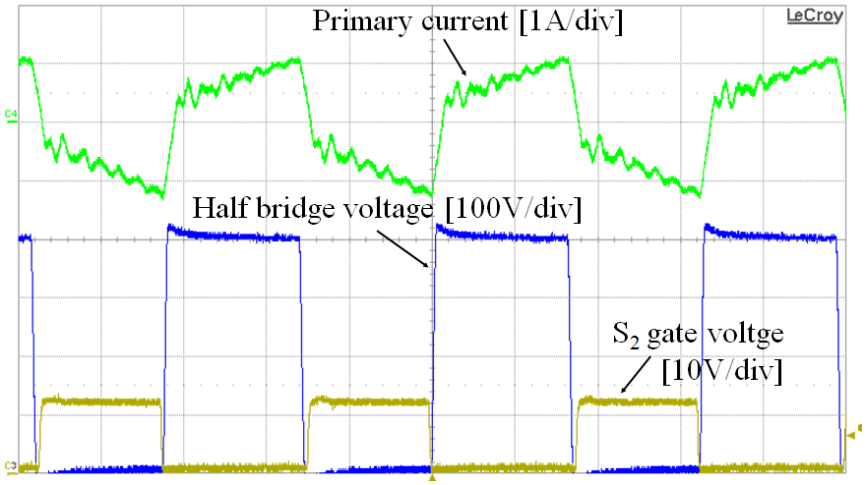


Fig. 4.7.8 - Half bridge converter. Primary side current, half bridge voltage and ground switch gate-source voltage experimental waveforms in correspondence of the load range midpoint.

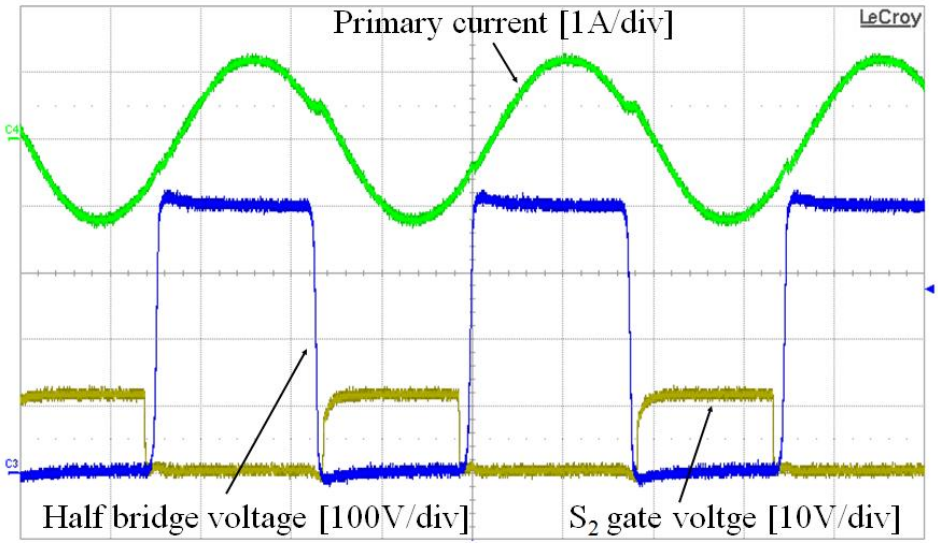


Fig. 4.7.9 - LLC resonant converter. Primary side current, half bridge voltage and ground switch gate-source voltage experimental waveforms in correspondence of the load range midpoint.

As concerns the output twin BUS buck stage implementation, 60V rated components have been chosen for the solution involving the use of an LLC resonant converter based intermediate stage, while 150V rated components have to be used in the alternative investigated case, due to the higher voltage stress level.

The overall ballast's measured efficiency in nominal load conditions is equal to the 92%, if the LLC resonant converter is used as DC isolation stage, and to the 91%, if the Half Bridge based implementation is preferred.

Conclusions

Thanks to recent remarkable advances, solid state lighting provides nowadays a viable way towards a significant reduction of the electrical energy consumptions. The widespread use of this technology would, indeed, substantially improve the efficiency of the lighting sector, giving a concrete chance to get considerable beneficial effects from both an environmental and an economic standpoint.

As observed, however, the high initial price still hinders the increase of solid state lighting market share, actually calling for further efforts aimed at reducing the cost per lumen characterizing this technology, so as to shorten its payback time.

In this perspective, if, on one hand, an improvement of LED devices manufacturing is desirable, on the other, a relevant role is played by the optimization of the LED driving and control stage. As discussed, the latter concern actually forces to tackle some major issues such as the compliance with harmonic injection and energy saving standards, the minimization of component count, the maximization of ballast reliability and efficiency, LED current regulation, emitted light dimming capability, etc...

Different approaches can be considered for the offline driving of solid state light sources, depending on the specific features and on the power rating of the target lighting application. Inter alia, three different general kinds of solution have been pointed out and discussed in this thesis, which are based on the use of a single stage, a double integrated stage and a multiple stage configuration, respectively. A novel offline LED power supply has been proposed for each approach.

In particular, as concerns the first mentioned driving configuration, the AHB-flyback converter has been investigated.

Thanks to its low component count, this single stage topology results to be a very suitable solution for cost effective applications in which compactness is a major concern, as for example in the case of bulb replacements. The strong variability of converter operating conditions, actually forces, however, to a converter suboptimal design, consequently

calling for the implementation of optimization techniques, so as to improve converter efficiency, as carefully discussed. In this regard, a further development of the research activity performed, could be aimed at comparing the net converter efficiency improvements deriving from the use of each of these proposed technique. Moreover, the incorporation of the whole optimization networks and converter output regulation circuitry in a single integrated circuit is desirable, so as preserve ballast compactness.

As concerns the integrated configuration approach, the double integrated buck topology has been investigated. This compact and reliable solution turns out to be particularly suitable in medium power solid state lighting applications, such as downlighting, in which, besides cost and volume minimization also good line side performance are required. The features of the double buck integrated topology have been carefully analyzed, discussed and tested at simulation level, actually confirming the analytical results. Future developments of this study include the verification of converter performance also at experimental level, by performing laboratory tests on a converter prototype complying with the outcomes of the presented design procedure. It will thus possible, indeed, to check the actual conversion efficiency and output regulation capability of the proposed topology as well as the effective compliance with the EN 61000-3-2 and the Energy Star standard requirements.

Finally, as concerns high power applications, such as street lighting, two different solutions has been proposed, both based on the use of the multiple stage approach. The investigated offline ballasts actually relies on a triple stage configuration made of an input PFC stage, an intermediate DC/DC transformer stage and an output LED current regulation stage. The difference between the two options essentially lies in the kind of topology selected for the implementation of the intermediate isolation stage, namely a LLC resonant converter and a soft switched half bridge converter. A comparative analysis of such solutions has been performed, which revealed that the former topology is actually the most suitable solution for the target application. High efficiency, power factor correction and output regulation performance have been achieved through the use of highly optimized power conversion stages. Further development of this work could be aimed at investigating the net benefits of the proposed highly optimized configuration with respect to the solution that dispenses the output DC/DC conversion stage, directly using the LLC converter to regulate the LED currents. Another interesting aspect that could be finally worth examining is the effect, on the LLC resonant converter behavior, of the transformer leakage inductance split between primary and secondary side.

When using integrated magnetic, indeed, that is when transformer windings are arranged so as to achieve the leakage inductance value required to implement converter resonant inductance, two leakage inductances are actually created, one associated to each winding. So the typical transformer model, that considers its magnetizing inductance together with a lumped leakage inductance located at the primary side, will no longer be suitable to carry out converter analysis. An accurate investigation of the effects of the split resonant inductance on the overall voltage conversion ratio and on converter small-signal behavior should be therefore performed.

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