Università degli Studi di Padova

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Analysis and Design of High Performance Building Blocks for Phased Array System in BiCMOS Technology

Tesi di: FABIO PADOVAN

Scuola di dottorato in Ingegneria dell'Informazione
Indirizzo in Scienza e Tecnologia dell'Informazione
Ciclo XXVIII

Supervisore:
Prof. Andrea Bevilacqua

Direttore della Scuola:
Prof. Matteo Bertocco
Coordinatore di indirizzo:
Prof. Carlo Ferrari

I would like to dedicate this thesis to my family ...

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Abstract

Phased array systems are spreading a lot in these years due to their higher performances respect to a single antenna. These systems have been progressively more and more employed in many fields such as satellite communications, high data rate links (emerging 5G technology), military and automotive radars. Initially they where only used for military applications due to their higher costs and complexity. Thanks to the technology development and the researchers efforts, these days it is possible to integrate on the same chip an entire phased array system, leading to a drastic cost reduction. The explosive growth of the applications that use the phased array approach is the motivation behind this thesis, which deals with the analysis and design of high performance building blocks for phased array systems.
The first part of this work gives a brief introduction on the phased array systems illustrating the working principle, the main tasks and issues of the design related to the need for high resolution and directivity of the antennas array.
The second part of the thesis is dedicated to the analysis and design of building blocks for phased array systems. More in detail, the design of VGA (variable gain amplifier) and VCO (voltage controlled oscillator) will be described. VGAs are very important in the whole system because they are responsible for the array directivity and precision in the beam forming. The impact of the VGA performance impact on the phased array functionality is hence treated and analyzed. The phase behavior when the gain setting is changed is analyzed and discussed in depth. The aim of the design is to keep the phase of the signal constant for all the gain range variation in the frequency band of the amplifier. Several phase error compensation techniques have been studied and implemented. Some X-Band SiGe VGA have been realized and measured. The performance in terms of phase error as the gain is varied out-performs the state-of-the-art. In addition to X-Band applications, some work on the upcoming 5G Communication Network has been done. A Wide Band ($15-40\,\text{GHz}$) Variable Gain Amplifier has been prototyped in SiGe BiCMOS technology and a $28\,\text{GHz}$ VGA has been implemented in a $40\,\text{nm}$ CMOS Technology.

The VCO is the other fundamental building block that we take into consideration in this thesis. In this case, we focus our attention on the phase noise, a crucial parameter that is directly related to the performance of the phased array system. An in-depth analysis on the minimization of the phase noise has been done and some K-band (i.e. 18-27 GHz) VCOs have been realized in a SiGe bipolar technology. The VCOs feature a phase noise as low as -137 dBc/Hz at 10 MHz offset from the carrier. This result out-performs the state of the art if compared to other Silicon K-band Silicon-based VCOs. Only VCOs implemented using compound semiconductor technologies show better performance in terms of phase noise. However the technology cost is in this case, dramatically higher.
The work shows the feasibility of realizing high performance building blocks for phase array systems in Silicon technology. The possibility to integrate an entire phased array system on the same chip leads to a drastic cost reduction, overcoming the barrier that has stopped the development of this approach for several applications for many years. This a is crucial point for the development of next generation high data rate communication links and high precision automotive and military radars

Sommario

I sistemi Phased Array si stanno diffondendo molto in questi anni grazie alle loro elevate prestazioni rispetto alla singola antenna. Questi sistemi sono stati usati sempre più in molti campi, per esempio nelle comunicazioni satellitari, nei link ad alta velocità di trasmissione (emergente tecnologia 5G), nei radar militari e automotive. Inizialmente erano usati solo nelle applicazioni militari a causa dell'elevato costo e complessità del sistema. Grazie allo sviluppo di nuove tecnologie e allo sforzo dei ricercatori, al giorno d'oggi è possibile integrare nello stesso chip un intero sistema Phased Array, portando quindi ad una drastica riduzione dei costi. La motivazione di questa tesi è appunto la crescita esplosiva delle applicazioni che adottano l'approccio dei Phased Array, in particolare la tesi si occupa dell'analisi e progettazione di blocchi circuitali ad alte prestazioni per i sistemi Phased Array.
La prima parte del lavoro consiste in una breve introduzione dei sistemi con array di antenne illustrando il principio di funzionamento gli oobiettivi e le problematiche della progettazione relazionate al bisogno di avere alta risoluzione e direttività dell'array di antenne.
La seconda parte della tesi è dedicata all'analisi e progettazione di blocchi circuitali per i sistemi Phased Array. Più in dettaglio, verrà descritta la progettazione di VGA (amplificatori a guadagno variabile) e VCO (Oscillatori controllati in tensione). I VGA sono molto importanti nel sistema perche sono responsabili della direttività dell'array e nella precisione nella formazione del fascio. Nella tesi viene analizzato l'impatto delle prestazioni del VGA rispetto alla funzionalità del sistema. Viene analizzato più in particolare il comportamente della phase del segnale rispetto alla variazione del guadagno. L'obiettivo del progetto è quello di avere la fase del segnale costante per tutto il range di variazione di guadagno nella banda di frequenze dove opera l'amplificatore. Sono state studiate e implementate diverse tecniche di compensazione dell'errore di fase. Sono stati realizzati e misurati diversi VGA in banda *X* in Silicio Germanio. Le prestazioni in termini di errore di fase superno lo stato dell'arte. Oltre alle applicazioni in banda *X* è stato fatto del lavoro per l'imminente tecnologia di comunicazione 5G. E' stato prototipato un amplificatore a guadagno variabile a

larga banda ($15-40$ GHz) in tecnologia SiGe BiCMOS ed un VGA a 28 GHz in tecnologia CMOS 40 nm.
Il VCO è un altro fondamentale blocco circuitale che abbiamo preso in considerazione in questa tesi. In questo caso ci siamo focalizzati sul rumore di fase, un parametro cruciale che è direttamente collegato alle prestazioni del sistema Phased Array. E' stata fatta un'analisi dettagliata sulla minimizzazione del rumore di fase e sono stati realizzati dei VCO in SiGe operanti in banda K (18-27 GHz). I VCO mostrano un romore di fase che arriva a -137 dBc/Hz a 10 MHz di offset dalla portante. Questo risultato è superiore allo stato dell'arte se confrontiamo con gli altri VCO operanti in banda K e realizzati in Silicio. Solo i VCO relizzati con semiconduttori compositi hanno prestazioni migliori in termini di rumore di fase. Ad ogni modo, il costo di queste tecnologie è drammaticamente più alto.
In conclusione, il lavoro dimostra la fattibilità di realizzare blocchi circuitali ad alte prestazioni per i sistemi Phased Array in Silicio. La possibilità di integrare l'intero sistema Phased Array sullo stesso chip porta ad una drastica riduzione dei costi, superando la barriera che ha fermato lo sviluppo di questo approccio in molte applicazioni negli anni precedenti. Questo è un punto cruciale per lo sviluppo della prossima generazione di comunicazioni ad alta velocità di dati e sistemi radar ad alta precisione sia militari che automotive.

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Chapter 1

Introduction to Phased Array Systems

The evolution of communication system standards, the demand for ever higher data-rates and the continued rise of the number of wireless link users, leading researchers to develop new ideas to achieve these results keeping a cost of communications systems relatively low. The use of phased array systems allows to increase the system performance at the expense of greater complexity and costs.

Phased array antenna has bees used in the past in military and aerospace applications, where the complexity and the high costs are not an issues. In recent years, thanks to the technology development, it is possible to integrate in the same chip parts of the phased array system leading to a huge cost reduction. Accordingly to this, phased array systems are being heavily introduced in commercial applications like Cellular Basestation, Point-to-Point Wireless Link and Automotive Radar; the researchers are then encouraged to focus their attention in this field. Literature shows several works where multiple phased array channels are integrated into the same substrate [1], [2].

Chapter 1 gives an overview of the phased array system, starting from the theory and mathematical formulations that describe the working principle, Section 1.1. The applications and the commonly used architectures are presented respectively in Section 1.2 and 1.4 respectively. Section 1.5 gives a description of the issues relative to phase errors in the phased array channels and Section 1.6 reports a brief presentation of the technology evolution in these years explaining how this evolution can help the rapid diffusion of the phased array system in commercial applications too.

1.1 Description and Working Principle

Phased array systems exploit the use of multiple antennas to increase the directivity of the equivalent antenna resulting in a greater resilience to the spatial interference, an improvement of the signal-to-noise ratio and reduced power amplifiers constrains [3]. Fig.1.1 illustrates the concepts in the case of one-dimensional array.

Let's consider a linear array of isotropic radiating elements properly spaced d between each

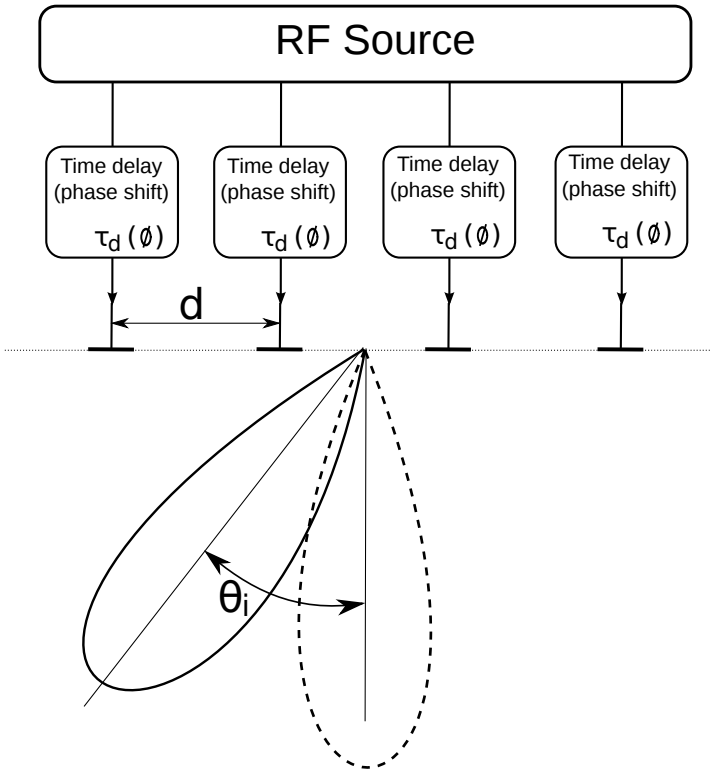

Fig. 1.1 Phased array working principle.

one of them: if a signal is applied at the same time for each element, the resulting irradiated field follows the array factor described by the Equation 1.1:

$$E(\theta) = \sum_{i=1}^{N} A_i \cdot exp\left[j \cdot 2\pi \cdot \frac{d}{\lambda} \cdot i \cdot (sin(\theta)) \right] \tag{1.1}$$

where A_i is the amplitude of the radiating element with index i, θ is the scanning angle, N is the number of antennas and λ is the wavelength. In this case the irradiated field has his maximum value at $\theta = 0°$. The shape of the field is illustrated as instance in Fig. 1.2 (a).

If a phase shift is introduced between the radiating elements, (the signal radiated from the

i-th element has a phase shift ϕ respect to the signal radiated from the previous one), the array factor of the antennas array can be evaluated by the Equation 1.2

$$E(\theta) = \sum_{i=1}^{N} A_i \cdot exp\left[j \cdot 2\pi \cdot \frac{d}{\lambda} \cdot i \cdot (sin(\theta) - \phi) \right] \tag{1.2}$$

In this case the field has a maximum at the incidence angle θ_i that is related to the phase shift ϕ through the Equation 1.3:

$$\phi = \frac{2\pi d \cdot sin\theta_i}{\lambda} \tag{1.3}$$

In this calculations the hypothesis of narrow band system has been done. In a general case, time delay τ_d between radiating elements is evaluated to determine the pointing direction of the phased array system.
If τ_d is related to the distance d between the elements through the Equation 1.4, the equivalent pattern shows a maximum at the angle θ_i.

$$\tau_d = \frac{d \cdot sin\theta_i}{c} \tag{1.4}$$

where c is the speed of light.
Hence it is possible to change the direction of the main beam varying the delay τ_d or the phase shift ϕ between the elements.
With the use of a processor that controls the time phase shift (time delay) units, the beam can be easily electronically steered. Differently, the mechanical approach is very slow and it need a lot of periodical maintenance, moreover the system cost is higher. Rapid beam steering gives for example the ability to track a mobile device that is moving in a car (base station applications) or let a missile to follow a plane (military radar applications).
Further simplifications can be done in order to better understand the behavior of the antennas array. Let's now consider the array to be uniformly excited, i.e. all the radiating elements have the same amplitude signal ($A_i = A$), and with phase shift $\phi = 0°$. At this point we can use the identity expressed by the Equation 1.5:

$$\sum_{i=1}^{N-1} c^n = \frac{c^N - 1}{c - 1} \tag{1.5}$$

The array factor in Equation 1.1 can then be described by the Equation 1.6:

$$E(\theta) = \frac{sin\left[N \cdot \pi \cdot \left(\frac{d}{\lambda}\right) \cdot sin\theta\right]}{sin\left[\pi \cdot \left(\frac{d}{\lambda}\right) \cdot sin\theta\right]} \tag{1.6}$$

The array factor is usually evaluated as a normalized power: the radiation pattern is equal to the normalized square of the amplitude [4], as described in Equation 1.7:

$$G(\theta) = \frac{sin^2\left[N \cdot \pi \cdot \left(\frac{d}{\lambda}\right) \cdot sin\theta\right]}{N^2 \cdot sin^2\left[\pi \cdot \left(\frac{d}{\lambda}\right) \cdot sin\theta\right]} \tag{1.7}$$

Let's for example see the radiation pattern of an array with $N = 20$ and $\phi = 0^\circ$ in Fig. 1.2 (a). In Fig. 1.2 (b) the incident angle is $\theta = 10^\circ$. In Fig. 1.2 (c) is plotted the radiation pattern for an array with $N = 60$ radiating elements, a reduced width of the main lobe is observable, as a consequence, the directivity of the phased array system is increased.
The half power beam-width is one of the properties of the phased array system and gives an idea of the directivity of the antennas array. It is related to the resolution of the system if the antennas array is used as a radar, typical in military and aerospace applications as described in detail in Section 1.2.1. Practically half power beam-width is the quantity $2 \cdot \theta$ at the point where the main lobe attenuation is 3 dB.

Looking the Equation 1.7, the directivity raises with the size of the array: $D = N \cdot d$. Accordingly to this, another way to increase the directivity is to increase the distance d between the radiating elements. The radiation pattern plotted in Fig. 1.2 (d) corresponds to an antennas array with $N = 20$ but $d = \frac{3 \cdot \lambda}{2}$. The size of the array is then the same of the case plotted in Fig. 1.2 (c), but in that case d was kept constant and N increased by 3 times. In the case described by Fig. 1.2 (d), grating lobes appear in the radiation pattern. The condition for no grating lobe being visible is expressed in Equation 1.8:

$$\frac{d}{\lambda} < \frac{1}{1 + |sin\theta|} \tag{1.8}$$

Grating lobes must not be visible, they cause a drastic reduction of the signal-to-interference ratio. Usually the distance between the radiating elements is set to $d \leq \frac{\lambda}{2}$ and the directivity of the array is then set by the number of antennas N.
Another important properties of the antennas array is the intensity of the first side lobe, that is related to the interference attenuation [4]. The ideal radiation pattern would have no side lobe, (only the main lobe appears in the array factor) as a consequence, interferences coming from wrong direction are suppressed and there is more relax on the SNR system requirements.
The type of array illumination determines the attenuation of the first side lobe [4]. In Fig. 1.3

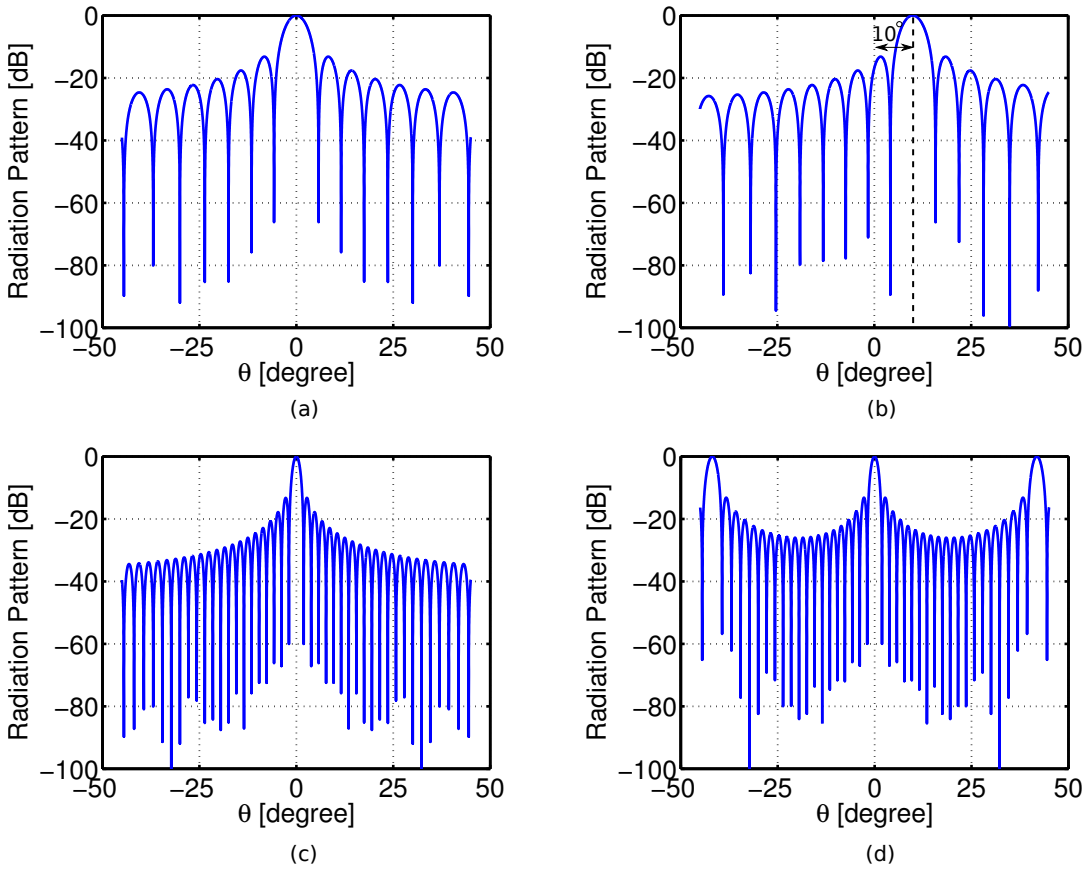

Fig. 1.2 Radiation Pattern: (a) $N = 20$, Incident angle $= 0°$, $d = \frac{\lambda}{2}$, (b) $N = 20$, Incident angle $= 10°$, $d = \frac{\lambda}{2}$, (c) $N = 60$, Incident angle $= 0°$, $d = \frac{\lambda}{2}$, (d) $N = 20$, Incident angle $= 0°$, $d = \frac{3 \cdot \lambda}{2}$.

(a) and in Fig. 1.3 (b) is depicted respectively the uniform and triangular array illumination. In the case of uniform array illumination the attenuation is 13.2 dB respect to the maximum of the main lobe as depicted in Fig 1.4 (a). If a triangular illumination is applied to the antennas array, the attenuation of the first side lobe is 26.4 dB, therefore the communication system has a greater resilience to the interferences. The drawback of the triangular array illumination is an increased half power beamwidth, then a reduced directivity. In Fig. 1.4 (b) is depicted the radiation pattern for a triangular illuminated antennas array with $N = 20$.

Antenna sidelobes are then reduced by tapering the array excitation so that elements at the array center are excited more strongly than those near the edge. Other types of low-side-lobe array illumination is reported in literature, for example *Taylor*-illumination gives 40 dB first side lobe attenuation [5]. Variable gain amplifier is commonly used to ensure different amplification for each radiating element, a detailed description of the VGA design

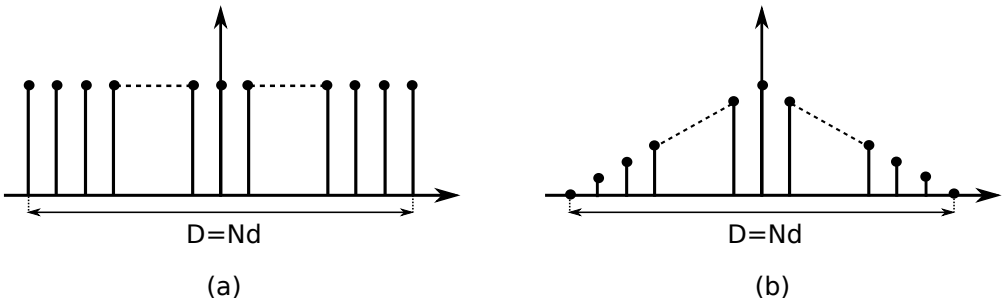

Fig. 1.3 Example of array illumination: (a) Uniform, (b) Triangular.

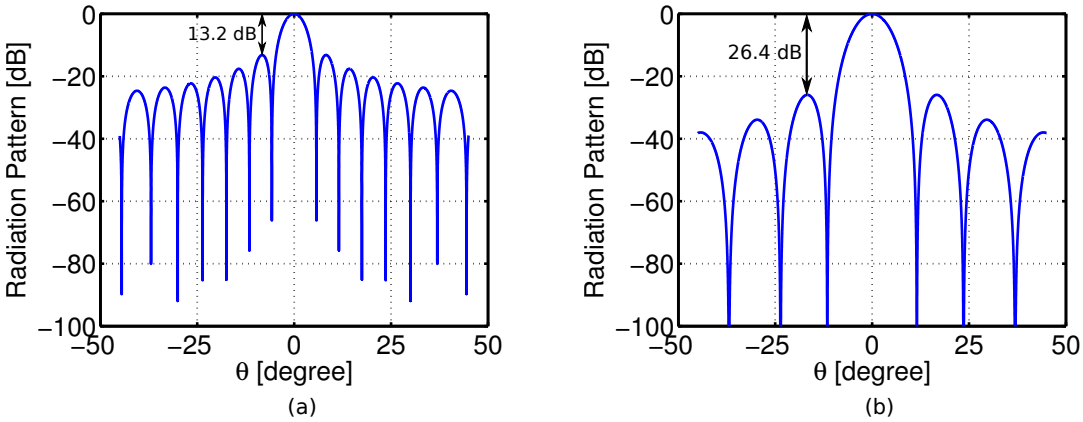

Fig. 1.4 Radiation Pattern, $N = 20$: (a) Uniform illumination, (b) Triangular illumination.

is described in Chapter 2.

Position of the nulls in the radiation pattern is an important phased array system feature [6]. Signal-to-interference ratio can be improved if nulls are close to the main beam or if they are placed in a particular angular position where there is some strong interference. Nulls position can be controlled by algorithms that vary phase and gain of each phased array channel [7]. In common applications planar array are used instead of linear array. The basic principle of beam forming and beam scanning discussed above for linear arrays can be readily extended to planar arrays [8].

1.2 Applications of Phased Array Systems

Looking at the history, the initial application was satellite surveillance in 1958 [9]. The development of phased arrays for a wide variety of military missions had started during cold war. Firsts phased array systems was operating at frequencies close to 900 MHz, the antennas array size was tens of meters and the system complexity and costs were very high. More commercial and popular applications are emerged in the 2000s when the technology evolution allowed to integrated parts of the phased array system into the same chip leading to a huge cost reduction.
5G Communication standard is one of the possible phased array application [10]. 5G (5th generation wireless systems) is the next generation of mobile telecommunication standard beyond the current 4G-Advanced standard. 5G should be rolled out by 2020 to meet business and consumer demands. 5G should feature data-rates of several tens of megabits per second for tens of thousands of users and more than one gigabit per second will be offered simultaneously to many workers on the same office floor. With 5G the coverage should be improved and signaling efficiency should be enhanced [10]. High directivity antennas and millimeter-wave are two key points to help reaching these goals.
In the following subsections there will be a brief overview of the most important phased array system applications.

1.2.1 Military Radar

Military researchers were the first to deal with antennas array in radar detection system. Phased array radar systems are mainly used by warships. Because of the electronic beam steering rapidity, phased array radars allow a warship to use one radar system for surface detection and tracking (finding ships), air detection and tracking (finding aircraft and missiles) and missile uplink capabilities.
Before using these systems, each surface-to-air missile in flight required a dedicated fire-control radar, which meant that ships could only engage a small number of simultaneous targets. The evolution let to a wavelength reduction and then the possibility to realize more compact phased array systems. Accordingly to this, phased array systems has been installed on military planes, as depicted in Fig 1.5. In these years phased array systems can also be used to control missiles during the mid-course phase of the missile's flight. During the terminal portion of the flight, continuous-wave fire control directors provide the final guidance to the target. Because the radar beam is electronically steered, phased array systems can direct radar beams fast enough to maintain a fire control quality track on many targets simultaneously while also controlling several in-flight missiles.

Summarizing, phased array approach has been highly implemented in military applications thanks to its three most important features:

- High directivity;
- Agile electronic beam steering;
- Multi-function operation by emitting several beams simultaneously.

Fig. 1.5 Phased array radar installed to a military plane.

1.2.2 Satellite Communications

Phased array systems have also taken hold in many Satellite Communications. A typical ground station for NASA's low-earth orbiting (LEO) satellites utilizes a single large (10 m – 11 m) dish antenna, and tracks a single satellite at a time by mechanically scanning the antenna through as much as 160° [11]. The down-link supports data rates ranging from 2 kbps up to 150 Mbps. To maximize contact with these polar-orbiting satellites, the ground stations are close to the poles. The ground stations cost from 2.4 millions dollars each to build and have an associated high maintenance cost. With the use of phased array systems, a remotely programmable ground station can be installed, with ideally no moving parts, in non-polar regions, and with a cost of less than a tenth of the cost of a current ground station to build and maintain [11]. Instead of a single dish, the ground system would comprise a number of phased arrays with small-to-moderate aperture sizes, and the phased array outputs would be adaptively combined to maximize the signal-to-interference-and-noise-ratio (SINR) of the desired satellite transmission. The main challenge of these systems is the physical layer, that

is, the design of the RF front end and digital signal processing of the phased array outputs. Phased array station will not support the highest data rates now possible with a large dish, however, since more of the ground stations would be deployed, the data could be downloaded in a distributed manner as the satellite passes over a series of ground stations. The phased array architecture is capable of rapidly and electronically controlled reconfiguration, to enable fast switching from one satellite to another within the same constellation or simultaneous communication with multiple satellites [11].
In these years the develop of phased array systems for satellite communications is widely employed and studied. Two phased array technologies are being investigated by researchers at NASA's Glenn Research Center and at University of Colorado [11]. One of these, the space-fed lens array [12], is composed of a feed array and a radiating array with each corresponding element pair interconnected by transmission lines of different lengths to radiate a plane wave in the forward direction. The other of these, the reflectarray, has a surface containing integrated phase shifters and patch radiators, it is illuminated by a single feed at a virtual focus. The signal passes through the reflect-mode phase shifters and is re-radiated as a collimated beam in essentially any preferred direction in the hemisphere in front of the antenna.
Both approaches provide electronic beam steering, have no moving parts, and promise low cost.

1.2.3 Cellular Basestation

The advantages of a directive base station have been know for many years [13]. In the modern base station mobiles are tracked by pencil beams as they cross through a cell. In the past these systems with tracking pencil beams have not been realized due to the potential cost and complexity of implementing such a system. The approach which appears to have the greatest potential for achieving the pencil beams is an electronic scanning phased array antenna.
An example of modern base station cellular antenna is shown in Fig. 1.6. Depending on where the mobile is located in the cell, a number of radiating elements will be assigned to that mobile. Each of these allocated elements will receive a phase shifted version of the baseband signal, which will add constructively at the mobile. As the mobile moves through the cell the phase shifters will be adjusted, and new radiating elements will be assigned to the mobile. To minimize co-channel interference a systematic scanning procedure can be utilized. If the scanning process is coordinated with the co-channel base stations, we can avoid the same channel beams pointing directly at each other. This requires the mobile telephone switching office to keep track of the beam positions. The base station dynamically defines a restriction region which the co-channel beam is not allowed to scan. If the beam approaches

the restricted region, a different channel can be automatically selected for communications. This description give an idea of the basestation operations, remarking the importance of the phased array system for this application.

Fig. 1.6 Example of base station antennaes.

1.2.4 Point-to-Point Wireless Link

It is believed that the emerging gigabit wireless personal communication systems at 60 GHz will be the first product with a large commercial market in the millimeter-wave frequency band [14]. Phased array systems can play a significant role in the development of these systems. Spatial selectivity of phased array beams can increase the channel capacity of the gigabit wireless personal communication systems to achieve data-rates that have not been possible before. Furthermore, phased arrays can facilitate the deployment of these systems by significantly reducing their power consumption through more efficient power management. It is challenging to generate high power levels using the low cost commercial integrated circuit technologies. Exploiting phased array can alleviate this problem by providing beam forming and increasing the radiation gain in a desired direction. This will obviate the need for prohibitively large output power levels from millimeter-wave power amplifiers. Finally, more reliable and robust communication links can be achieved through mitigating the problem of co-channel interference and by suppressing the signals emanating from undesirable directions. As reported in Section 1.6, integrated circuit technologies now show a promising performance at mm-wave frequencies. Low cost, high integration density of the existing technologies allows for a system-on-chip implementation of mm-wave systems, and is expected to provide a great opportunity for application of phased array systems in the next generation of wireless communication networks.

1.2.5 Automotive Radar

Another important application that can take advantage from phased arrays is automotive collision avoidance radar or adaptive cruise-control technology [15]. As described in Fig 1.7, using radar sensors in the car can provide the driver with several driving-aid functions such as automatic cruise control (ACC), parking aid, blind spot detection, and side collision warning [15].

High resolution radar systems having powerful signal processors capable of advanced image processing can further enable object classification, roadside detection, and prediction of the lane-course, therefore enabling intelligent interpretation of traffic scenes [16]. Finally, autonomous driving can be realized by combining short-range radar, global positioning techniques, and wireless communications. Every minute, on average, car accidents take life of at least one person. This results in more than 42000 deaths and 3 millions injuries a year in the United States only [17]. The financial damages caused by car accidents can be as high as $1-3$ percent of the world gross domestic product every year. Collision avoidance radars can reduce these staggering numbers.

The current collision avoidance radars could is quite expensive and is an option only on luxury models. Developing low cost integrated phased array systems may encourage the introduction of the radar technology in ordinary cars too.

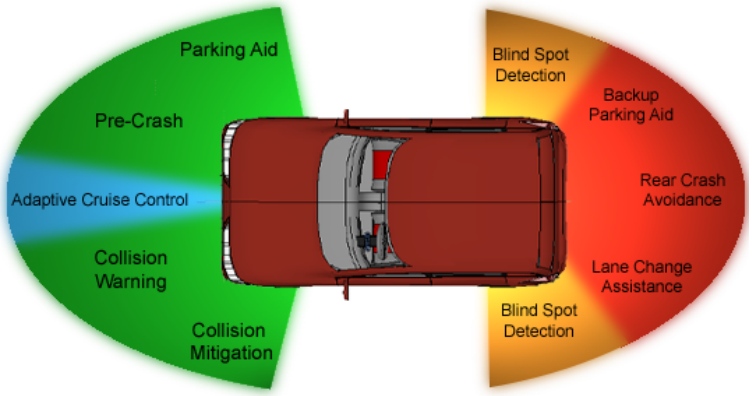

Fig. 1.7 Car radars.

1.3 Phased Array Building Blocks

A typical phased array system block diagram is described by Fig. 1.8. If N radiating elements represent the antennas array, the system consists of N different paths. Each path is composed by a variable gain amplifier (VGA) and a variable delay element. The time-delayed signals from the different paths add coherently through the power combiner. In a conventional implementation only two path are combined at a time. This results in a total $(N-1)$ power combiner and a combiner depth of $log_2 N$, this can cause huge losses if the array has many elements. Furthermore, the large amount of required combiners sets the area consumption as an important constraint.
If the antennas spacing is sufficient enough to consider uncorrelated the noise of each antenna from that of the other antennas, the noise adds incoherently, resulting in an SNR improvement [3]. After power combiner the signal is down-converted to intermediate/baseband frequency where it is converted to a digital signal and processed. Three important building blocks are briefly described in the Subsections 1.3.1, 1.3.3, 1.3.2.

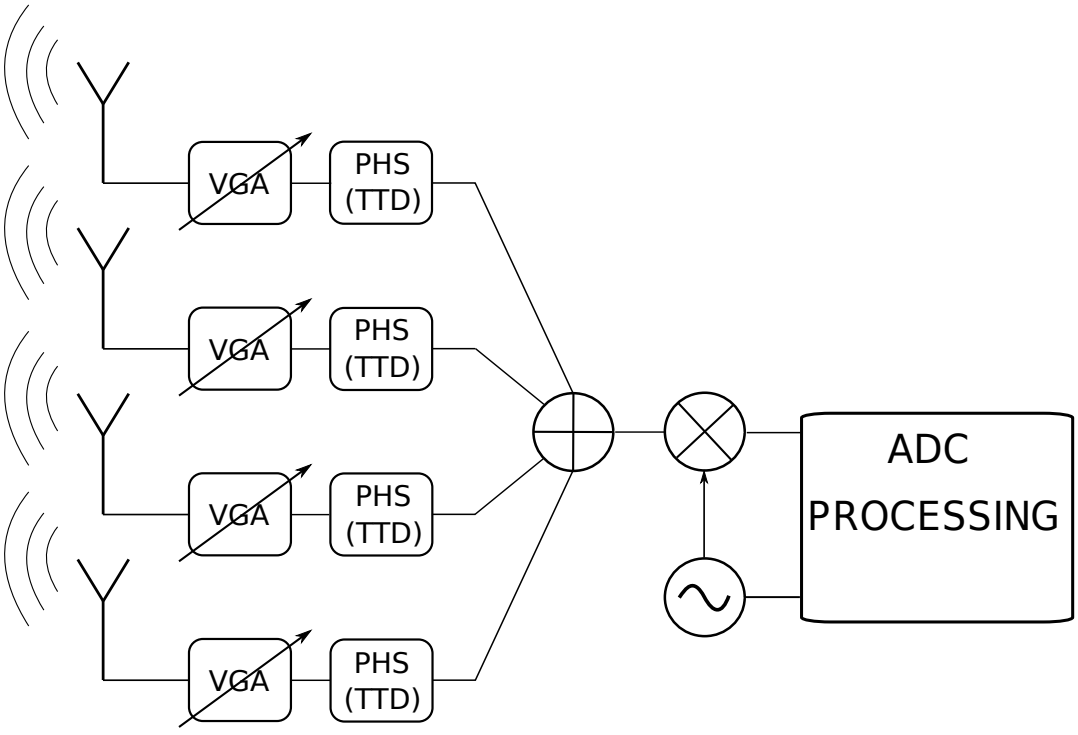

Fig. 1.8 Example of Phased Array (Timed Array) Block Diagram.

1.3.1 Phase Shifter and True Time Delay

The building block that provides the phase shift and time delay is called respectively phase shifter (PHS) and true time delay (TTD). The advantage of using TTD is related to the fact that it is frequency independent, therefore it can be used in wideband systems. However it is not trivial to realize a millimeter-wave TTD. As explained in Section 1.1, in narrow-band applications time delay can be approximated to phase shift that is generated by a phase shifter, which has easier realization complexity respect to the TTD.
Phase controllability at each channel of the phased array system is also exploited to manipulates the radiation pattern, for example to introduce some nulls at certain angular position where the interference are strong [18].

In Fig. 1.8 the phase shifter is implemented at the RF path, which is the most simple and promising architecture in terms of low components count and power consumption, overall when the number of antenna array elements became large as described in Section 1.4. Passive phase shifter implementation is usually preferred over the active one due to the linearity limitations of the active devices in the RF path. Common passive phase shifter designs are based on the switching between all-pass/band-pass circuits as depicted in Fig. 1.9. A design example is reported in [19]. Phase error and linearity degradation can be introduced by the switch when a high number of section are needed. A combination of switchable

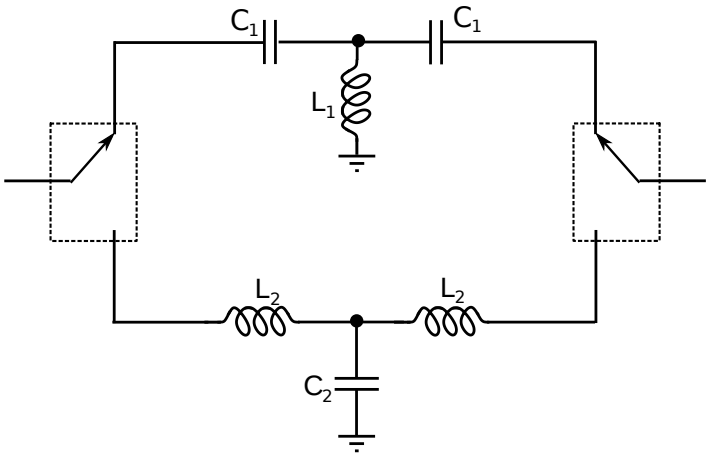

Fig. 1.9 High-pass/low-pass phase shifter topology.

low-pass/band-pass network followed by a continuously tunable circuit can also be adopted to limit the number of sections [20]. Varactor is used as capacitor and the phase shift can be varied adjusting the varactor capacitance. The area consumption for a given phase shift value can be reduced using a phase shifter based on 90° hybrid coupler [19]. However hybrid

coupler can limit the maximum fractional bandwidth.
If the time delay approach is used, true time delay is implemented instead of phase shifter. Conventional passive TTD is based on loaded transmission line [21]. Transmission line are distributed low-pass network showing a constant characteristic impedance. They are commonly used to connect two circuits when the connection length approaches the wavelength of the signal and they are wideband structures. Disadvantage of this configuration is the large occupied area. Lumped element approach is usually preferred to reduce area consumption [22]. Each section is a LC low-pass filter where L and C are respectively the lumped inductor and capacitor as depicted in Fig. 1.10.

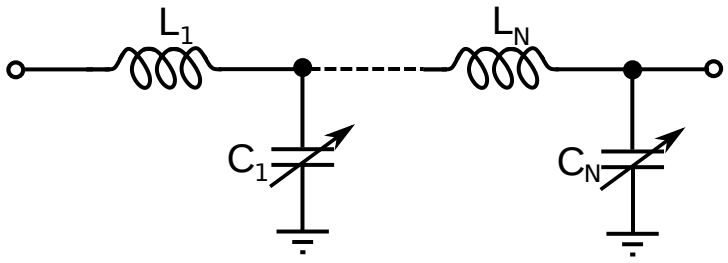

Fig. 1.10 TTD based on lumped elements.

1.3.2 Variable Gain Amplifier

Variable gain amplifier is usually used in each path of the phased array system in order to vary the amplitude of the signal coming from each antenna. This feature give the possibility of non-uniform array illumination, therefore a greater side lobe reduction as explained in Section 1.1. VGA in combination with the PHS adjust amplitude and phase of the signal at each channel of the antennas array following the control algorithms. Algorithms are used for example tho introduce a wideband null on the radiation pattern to increase the signal-to-interference ratio or to track a mobile device [23].
Delay time element can introduce different attenuation for different delay settings, for this reason VGA is also implemented in each phased array path to compensate the TTD or PHS non-ideality. Moreover, VGA is used to compensate for the possible attenuation caused by the transmission lines that connect each radiating element to the amplifier.
A deep description of the VGA design for *X*-band and *K*-band applications both with an analysis and a description of the phase error is presented in Chapter 2.

1.3.3 VCO

A Voltage controlled oscillator is a system that generates an oscillating signal. Oscillation frequency is varied by the input tuning voltage. VCO is usually part of a phased-locked-loop and give the frequencies to the mixer to down-convert or up-convert the signals in a general communication system. Ring oscillator and LC-oscillator are the most used ways to realize VCO [24]. In RF communications systems, LC-oscillator is commonly implemented due to its high performances [24]. Integrated LC-VCO usually can be described by Fig. 1.11. Oscillation is generated in the resonant network and it is sustained by the negative resistance. The latter is realized by active devices (BJT, CMOS or other technologies) and there are various possible configurations. Resonant network is called tank, inductive element is made

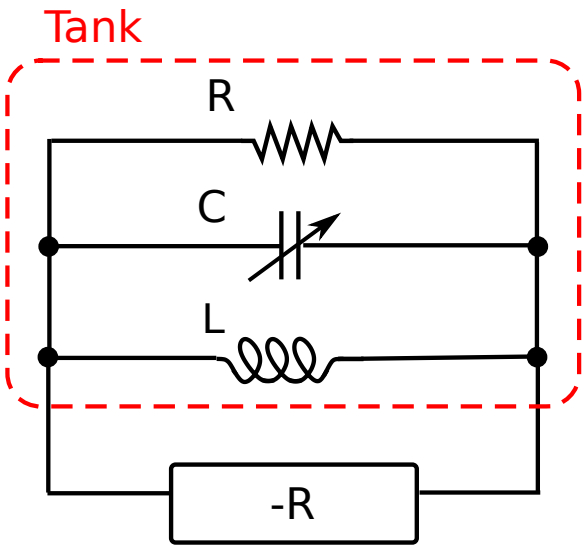

Fig. 1.11 Electric VCO representation.

by an inductor, transformer or a transmission-line. Variable-capacitance element is realized by a varactor that is used to change the frequency accordingly with an input voltage. The difference between the maximum and minimum oscillation frequency is called tuning range. Resistive part (R) indicates the losses of the tank that must be compensated by the active devices in order to start-up the oscillations.
The main parameter of the VCO is the phase noise that is the result of small random fluctuations or uncertainty in the phase of an electronic signal. An ideal oscillator produces a perfectly-periodic output that is viewed as an impulse in the frequency domain. The noise of the oscillator devices randomly perturbs the zero crossing of the signal. This perturbation

can be modeled through the Equation 1.9:

$$x(t) = Acos[2\pi f_c t + \phi_n(t)] \tag{1.9}$$

where $\phi_n(t)$ is a small random phase quantity that deviates the zero crossings from integer multiple of the signal period $T_c = \frac{1}{f_c}$. The consequence of the random frequency perturbations results in a broadened spectrum as depicted in Fig. 1.12. In order to quantify phase noise, as shown in Fig. 1.12, we consider 1 Hz bandwidth of the spectrum at an offset frequency Δf, measure the power in this bandwidth, and normalize the result to the carrier power. The phase noise unit is dBc/Hz, where dBc means normalization of the noise power to the carrier power.

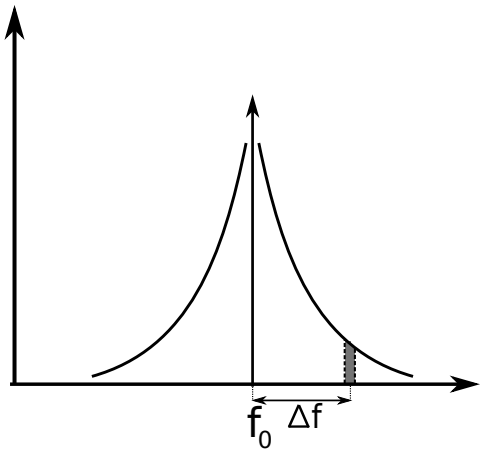

Fig. 1.12 Phase noise of a signal with frequency f_0.

Phase noise is a fundamental limitation in the performance of systems. This shows up in radar and communications as loss of sensitivity, in imaging as lack of definition and in digital systems as higher bit error rate. In Chapter 3 some low phase noise K-band VCO are presented with a detailed description of the phase noise optimization techniques and technology limitations.

1.4 Phased Array Architectures

Silicon technology evolution for integrated circuits have resulted in very fast transistors with cutoff (unity current gain) frequencies above 300 GHz as highlighted in Section 1.6. However, transistor speed is only one of the parameters affecting system operation. Additional constraints imposed by the low breakdown voltages, losses of integrated passive elements, low power consumption, cost and area have important hearings on overall system performance. The system architecture choice plays an important role on the phased array system design [8]. For example, a variable delay element should have the same attenuation for different delays, in fact an amplitude error will lead to distortion when the signals are combined. Such delay elements are quite challenging to implement at RF frequencies, an implementation at baseband frequency would be more easy at the expense of area consumption.
Four different phased array architectures are illustrated in Fig. 1.13. The phase shift can he provided at RF (Fig. 1.13 a), intermediate frequency (Fig. 1.13 b), or digitally (Fig. 1.13 c). The phase shift can also be provided by down-converting the signal in each path with a phase shifted LO signal (Fig. 1.13 d). Each configuration has some advantages and disadvantages and the final choice come from the trade-offs in power-consumption, area, capacity, reliability and technology limitations.
Power consumption can be minimized placing phase shifters in RF path as in Fig. 1.13 (a) and then combining the signal at RF. With such configuration only one IF stage is needed. Additionally, the combination of all the path in RF domain allows to relax the linearity requirements of the IF stages.
Realizing phase shifters with low loss and constant attenuation for different phase settings is challenging at RF frequencies [3].Phase shifter realized at IF frequencies increase power consumption because in an N element receiver, there will be N downconversion mixers before the phase shifters as depicted in Fig. 1.13 (b). Moreover, implementing the phase shifters at IF frequencies drastically increase the chip area.
Fig 1.13 (c) describes a phased array architecture where all the phase shift and amplitude control operations are realized by the digital processor unit. This increases the flexibility of the system. However, such a system presents high power consumption, it is essentially equivalent to N receivers operating in parallel. Also, analog-to-digital converter must be high performance in order to provide accurate delay. As compared to a signal path implementation at RF, IF, or digital signal processing, a phase shifter in the LO stage is relatively easier to implement (Fig. 1.13 d) [3]. Since the downconversion mixers have their best performance when they are hard-driven, the LO stage should preferably be operated in saturation. Noting that the output of the VCO has constant amplitude as well, the amplitude and phase variations can be completely decoupled. Therefore, each path will have a constant gain irrespective

of phase shift. Moreover, since in this architecture there is only one IF stage, the power consumption is reduced respect to the IF phases shift architecture.

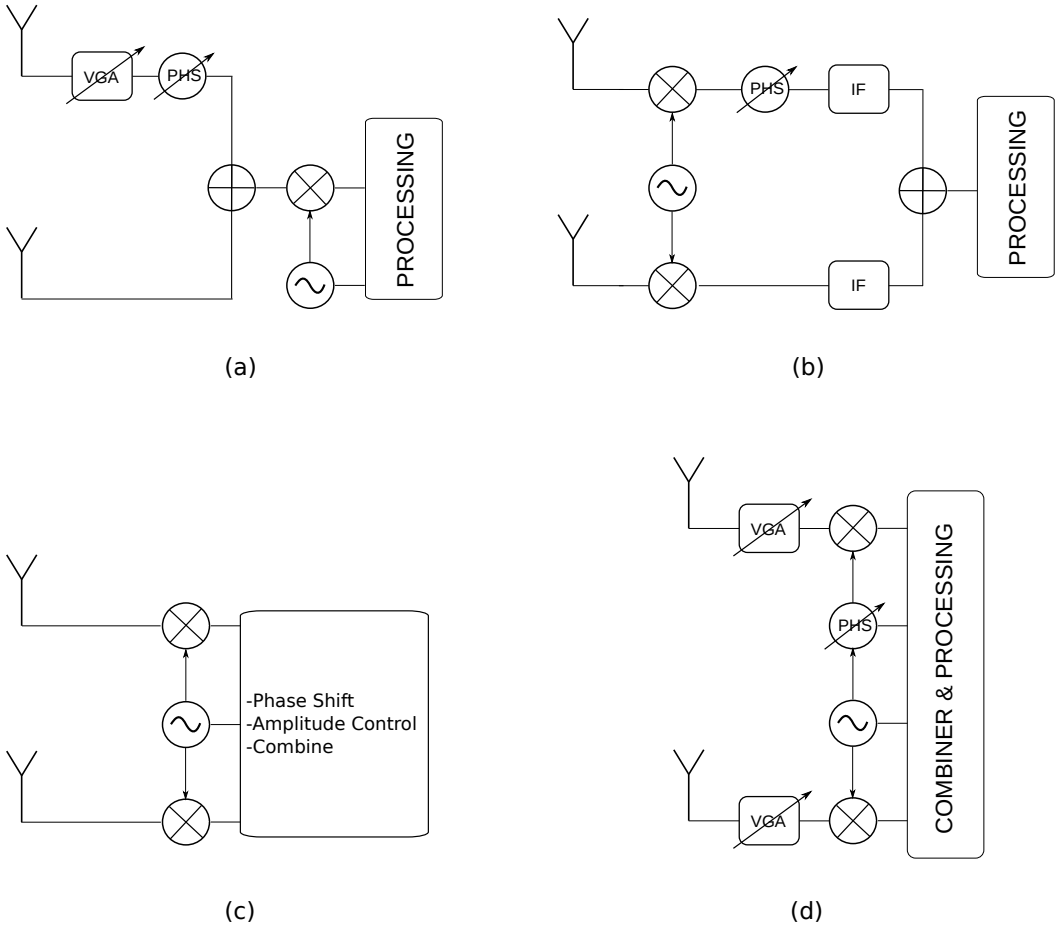

Fig. 1.13 Phased Array Systems Architectures.

1.5 Phase error issues

Amplitude control and phase control in each phased array channel give the possibility to optimize the radiation pattern increasing the directivity, reducing the side lobes intensity and regulating the null positions [7]. In a phased array basestation for example, the signals received by each antenna element are weighted and combined to create a beam in the direction of the mobile device. Phase shifters and variable gain amplifiers work coordinately in order to adjust the antenna radiating pattern to enhance the desired signal, null or reduce interference, and collect correlated multi-path power. Electronic control can adjust their pattern to track mobile user if a direction of arrival (DOA) algorithm is used [6].
The techniques of placing nulls in the antenna patterns to suppress interference and maximizing antennas array gain in the direction of desired signal has received considerable attention in the past and still of great interest [6], [23]. These techniques are very important in communication system, and radar applications for maximizing signal-to-interference ratio (or signal to interference and noise ratio). Proper operation of the algorithms that realize the radiation pattern is guaranteed only if the VGA and PHA (or TTD) have an almost ideal behavior. Phase of the signal should not change if the gain is varied in the VGA and attenuation should not vary when the phase is varied in the phase shifter.

Some examples of phase error effects in a particular case where the array is uniformly illuminated are reported in Fig. 1.14. The red dasher curve represents the radiation pattern

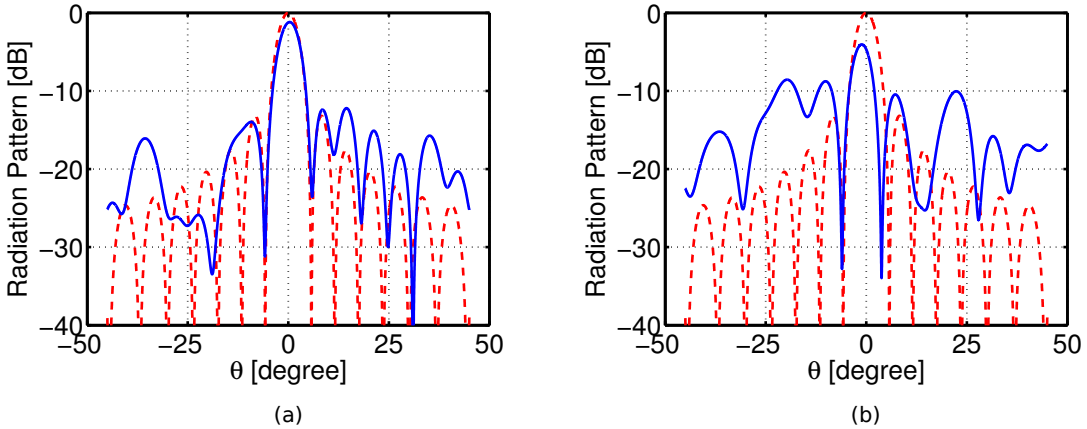

Fig. 1.14 Radiation pattern: (a) Phase error $\mu = 0°$, $\sigma = 30°$ (b) Phase error $\mu = 0°$, $\sigma = 60°$. Dashed line indicate the radiation pattern without phase errors.

of an uniformly irradiated antennas array where $N = 20$, $d = \frac{\lambda}{2}$. In Fig. 1.14 (a) the blue solid line describes the radiating pattern of the same antennas array but random phase error is introduced to each radiating element. Phase error in this case comes from a random vector

represented by a gaussian distribution with $\mu = 0°$ and $\sigma = 30°$. Phase error vector used for the simulation is depicted in Fig 1.15. In the x-axis there is the sequence of the radiating elements and in the y-axis there is the random phase error introduced to each element. In Fig. 1.14 (b) instead, standard deviation is greater, in this case $\mu = 0°$ and $\sigma = 60°$. A

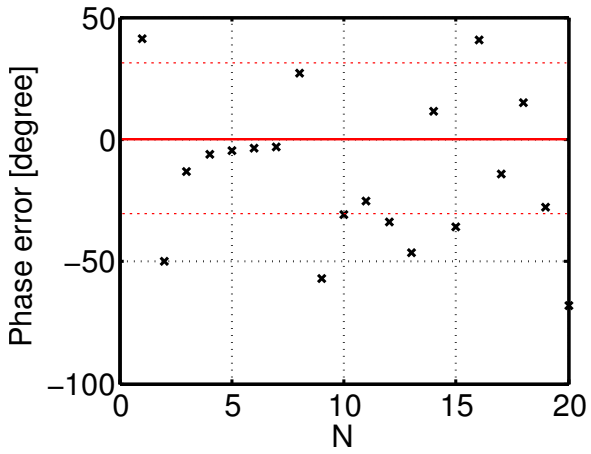

Fig. 1.15 Vector of phase errors introduced in the case of Fig. 1.14 (a), *x*-axis represents the antennas array elements .

substantial phase error deforms the radiating pattern, side lobes have higher intensity then the system has less resilience to the interferences. Beam pointing angular errors can also appear, then the phased array system has an imprecise pointing system, this is fundamental in applications where the phased array is used as a radar. Moreover, the nulls in the radiation pattern disappear or they appear in wrong angular positions (nulls on the pattern are important to filter a strong highly directional interference).

Fig. 1.14 shows a particular case of phase error added to each radiating element. Some statistical simulation have been done in order to see the average behavior. Fig 1.16 illustrates the results of an average taken from 50 tests. In each test random phase error has been introduced in the phased array system. In the case of Fig. 1.16 (a) the phase error is a gaussian vector with $\mu = 0°$, $\sigma = 30°$, in the case of Fig. 1.16 (b), the error is greater: $\mu = 0°$, $\sigma = 60°$. In this case the nulls of the radiation pattern disappear, in fact the nulls come from a particular phase shift between the elements of the antennas array, if this phase shift is varied randomly, also the nulls angular position vary randomly. In this simulations the media of the gaussian vector is $0°$. Anyway, an equal phase error introduced to all the radiating elements does not causes radiation pattern variation, a constant phase offset has no impact, it is easy to see from the Equation 1.2.

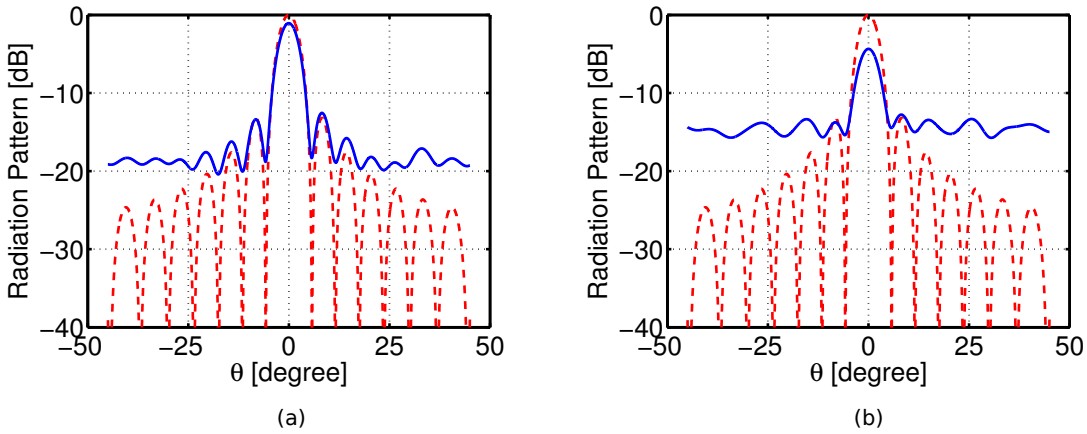

Fig. 1.16 Radiation pattern of an antenna array with phased error, average of 50 tests : (a) Phase error $\mu = 0°$, $\sigma = 30°$ (b) Phase error $\mu = 0°$, $\sigma = 60°$. Dashed line indicate the radiation pattern without phase errors.

Phase error issues are the same also in the case of non-uniform array illumination with the addition that there could be a proportionality between the phase errors and the various gain settings of the variable gain amplifiers. Fig. 1.17 shows average radiation patterns of triangular irradiated array as depicted in Fig. 1.4 (b). Here the number of antennas is $N = 40$ and $d = \frac{\lambda}{2}$. In the case depicted in Fig. 1.17 (a) the phase error comes from a gaussian variable with average $\mu = 0°$ and standard deviation $\sigma = 30°$. In the case represented by Fig. 1.17 (b) the standard deviation is $\sigma = 60°$. Simulations show that nulls in the pattern do not exist anymore, intensity of the main lobe is deteriorated and intensity of the side lobe are increased as in the uniform-illumination case.

Phased array system can have some particular combination of phase errors that destroy the beam pointing precision. Fig. 1.18 (a) describes a special case where the phase error vary increasingly along the antennas array. As in the previous examples the result comes from an average of 50 tests on an array with triangular illumination and 40 radiating elements. In this case the vector of random phase errors introduced has standard deviation $\sigma = 10°$ and the average grows linearly along the antennas array. An example of phase error vector is plotted in Fig. 1.18 (b). Starting from the begin of the array, the phase error increases with an average of 5° between one element and the other, this causes an angular beam pointing error. Angular beam pointing error are important in radar military applications. For example, if a system controls the presence of airplanes at a distance of 10 Km and the phase error gives an angular beam pointing error of 1°, then using the approximation $sinx \approx x$ the spatial error at 10 Km is 174 m hence the system could not acquire the right airplane position.

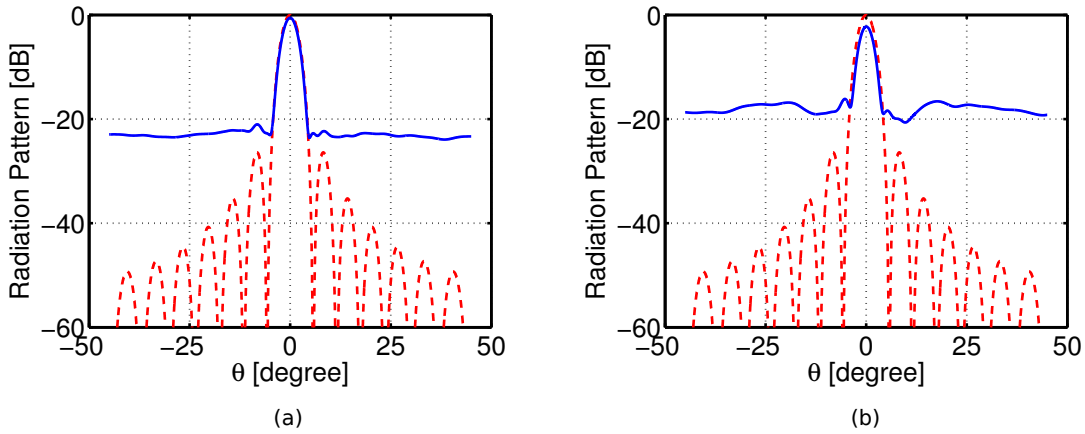

Fig. 1.17 Radiation pattern of an antenna array with phased error and triangular illumination, average of 50 tests : (a) Phase error $\mu = 0°$, $\sigma = 30°$ (b) Phase error $\mu = 0°$, $\sigma = 60°$. Dashed line indicate the radiation pattern without phase errors.

Phase errors can be caused by the non-ideal behavior of phase shifters and variable gain amplifiers. Systematic error information can be extracted through a characterization of each building block and calibration algorithms is often used to compensate the errors.
Calibrations greatly increase the complexity of the system an the overall power consumption due to the addition of more digital circuits. Researchers aim is to realize integrated building blocks which have performance close to the ideal behavior. In the Chapter 2 phase behavior of integrated variable gain amplifier is analyzed with the objective to realize a VGA with flat phase characteristic within the entire control range.
The goal is to have an almost ideal building block for a phased array system, hence to facilitate the calibration algorithm and to make effective the algorithms used for the nulls position placement or for the tracking of the mobile devices in the case of basestation [23].

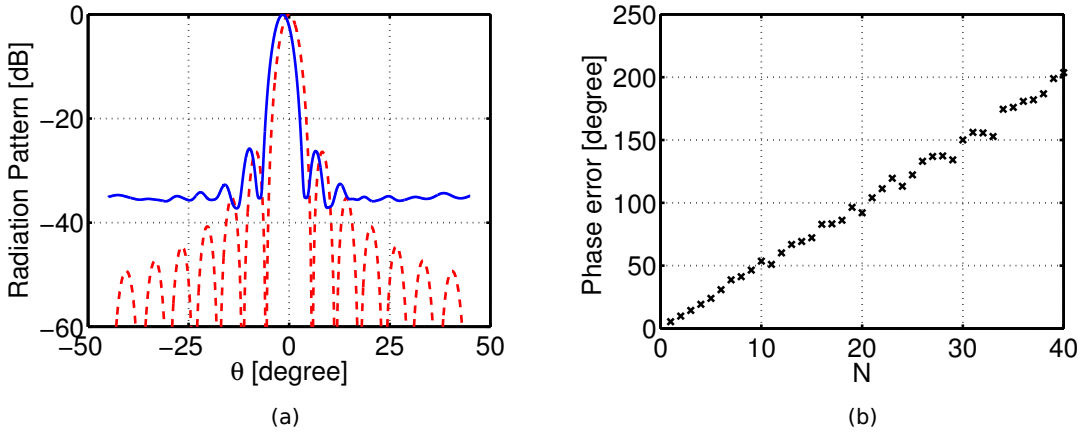

Fig. 1.18 (a) Radiation pattern of an antenna array with phase error and triangular illumination and systematic phase error, average of 50 tests. (b) Example of phase error vector used in the simulation.

1.6 Technology Overview

Number of radiating elements is directly connected to both, directivity and SNR performances. The choice of highly-dense antenna array is therefore very attractive. The demand for even higher data-rate wireless communication systems and for even higher radar resolution leads to even smaller wavelengths. Integrated circuits is then an interesting solution for the implementation of highly-dense phased array systems. In fact they let to reduce the complete system size and complexity, consequently a huge cost reduction.
The integration of all the building blocks obviously has some disadvantages respect to the discrete realization. The performances of integrated systems are lower in terms of loss, noise and linearity. Researchers efforts are then focused on the optimization of the integrated solutions. Silicon technology offers transistors with very high transition frequency, about 300 GHz both in CMOS and bipolar as described in Fig. 1.19. Such devices can be adopted to realize millimeter-wave phased array system [25] keeping relatively low cost and complexity. While being extremely fast, these transistors suffer from several limitations that affect their analog and RF performances. For example, CMOS devices present low supply voltages, this limits the output power and the receiver dynamic range. III/V compound semiconductor offers faster transistors than conventional silicon technologies, moreover they have higher breakdown-down voltages. The drawback of such devices is the extremely high production cost. However when the performance requirement must be high, III/V devices are implemented in the system. Usually they are used in the receiver just after the antenna to realize the LNA with a very low noise figure and high gain. III/V devices are also needed when extremely low phase noise VCO is required.

SiGe and SiGe-BiCMOS technology is very attractive due to its excellent performance and overall cost trade-off. State-of-the-art SiGe BiCMOS technology features cut-off frequencies of about 250 GHz, $f_{max} > 400$ GHz, extended temperature range, high reliability and long process lifetime, this making it a good candidate for mm-wave applications [26].
In addition to lower fabrication cost, SiGe technology is much more easily scaled than conventional III-V technologies. The high f_T, f_{max} achieved at very small devices geometries allows SiGe HBTs to deliver high gain and low noise even at extremely low current densities. This low-power design advantage of SiGe HTBs can help with the package level power dissipation constraints [27]. In consideration of the implementation costs and system integration, standard CMOS process have also attracted great attention in recent year [14].However, SiGe bipolar devices still have lots of advantages compared to CMOS for millimeter wave applications such as lower $1/f$ noise, four times better gm/I_C, four times higher breakdown voltage (for identical f_{max}), then are most useful for circuits like power-amplifiers and to achieve a very low phase noise in VCO's [28]. Moreover SiGe BiCMOS technology offers

the possibility to use MOSFET devices in the same integrated circuit as the HBTs. It is a good candidate to integrate high performance analog/RF circuits with digital circuits on the same substrate. Algorithms for the beam steering, radiation pattern optimization and calibration can then be easily implemented on the same chip reducing the system complexity. Moreover CMOS features can be exploit also for the phased array building blocks, for example CMOS devices behave as better switch than bipolar devices.

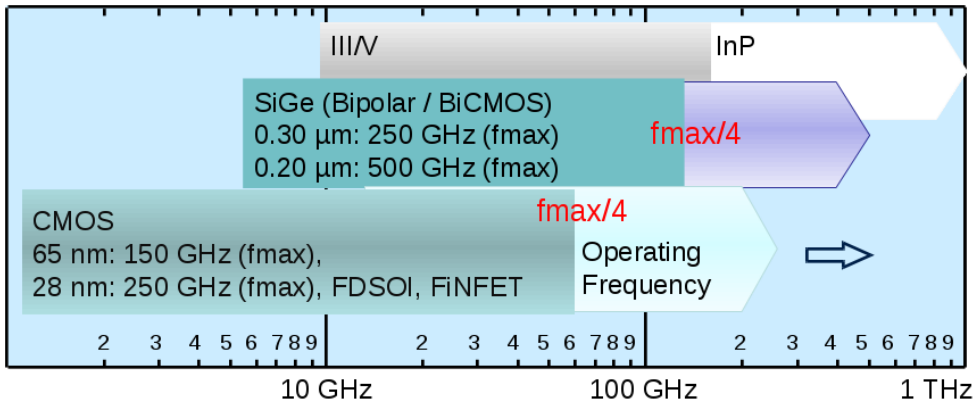

Fig. 1.19 Technology overview .

Chapter 2

Analysis and Design of Variable Gain Amplifiers for Phased Array Systems

2.1 Motivation

Variable gain amplifier is a fundamental building block in a general communication system. In a transmitter it is often advantageous to be able to adjust the power at the power amplifier output. For example, the output power might be increased to minimize interference problems. On the other hand, if the transmitted signal is being received very clearly, the power might be decreased to minimize power consumption in portable products.
Gain controllability is very important in the receivers in general. High gain in receiver path is essential to improve its noise characteristics. But, as the system gain increases, the linearity is degraded. So to guarantee high dynamic range, system gain must be controlled according to its input signal's power level [29].

Linear-in-dB gain control is often preferred to reduce the system complexity. Gain variation can be digitally implemented through switches or it can be implemented with an analog circuits [30]. In this case an analog-to-digital converter will be used to interface the control with the processor unit.

Automatic gain control in the receiver and power control in transmitter are typical examples of applications where the phase characteristics versus gain variation are not taken into account. Anyhow, for applications such as phased array system, feed-forward linearization, and measurement equipment the phase characteristics versus gain variation are very important [31].
As discussed in Section 1.5, phase errors in the phased array channels causes an increment of the side lobes, elimination of the nulls in the radiation pattern and pointing direction errors. A constant phase versus gain variation is a severe requirement for VGA implemented in a phased array system [31]. Of course, the phase deviations generated in a VGA could be corrected in the phase shifter. In turn, the phase shifter may not have a constant gain versus phase. Consequently, recursive adjustments would be required. Hence, any phase variations versus gain control and any gain variations versus phase control have to be avoided to minimize the associated control complexity, response time and power consumption. A brief discussion on the phase behavior in a voltage gain amplifier is introduced in Section 2.2, different possible VGA topologies are described in Section 2.3 with a performance comparison in terms of input matching, gain range variation, noise figure, linearity, power consumption and phase error. Subsequent sections present some VGA design for phased array system with phase error compensations.

2.2 Phase Error in VGA

Phase error indicates the dependence of the phase of the signal from the gain variation. In fact if the phase is independent to the gain variation, phase error will be zero. In a RF building block the phase is evaluated through the S-parameter analysis, hence the phase of S_{21} The gain is expressed as the magnitude of S_{21}. In order to understand the VGA behavior, it can be represented by a transfer function through a small-signal analysis. Fig. 2.1 describe a representation of the VGA with his input and output voltages and currents respectively.

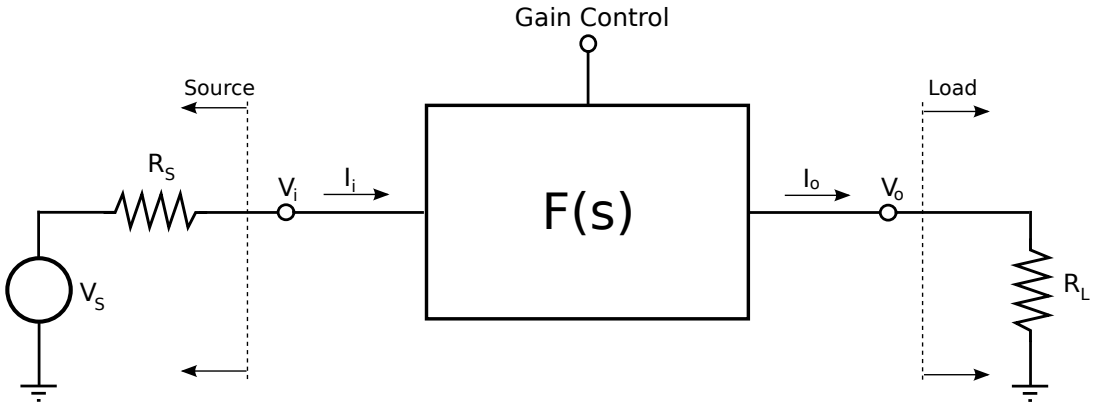

Fig. 2.1 VGA representation.

In an RF system, the source is usually represented by an ideal voltage source with a series resistance of 50 Ω, 100 Ω if a differential system is take into account. VGA source could be the output of a low noise amplifier or directly the antenna. The load is modeled by a 50 Ω (100 Ω) resistance. VGA load is for example the phase shifter or the down-conversion mixer RF-port. Whether the source and load are as explained and the amplifier is matched at the input, voltage ratio between input and output in frequency domain represents the S_{21} of the VGA as expressed in Equation 2.1.

$$F(s) = \frac{V_o(s)}{V_i(s)} \tag{2.1}$$

General transfer function can be described by Equation 2.2:

$$F(s) = \kappa \frac{(1+s/\omega_{z1})\cdots(1+s/\omega_{zN})}{(1+s/\omega_{p1})\cdots(1+s/\omega_{pM})} \tag{2.2}$$

where κ is the DC gain, ω_{z1}, ω_{z2}, ...ω_{zN} represent the angular frequency of the N system zeroes and ω_{p1}, ω_{p2}, ...ω_{pM} represent the angular frequency of the M poles. Let's change the variable $s = j\omega$:

$$F(j\omega) = \kappa \frac{(1+j\omega/\omega_{z1})\cdots(1+j\omega/\omega_{zN})}{(1+j\omega/\omega_{p1})\cdots(1+j\omega/\omega_{pM})} \tag{2.3}$$

At this point, the gain is the magnitude of the transfer function $|F(j\omega)|$ and the phase is $\angle F(j\omega)$. In order to analyze the phase error, sensitivity of phase $\angle F(j\omega)$ to the magnitude of the gain $|F(j\omega)|$ is evaluated in the operation frequency band of the amplifier.
Accordingly with the Bode diagram theory, the phase of each pole is $-\arctan \omega/\omega_p$ and the phase of each zero is $+\arctan \omega/\omega_z$ Hence the total phase $\angle F(j\omega)$ is expressed as in Equation 2.4:

$$\angle F(j\omega) = \sum_{i=1}^{N} \arctan \omega/\omega_{zi} - \sum_{j=1}^{M} \arctan \omega/\omega_{pj} \tag{2.4}$$

In order to understand the phase behavior of the variable gain amplifier we refer to the dependence of the poles and zeroes position from the gain variation. If the phase does not vary when the gain is changed, phase error is zero.

Let's introduce a simple example in order to understand the phase error mechanism. The circuit in Fig. 2.2 is a variable attenuator realized by a resistor, R a variable resistor R_v and an output capacitor C. The transfer function between the output voltage and the input voltage

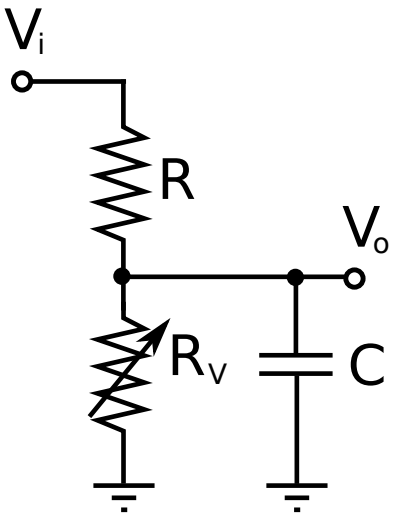

Fig. 2.2 Schematic of a variable attenuator.

is reported in Equation 2.5:

$$\frac{V_o(s)}{V_i(s)} = \frac{R_v}{R_v + R} \cdot \frac{1}{1 + s \cdot \left(\frac{RR_vC}{R+R_v}\right)} \tag{2.5}$$

DC gain κ and the pole frequency ω_p are described in Equation 2.6:

$$\kappa = \frac{R_v}{R_v + R} \qquad \omega_p = \frac{R + R_v}{RR_vC} \tag{2.6}$$

Let's give some value to the components in order to plot an the Bode diagrams and to quantify the phase error.

- $R = 100\,\Omega$;
- $R_v =$ variable resistance from $20\,\Omega$ to $200\,\Omega$;
- $C = 60\,fF$.

With this values, we can calculate the maximum and minimum DC gain: the maximum is when $R_v = 200\,\Omega$ and it is expressed in dB, $\kappa = -3.5\,dB$ and the minimum ($R_v = 20\,\Omega$) is $\kappa = -15.5\,dB$, hence the variable attenuation range is $12\,dB$. The gain variation is plotted in Fig. 2.3 (a). In Fig. 2.4 and Fig. 2.5 magnitude and phase of the transfer function are plotted

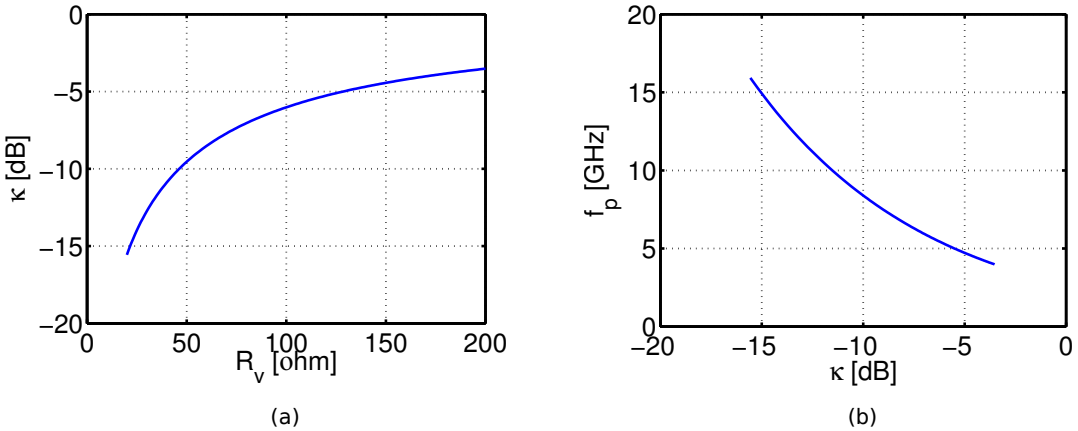

Fig. 2.3 (a) DC gain as function of R_v; (b) Pole frequency f_p as function of the gain κ;

respectively at three different values of the variable resistance R_v: $20\,\Omega$, $100\,\Omega$ and $200\,\Omega$. The phase of the transfer function changes varying the variable resistor, because the pole frequency $f_p = \omega_p/2\pi$ depends from the value of R_v as described in Fig. 2.3 (b).

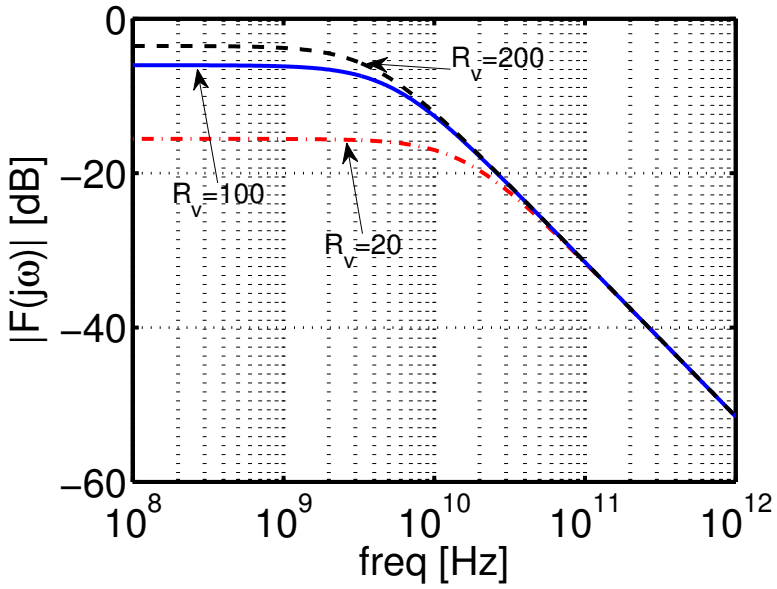

Fig. 2.4 Magnitude of the transfer function $F(j\omega)$ at three different value of Rv.

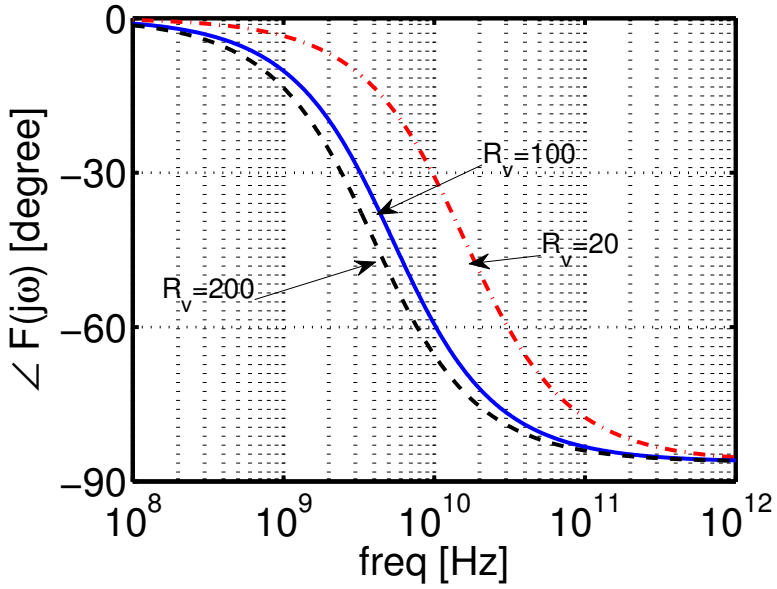

Fig. 2.5 Phase of the transfer function $F(j\omega)$ at three different value of Rv.

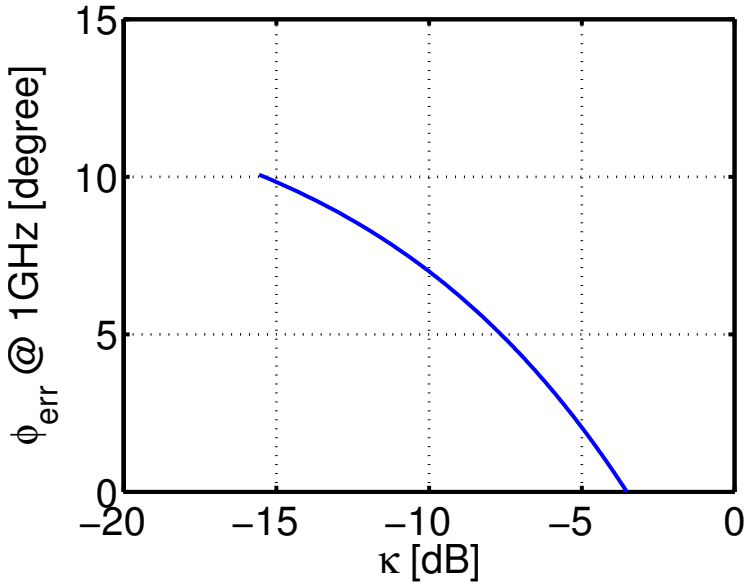

Fig. 2.6 Phase error at 1 GHz versus gain variation.

Phase error is plotted in Fig. 2.6 evaluating the phase differences between the various gain states at 1 GHz. If the phase error is evaluated at frequencies closer to f_p, obviously it will be greater. In this particular case the pole frequency changes from $f_p = 16\,\text{GHz}$ at minimum gain to $f_p = 4\,\text{GHz}$ at maximum gain and the total phase difference is approximately 10°. This simple example has been done just to understand how to calculate and analyze the phase error dependence from the gain variation. In VGA design for phased array application is important to exploit a control gain mechanism that does not change a lot the poles and zeroes position when the gain is varied otherwise the phase error will be huge, above all the pole and zeroes that are close to the operation frequency of the amplifier. Poles and zeroes of the network that realize the operational band of the amplifier for example should be independent from the gain variation.

Phase error performance is then related to the f_t of the devices. Higher f_t is, higher are the pole and zeroes position respect to the operation frequency. This is a further motivation that let the high f_t HBT SiGe bipolar and BiCMOS devices good candidates for phased array system as previously discussed in Section 1.6. The main points to take into consideration in order to design a variable gain amplifier with low phase error are three: chose a topology that ensure that the poles and zeroes close the to operation frequency of the amplifier are independent from the gain variation mechanism; let the devices responsible of the gain variation work at current densities of maximum f_t; understand the phase dependence from the gain looking at the poles and zeroes equations and check if some compensation can be

added in order to reduce this dependence.
In Section 2.3 some VGA topologies are discussed and compared also in terms of possible phase dependence from gain variation.

2.3 VGA Topologies

Different techniques are employed to vary the gain of an amplifier, the main ones are illustrated in Fig. 2.7. Variable feedback approach is depicted in Fig. 2.7 (a), the gain is varied by altering the feedback resistance R_F. Gain can also be controlled varying the degeneration resistance since it is part of a feedback. Variable resistor can be implemented by a FET device in the case of CMOS or BiCMOS technology or by a PIN diode if available [32]. While this approach has potentially high linearity and low DC power consumption, its disadvantages are possible stability issues, bandwidth limitations and gain control range, moreover it has noise figure sensitivity over the gain control range [33]. In terms of input matching, it can be dependent on gain variation. Feedback variable resistance can vary a lot the position of the dominant pole, then it can change the phase of the signal when the resistance is varied.

Second approach, shown in Fig. 2.7 (b), is to incorporate a variable bias network and change the gain by varying the bias current of the drive transistor. This approach has the advantage of a low noise figure, but the disadvantage that the linearity of the amplifier is strongly dependent on the bias current and the gain control range is limited [34]. Since the transconductance of the transistor varies with the gain, S_{11} can change as the gain is modified. The parameters of the input devices are gain-dependent, (C_{pi} for example in bipolar devices) as a consequence also the phase of the signal could be gain-dependent. This configuration is not good if the phase error is critical for the application.

Third approach is to use differential cascode transistors to steer current to the load or to ground as depicted in Fig. 2.7 (c). Gain control is achieved by varying the current through the load resistors which varies the amplitude at the output. This approach has been reported frequently in literature, with implementations in both SiGe-bipolar and GaAs HBT [35], [36], [30]. The advantage of this approach is that it allows a high gain control range with good broadband gain flatness characteristics, the disadvantage is that it tends to suffer more from noise than the other approaches [33]. In this case the current on the transistor Q_1 does not vary with the gain, then the input matching is independent to the gain variation, at least to the first order. Since S_{11} does not vary when the gain is changed, this topology could be a good candidate for low phase error VGA design.

In the fourth approach the gain in controlled by reducing the current in both the cascode transistor Q_2 and the main drive transistor Q_1. It is shown in Fig. 2.7 (d). This method has also been reported in literature, and it is attractive for its simplicity [37]. Input matching is dependent to the gain variation also in this case. Looking at the possible phase dependence from gain, also in this case like for the circuit depicted in Fig. 2.7 (b), the gain variation changes the parameters of the input devices hence the poles and zeroes related to the *gm*-stage are dependent to the gain variation. Table 2.1 resumes the VGA topologies comparison.

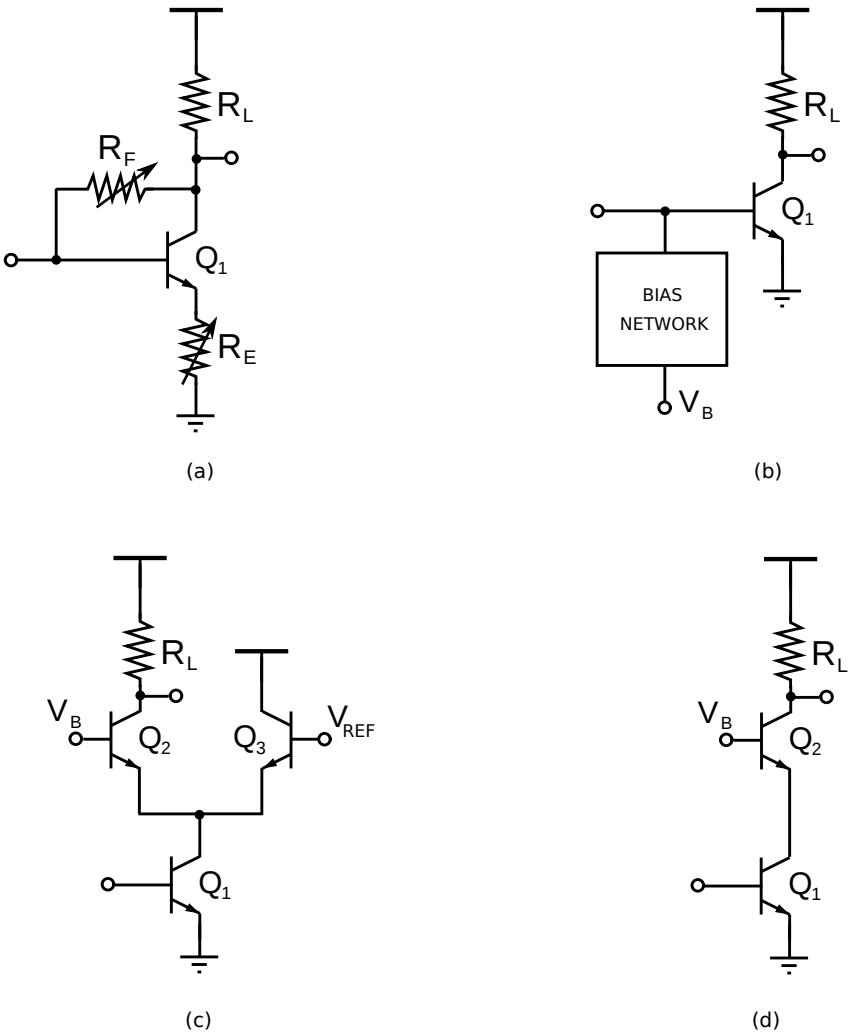

Fig. 2.7 VGA topologies: (a) variable feedback, (b) variable bias, (c) current steering, and (d) simple cascode.

The use of variable attenuators is another way to change the gain before the TTD stage. In this case the noise figure is high and the phase error issues is still present, in fact passive topologies also introduce impedance changes, and hence, phase variations versus attenuation control as briefly discussed in the example in Section 2.2.

2.3.1 Phased array channel performances

Requirements of the VGA must be chosen taking into account the performance of the whole system, in particular one channel of the phased array system. The performances in terms of noise figure, gain and linearity of one channel can be described as a cascade of different

Table 2.1 Comparison VGA topologies.

Topology	Gain Control Range	Input Matching	NF	IIP3	Power Cons.	Phase Error
Variable feed-back	Limited	Gain dependent	Medium	High	Low	Moderate
Variable bias	Limited	Gain dependent	Low	Low	Low	High
Current Steering	High	Gain independent	Medium	Medium	Low	Low
Cascode	Limited	Gain dependent	Medium	Medium	Low	High

blocks. An example of a simple phased array channel is depicted in Fig. 2.8. In this case the phased array works as a receiver, an LNA is used to amplify the weak input signal, then a VGA in series with a passive phase shifter follow the LNA. The whole channel gain is the sum of the three building blocks, whereas the noise figure comes from the Friis formula [38], (Equation 2.7) and the IIP3 come from Equation 2.8:

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 \cdot G_2} + \cdots + \frac{NF_N - 1}{G_1 \cdot G_2 \cdots G_{N-1}} \tag{2.7}$$

$$\frac{1}{IIP3_{tot}^2} = \frac{1}{IIP3_1^2} + \frac{G_1^2}{IIP3_2^2} + \cdots + \frac{G_1^2 \cdots G_{N-1}^2}{IIP3_{N-1}^2} \tag{2.8}$$

where G_i is the gain of the i-th stage, NF_i is the noise figure of the i-th stage and $IIP3_i$ the input referred intercept point of the i-th stage.

According to Friis formula, LNA helps the total noise figure due to his high gain and low noise figure. Common phased array receiver use high performance LNA to optimize the whole NF. The use of III-V semiconductors devices is often preferred even if the cost of the communication system increase. The linearity instead is degraded by the VGA stage because his IIP3 must be scaled by the LNA gain according to the Equation 2.8. However, we have to consider the entire channel gain, then the output referred intercept point, OIP3.

Performances of the channel obviously depends from the application of the phased array. For example if the noise figure is not so critical because the number of antennas is high, it is feasible to skip the LNA and use a VGA stage with good noise figure, saving area, power consumption and then reducing the cost.

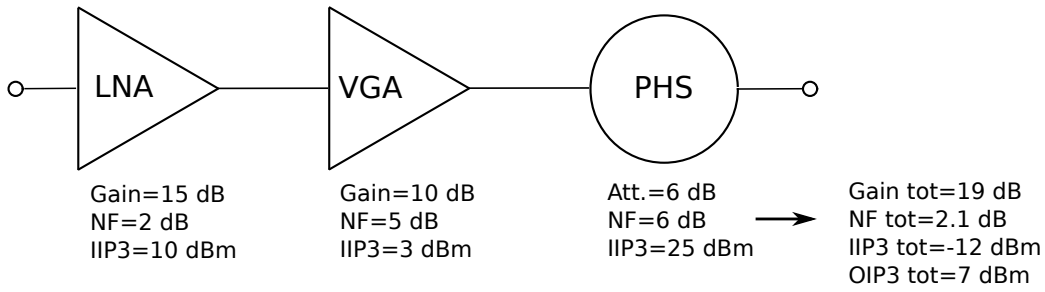

Fig. 2.8 Example of NF and IIP3 cascade stages calculation.

2.4 SiGe VGA with Capacitive Phase Error Compensation

A variable gain amplifier based on the current steering topology is presented in this Section. As described in Section 2.3 the current steering topology is a good candidate for VGA with low phase imbalance versus the gain variation, in fact, since the current on the input devices is constant, S_{11} does not vary if the gain is changed.
A small signal analysis has been done in order to understand the phase behavior of the circuit. Since both, the first stage and the load are independent from the gain (at first order) in this topology, the analysis has been done taking into account the current steering stage and the cascode that bring the current to the load. The schematic used for the ac-analysis is plotted in Fig. 2.9.

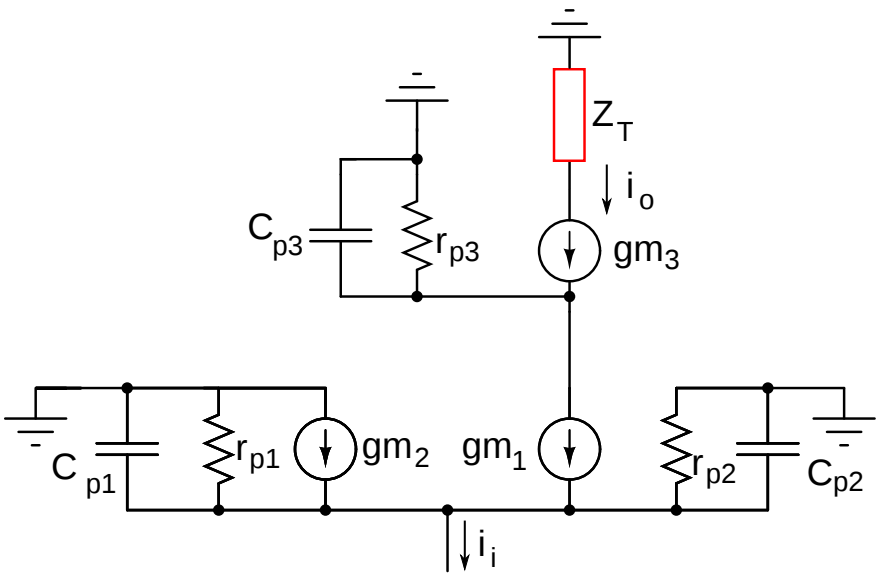

Fig. 2.9 Small signal circuit for ac-analysis.

The analyzed transfer function is the ratio between the current that goes to the load Z_L and the input of the steering stage, Equation 2.9:

$$\frac{i_o(s)}{i_i(s)} \cong \frac{g_{m2}}{g_{m1}+g_{m2}} \cdot \frac{1}{\left(1+s\frac{C_{\pi1}+C_{\pi2}}{g_{m1}+g_{m2}}\right)\left(1+\frac{C_{\pi3}}{g_{m3}}\right)} \tag{2.9}$$

The pole $\omega_{p1} = \frac{g_{m1}+g_{m2}}{C_{\pi1}+C_{\pi2}}$ does not change a lot when the gain is varied because the sum of the currents that pass through the transistor 1 and 2 is constant, hence $g_{m1}+g_{m2}$ is constant and approximately also the input capacitance $(C_{\pi1}+C_{\pi2})$ is quite constant.
Phase error come from the second pole $\omega_{p2} = \frac{g_{m3}}{C_{\pi3}}$, in fact the ratio $\frac{g_{m3}}{C_{\pi3}}$ changes a lot when

the current density become small.
The compensation consists on the introduction of a capacitance C_C in parallel to the device that steers the current through the load, as illustrated in Fig. 2.10. In this case the transfer function is:

$$\frac{i_o(s)}{i_i(s)} \cong \frac{g_{m2}}{g_{m1}+g_{m2}} \cdot \frac{\left(1+\frac{C_C}{g_{m3}}\right)}{\left(1+s\frac{C_{\pi 1}+C_{\pi 2}}{g_{m1}+g_{m2}}\right)\left(1+\frac{C_C}{g_{m3}}\right)} \cong \frac{g_{m2}}{g_{m1}+g_{m2}} \cdot \frac{1}{\left(1+s\frac{C_{\pi 1}+C_{\pi 2}}{g_{m1}+g_{m2}}\right)} \tag{2.10}$$

Capacitance C_C introduce a zero-pole pair with the same frequency hence they are simplified

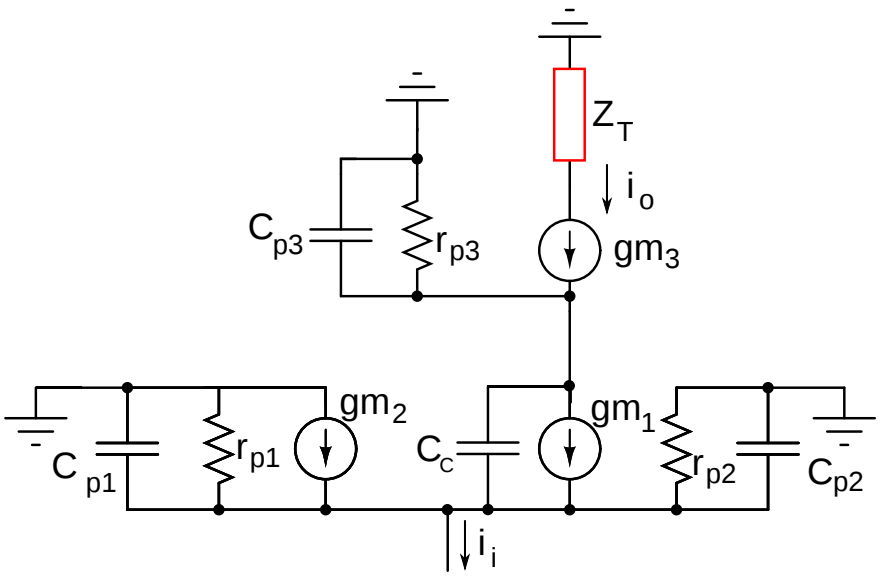

Fig. 2.10 Small signal circuit for ac-analysis.

from the transfer function. Now, the transfer function has only a pole (for this small-signal ac-model) that is locate close to f_T of the transistors (i.e. 200 GHz), hence even a small variation of this pole does not really affect the phase of the signal in the bandwidth of the VGA. This compensation technique has been patented by Infineon Technologies AG.

2.4.1 Design

The schematic of the VGA is illustrated in Fig. 2.11. The input stage is a conventional inductively-degenerated transconductor. Inductor L_b is used to resonate the PADs capacitance and as ESD protection for the input capacitor C_b. A current-steering stage is used for the gain control. A final cascode stage is realized using a quad to add a phase inversion feature:

control voltages V_C and $\overline{V_C}$ are operated such that either transistors $Q_9 - Q_{10}$ or transistors $Q_{11} - Q_{12}$ are on. The signal current is converted into voltage by a tuned load, whose quality factor is decreased by using an explicit load resistor R_L. An output buffer based on emitter followers interfaces the VGA core to the output to realize the output matching. Capacitor C_C is added in parallel to Q_3 and Q_4 to compensate the phase error.

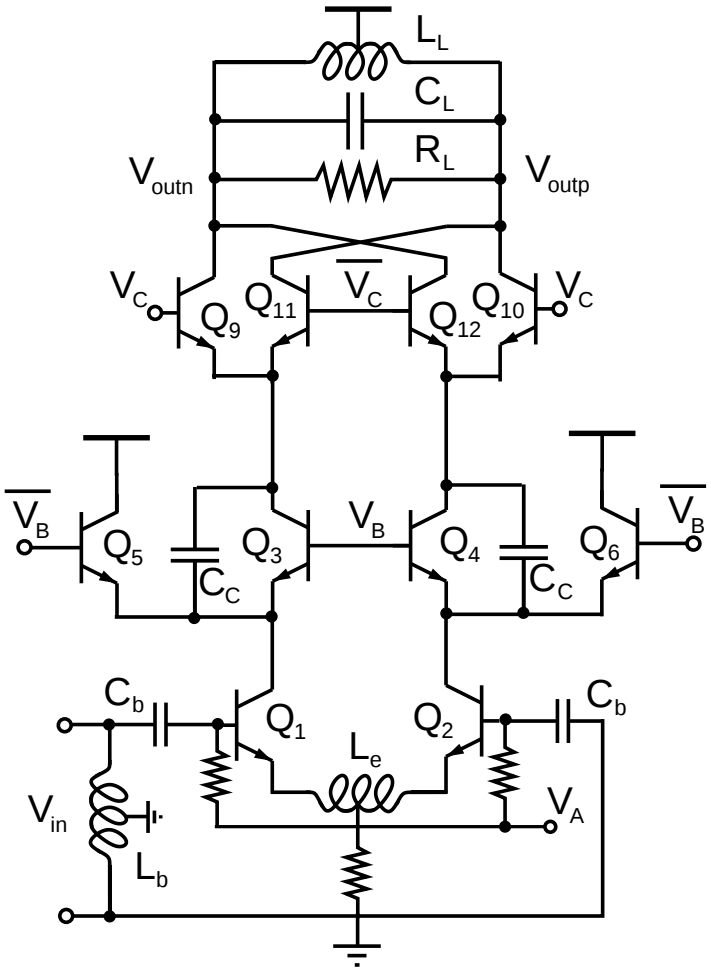

Fig. 2.11 Simplified schematic of the VGA with capacitive compensation.

2.4.2 Measurement Results

A protoype of the variable gain amplifier has been realized. Chip size is $1 \times 0.7\,\text{mm}^2$ including the pads, microphotograph of the chip is depicted in Fig. 2.12 The VGA core, draws 18 mA from the 3.3 V supply, the output buffer 22 mA.

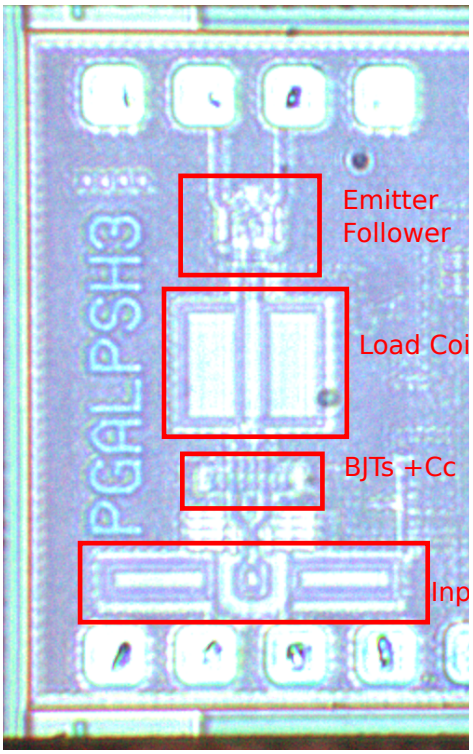

Fig. 2.12 Microphotograph of the VGA with capacitive compensation.

The measurements of the gain variation are reported in Fig. 2.13. The center frequency is $f_c = 10.2\,\text{GHz}$ and the bandwidth is 4.5 GHz. The maximum gain variation is about 60 dB as illustrated in Fig. 2.13 (a). In Fig. 2.13 (b) is plotted the gain variation from $-8\,\text{dB}$ to 16 dB. VGA is well matched for frequencies greater than 9 GHz as reported in Fig. 2.14 (a). The phase behavior is illustrated by Fig. 2.14 (b) for a gain variation of $\Delta G = 24\,\text{dB}$, from $-8\,\text{dB}$ to 16 dB. In this gain range the error is less than 6° at center frequency and goes up to 8° at the border of the band.

This work demonstrates an easy way to correct the major contribute of phase error in a current steering variable gain amplifier. Phase measurements shows still some phase imbalance at the various gain settings. Section 2.5 introduce a more detailed analysis of the current steering VGA and some phase compensation circuits.

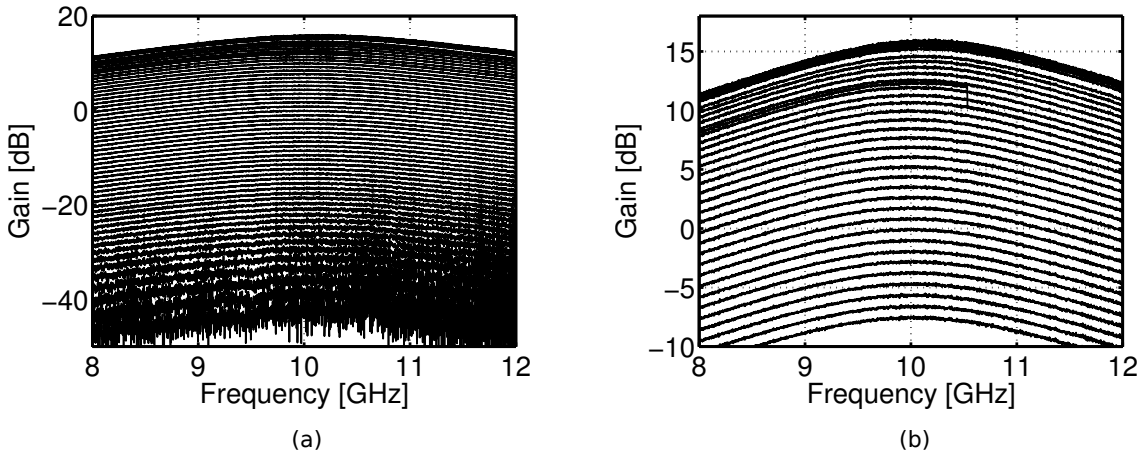

Fig. 2.13 (a) S_{21} for all gain states (b) S_{21} from -8 dB to 16 dB.

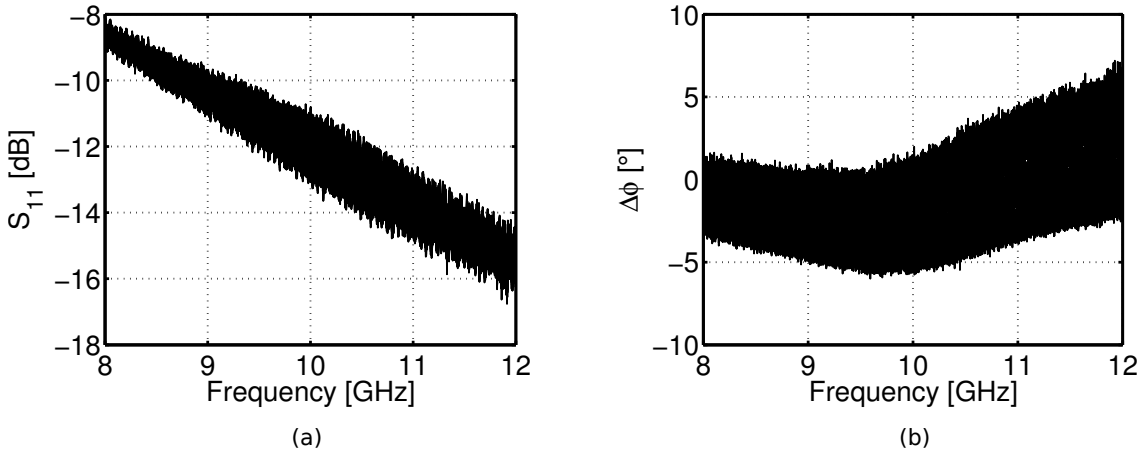

Fig. 2.14 (a) S_{11} for all gain states (b) Phase error relative to the gain variation from -8 dB to 16 dB.

2.5 SiGe VGA with Current Control Phase Error Compensation

VGA presented in Section 2.4 features a simple way to compensate the major contribution of the phase error in a current steering topology. Measurements results shows a phase error greater than 6° for a gain variation slighly higher than 20 dB, thus a more detailed analysis of the phase behavior must be done in order to understand other possible causes of phase error. In this Section a more detailed analysis of the phase error in the current steering topology is presented and two phase error compensation circuits is described .
Section 2.5.1 describes the design of the variable gain amplifier, Section 2.5.2 presents a new model for the phase analysis of the current steering topology. Section 2.5.3 describes the compensation circuitry and the measurements results are presented in Section 2.5.5.

2.5.1 Design

A simplified schematic of the proposed VGA is shown in Fig. 2.15. The input stage is a conventional inductively-degenerated transconductor. A current-steering stage follows, implementing the gain control. A final cascode stage is realized using a quad to add a phase inversion feature: control voltages V_C and $\overline{V_C}$ are operated such that either transistors $Q_9 - Q_{10}$ or transistors $Q_{11} - Q_{12}$ are on. The signal current is converted into voltage by a tuned load, whose quality factor is decreased by using an explicit load resistor R_L. An output buffer based on emitter followers, shown in Fig. 2.16, interfaces the VGA core to the output for testing purposes. Resistors R_{out} are used to achieve output matching. The dc current sources I_{cmp} and I_p in Fig. 2.15 are the phase shift compensation circuits, discussed in detail in Section 2.5.2. Next, the gain control circuitry is discussed.

Gain Control and Translinear Circuits

The current steering quad $Q_3 - Q_6$ in Fig. 2.15 is controlled in current-domain by using diode-connected transistors $Q_7 - Q_8$ as in the classic Gilbert multiplier [39]. The current through Q_3 and Q_4 is thus proportional to I_{exp}, and so is the amount of signal that is transmitted to the output and not steered away by Q_5 and Q_6. Transistors $Q_{13} - Q_{14}$ are a scaled replica of $Q_3 - Q_6$: they are used to implement a base current compensation circuit. The base currents of $Q_{13} - Q_{14}$ are sensed, input to current mirrors, scaled up, and properly injected into V_B and $\overline{V_B}$ nodes to supply the base currents to $Q_3 - Q_6$. This results in an extension of the attainable range of gain variation.

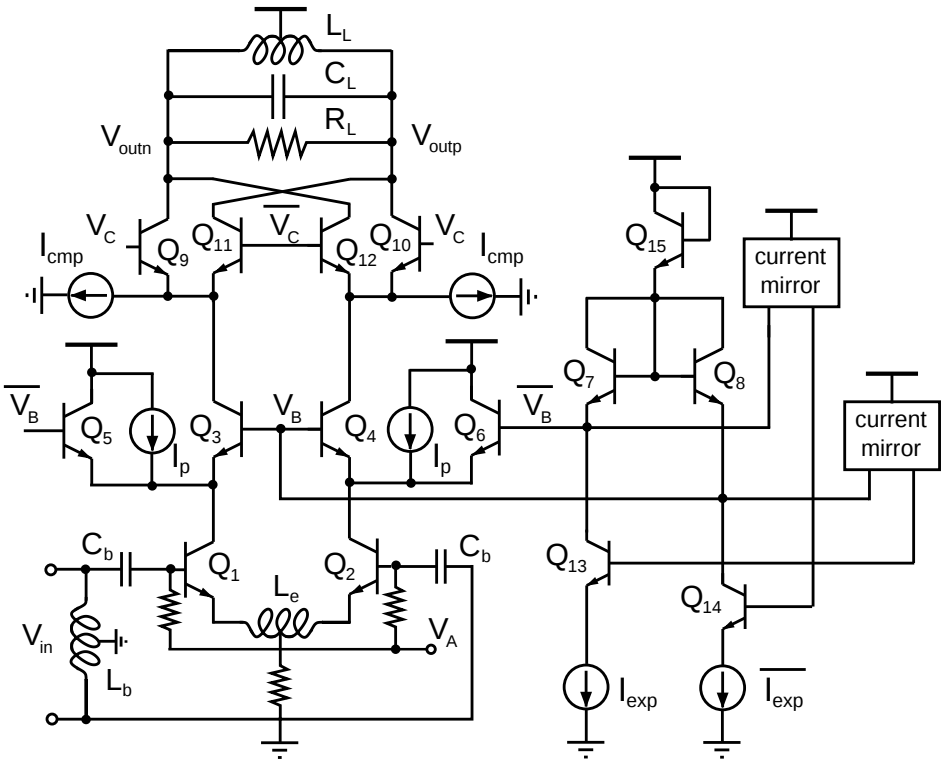

Fig. 2.15 Simplified schematic of the proposed VGA.

The current I_{exp} is obtained by means of a translinear circuit that maps an external control current, I_{ctrl}, into I_{exp} as:

$$I_{\text{exp}} = I_1 \exp(I_{\text{ctrl}}/I_2). \tag{2.11}$$

In this way, linear-in-dB gain control is achieved. Constant currents I_1 and I_2 in (2.11) are proportional to a bandgap reference, as it will be shortly clearer, such that I_{exp} shows a low temperature sensitivity.
The current $\overline{I_{\text{exp}}}$ is a complementary current to I_{exp}:

$$\overline{I_{\text{exp}}} = I_{\max} - I_{\text{exp}} - I'_p \tag{2.12}$$

where $I_{\max}$ is a constant current, proportional to the bias current of Q_1 and Q_2, and I'_p is a scaled version of I_p in Fig. 2.15.

Focusing, without loss of generality, on the mesh made of Q_3, Q_8, Q_7, and Q_5, we can write:

$$V_{\text{BE},3} + V_{\text{BE},8} = V_{\text{BE},7} + V_{\text{BE},5}, \tag{2.13}$$

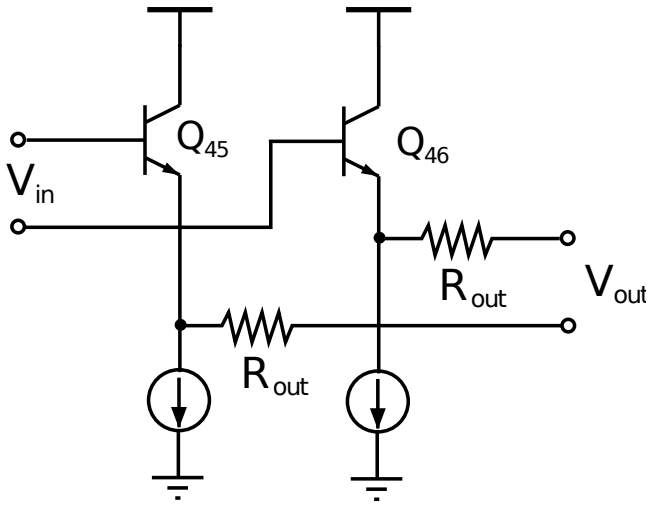

Fig. 2.16 Simplified schematic of the output buffer.

and

$$I_{C5} = I_{C1} - I_{C3} - I_p. \tag{2.14}$$

Recalling that $V_{BE} = V_T \ln I_C/(J_S A_e)$, where $V_T = kT/q$, J_S is the transistor saturation current density, and A_e the emitter area, and observing that Q_3 is matched to Q_5, and Q_7 to Q_8, (2.13) and (2.14) yield

$$\frac{I_{C3}}{I_{C1} - I_{C3} - I_p} = \frac{I_{\exp}}{\overline{I_{\exp}}}. \tag{2.15}$$

Since $I_{\max} \propto I_{C1}$, and $I'_p \propto I_p$, substituting (2.12) in (2.15) gives

$$I_{C3} = A \cdot I_{\exp}, \tag{2.16}$$

where $A = I_{C1}/I_{\max} = I_p/I'_p$ is a constant.

The circuit generating $I_{\exp}$ is illustrated in Fig. 2.17. Its operation is as follows. Applying Kirchhoff voltage law at the mesh made of transistors $Q_{25} - Q_{28}$ we get:

$$V_{\mathrm{BE},25} + I_i R_1 + V_{\mathrm{BE},26} = V_{\mathrm{BE},27} + V_{\mathrm{BE},28}, \tag{2.17}$$

which, observing that $V_{\mathrm{BE},26} = V_{\mathrm{BE},27}$, neglecting base currents, and recalling the exponential relationship between base-emitter voltage and collector current, yields:

$$I_{\exp} = I_1 \frac{A_{e,28}}{A_{e,25}} \exp(I_i R_1/V_T), \tag{2.18}$$

where $A_{e,25}$ and $A_{e,28}$ are the emitter areas of Q_{25} and Q_{28}, respectively. In the presented design, $A_{e,25} = A_{e,28}$. To achieve the desired linear-to-exponential current control conversion, while guaranteeing low temperature sensitivity, the current I_i (cf. Fig. 2.17 and (2.18)) must be proportional to the actual control current, I_{ctrl}, and to absolute temperature. Analysis of the mesh made of transistors $Q_{29} - Q_{32}$ shows the translinear circuit made of devices $Q_{29} - Q_{37}$ achieves this goal:

$$I_i = \frac{A_{e,31}A_{e,32}}{A_{e,29}A_{e,30}} \cdot \frac{I_{\text{ctrl}} \cdot I_{\text{ptat}}}{I_{\text{bg}}}, \tag{2.19}$$

where, in this design, $A_{e,29} = A_{e,30} = A_{e,31} = A_{e,32}$ was set. The circuit generating a bandgap-

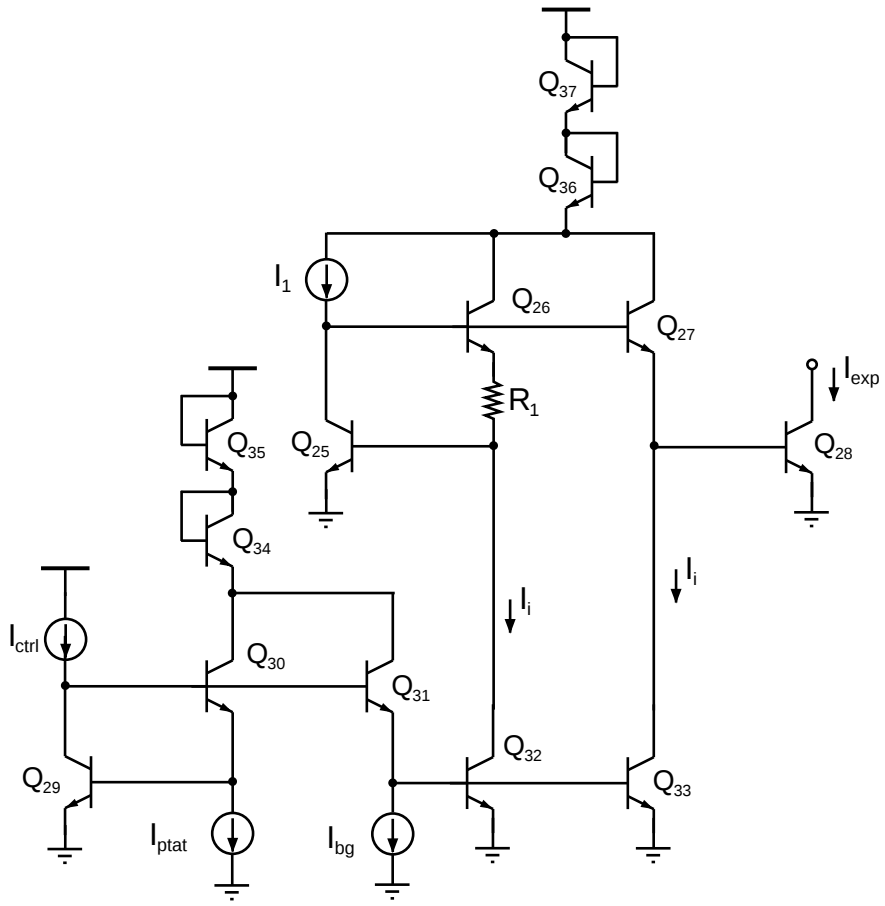

Fig. 2.17 Simplified schematic of the linear-to-exponential conversion circuit.

referenced current, I_{bg}, and a current proportional to absolute temperature, I_{ptat}, is shown in Fig. 2.18. The negative feedback loop set by Q_{41} and Q_{43} equalizes the voltage drops across

resistors R_3. The collector currents of Q_{39} and Q_{40} (and Q_{38}) are forced to be equal, such that

$$I_{\text{ptat}} = \frac{V_T}{R_2} \ln\left(\frac{A_{e,40}}{A_{e,39}}\right) = \frac{V_T}{R_2} \ln(n), \tag{2.20}$$

where $A_{e,39}$ and $A_{e,40}$ are the emitter areas of Q_{39} and Q_{40}, respectively, and, in this design, $n = A_{e,40}/A_{e,39} = 4$. The voltage across R_5 is $V_{BE,39} + I_{\text{ptat}}R_3$, such that the ratio R_3/R_2 can be chosen to obtain a bandgap-referenced current:

$$I_{\text{bg}} = \frac{1}{R_5}\left[V_{BE,39} + \frac{R_3}{R_2} V_T \log\left(\frac{A_{e,40}}{A_{e,39}}\right)\right] = \frac{V_{G0}}{R_5}, \tag{2.21}$$

where V_{G0} is the bandgap voltage.

Combining (2.18)–(2.21), the current I_2 in (2.11) is thus written as

$$I_2 = \frac{V_{G0}}{R_5} \frac{R_2}{R_1} \frac{1}{\ln(n)}, \tag{2.22}$$

emphasizing its low temperature dependence. Finally, the current I_1 in (2.11) is a scaled version of I_{bg}, obtained by means of a current mirror.

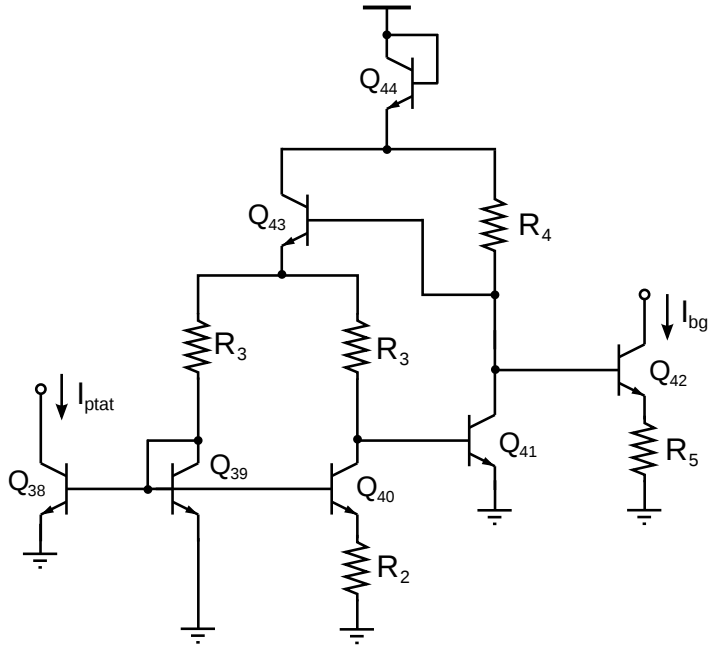

Fig. 2.18 Simplified schematic of the Widlar band-gap and PTAT reference current generation circuit.

2.5.2 Analysis and Compensation of Phase Shift Variation

Generally speaking, the VGA transfer function v_{out}/v_{in} will introduce a phase shift in the signal path. This is not a problem in a phased array, as long as this phase shift is constant, since it results in a phase offset, common to all paths of the array. However, the dependency of the phase shift on the VGA gain is a problem, since different (and undesired) phase shifts may, in this case, be introduced in different array paths.

To analyze the impact of the gain variations on the VGA phase shift, the simplified ac schematic shown in Fig. 2.19 and conventional small-signal analysis are used. At low

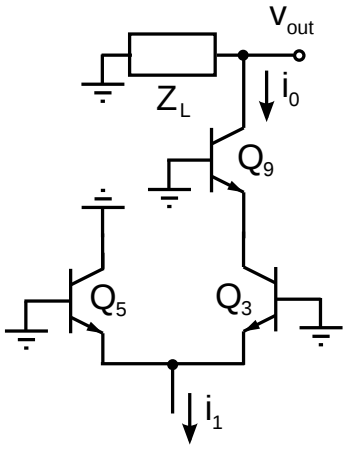

Fig. 2.19 Simplified ac schematic of the proposed VGA used to study the phase shift dependency on the gain setting.

frequency, the current transfer through the steering stage and the final cascode stage, i_0/i_1, is simply:

$$\frac{i_0}{i_1} = \frac{g_{m3}}{g_{m3} + g_{m5}} = \kappa, \tag{2.23}$$

capturing the gain variation feature of the steering stage.

A more careful analysis, however, shows that i_0/i_1 features various high-frequency poles and zeros. The pole and zero that result in the more significant phase shift variation as the gain is changed are reported in the following expression:

$$\frac{i_0}{i_1}(s) \propto \kappa \frac{1 + s/\omega_z}{1 + s/\omega_{p1}} \tag{2.24}$$

where

$$\omega_{p1} = \frac{g_{m9}}{C_{\pi 9} + C'_{\mu 3} + C_{cs3}}, \tag{2.25}$$

$$\omega_z = \frac{1}{(C_{\mu 5} + C_{\pi 5}) r_{b5}}, \tag{2.26}$$

and

$$C'_{\mu 3} = C_{\mu 3}[1 + \kappa(1-\kappa)(g_{m3} + g_{m5}) r_{b3}]. \tag{2.27}$$

$C_{\mu 3}$ and $C_{\mu 5}$ are the base-collector capacitances, $C_{\pi 3}$ and $C_{\pi 5}$ the base-emitter capacitances, and r_{b3} and r_{b5} the base resistances of Q_3 and Q_5, respectively. C_{cs3} is the collector-substrate capacitance of Q_3, $C_{\pi 9}$ the base-emitter capacitance of Q_9.

2.5.3 Phase Shift Compensation Circuits

The proposed compensation techniques aim at desensitizing the zero and pole in (2.24) with respect to variations of the gain, i.e. variations of the bias current through Q_3. As the latter is decreased, so is the collector current through Q_9, and hence g_{m9}. Consequently, the pole in (2.24) shifts to lower frequencies, such that, for any given operation frequency, its (negative) contribution to the amplifier input/output phase shift increases (in magnitude). In order to compensate for this effect, the variation of the dc current in Q_9 is reduced by means of the current source I_{cmp} (see Fig. 2.15). I_{cmp} is a scaled version of $\overline{I_{\text{exp}}}$, i.e. it is proportional to the dc current in Q_5, such that the collector current in Q_9 is approximately kept constant.

The impact of the compensation circuit I_{cmp} is illustrated in Fig. 2.20. Ω_{p1} is the pole angular frequency, ω_{p1}, normalized to its value at maximum gain, i.e., for $\kappa = 1$. Without the compensation circuit, the pole frequency decreases by a decade over the entire gain variation range. Since ω_{p1}, for $\kappa = 1$, can be estimated to be in the neighborhood the cutoff frequency of the technology, in this case $f_T = 200\,\text{GHz}$, the overall phase shift variation introduced at the center of the pass-band of the proposed VGA, i.e., 12 GHz, can be estimated to be around -28°. As clear in Fig. 2.20, the use of I_{cmp} reduces the variation of ω_{p1}, and thus of the related phase shift, to a negligible level.

The final cascode stage, i.e. transistor Q_9 in Fig. 2.19, plays another important role in reducing the phase shift dependency on gain, since it isolates the load tank from the steering stage. If Q_9 was removed, the output capacitance of Q_3, $C'_{\mu 3} + C_{cs3}$, would be in parallel with the tuned load Z_L. Since, from (2.27), $C'_{\mu 3}$ depends on κ, i.e. on the gain, the center frequency of Z_L would change as a function of the gain, resulting in a significant phase shift variation.

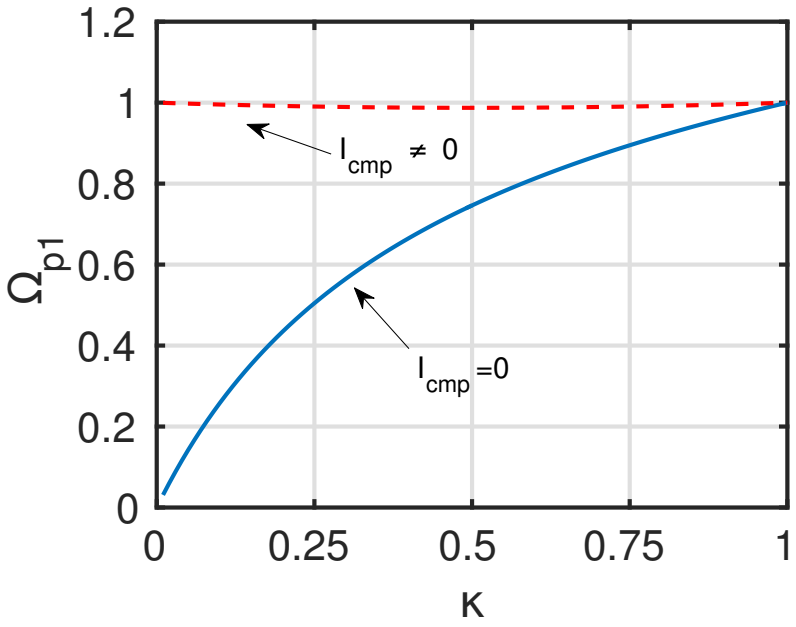

Fig. 2.20 Normalized frequency $\Omega_{p1} = \omega_{p1}/\omega_{p1}(\kappa = 1)$ of the pole in (2.24).

As the gain is decreased, steering the bias current into Q_5, the capacitance $C_{\pi 5}$ increases, shifting ω_z to lower frequencies, as clear from (2.26). This mechanism increases the VGA input/output phase shift as the gain becomes smaller. To counteract this behavior, the current source I_p in Fig. 2.15 is employed. Its goal is to decrease the maximum collector current flowing through Q_5, limiting the maximum value that $C_{\pi 5}$ attains. A simplified schematic of the circuit used to generate I_p is shown in Fig. 2.21. Transistors $Q_{16} - Q_{22}$ are a replica of the gain control scheme used in the VGA core reported in Fig. 2.15. Consequently, I_p is proportional to $\overline{I'_{\text{exp}}}$:

$$I_p \propto \overline{I'_{\text{exp}}} = I_{\text{max}} - I_{\text{exp}} \tag{2.28}$$

By comparing (2.12) and (2.28), and recalling that I'_p in (2.12) is proportional to I_p, one notices that the use of the compensation circuit does not change the functional dependency of the current through Q_5 on I_{ctrl}, i.e. on the gain setting. However, it introduces a down-scaling factor such that the maximum value of $C_{\pi 5}$ is reduced, and so is the variation of the zero in (2.24) with the gain. Moreover, the introduction of I_p does not change the dc current through Q_3. In other words, the collector current of Q_3 is still given by (2.16), while the collector current of Q_5 is

$$I_{C5} = B \cdot (I_{\text{max}} - I_{\text{exp}}), \tag{2.29}$$

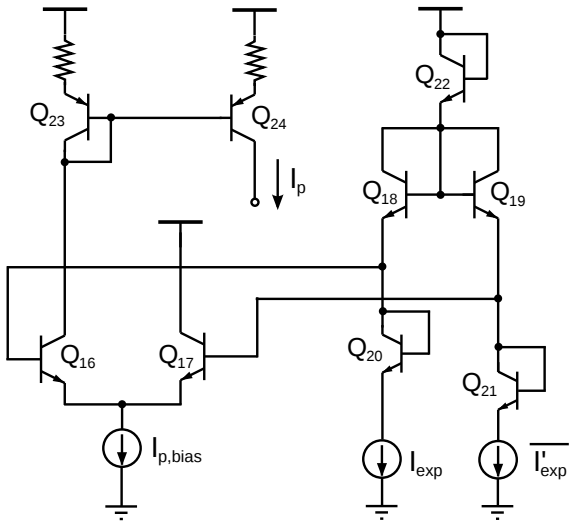

Fig. 2.21 Simplified schematic of the circuit used to generate I_p in Fig. 2.15.

the value of B being set by $I_{p,\max}$, that is the maximum value of I_p:

$$B = A\left(1 - N\frac{I_{p,\max}}{I_{\max}}\right). \tag{2.30}$$

N is a constant set by some current mirror ratios. To this regard, the circuit in Fig. 2.21 gives quite some flexibility. $I_{p,\max}$ can be in fact set by changing the bias current $I_{p,\text{bias}}$ (see Fig. 2.21).

Figure 2.22 shows Ω_z, i.e., the frequency of the zero in (2.24) normalized to its value for $\kappa = 1$, versus κ, that is, as the gain is changed. Without the use of a compensation circuit, the zero frequency experiences a decrease by a factor 3 over the gain variation range. This results in an estimated overall phase shift variation of about 8° due to the zero. The use of I_p, instead, limits the minimum value of ω_z to about 65% of its maximum value. The choice of the most appropriate value for the design parameter $I_{p,\max}$ is discussed next.

2.5.4 Further Insights on the Phase Shift Compensation Circuits

The introduction of the current source I_p to desensitize the zero in (2.24) with respect to the gain variations has some side effects. To appreciate this, (2.24) must be recast as

$$\frac{i_0}{i_1}(s) \propto \kappa\frac{1+s/\omega_z}{1+s/\omega_{p1}} \cdot \frac{1}{1+s/\omega_{p2}}, \tag{2.31}$$

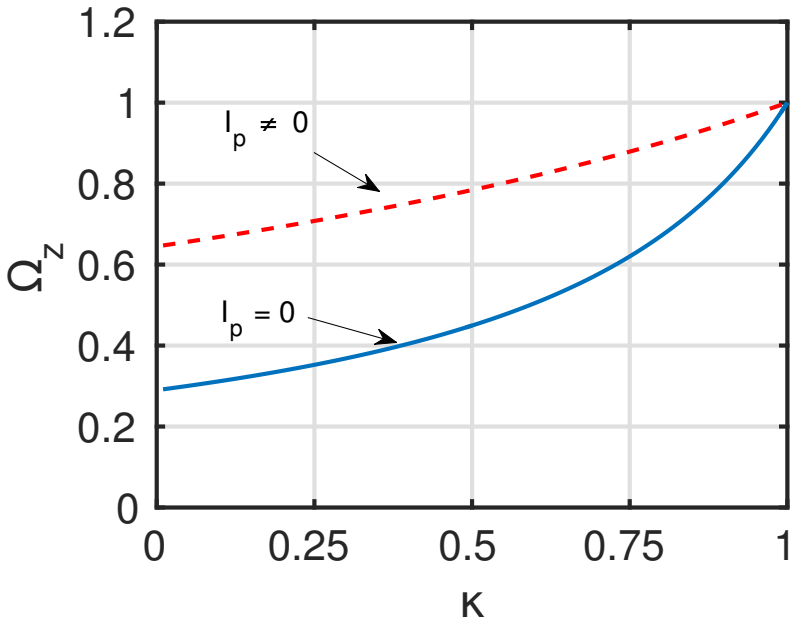

Fig. 2.22 Normalized frequency $\Omega_z = \omega_z/\omega_z(\kappa = 1)$ of the zero in (2.24).

where a previously neglected pole, ω_{p2}, has been now emphasized:

$$\omega_{p2} = \frac{g_{m3} + g_{m5}}{C_{\pi 3} + C_{\pi 5} + C_{cs1} + C_{\text{out},I_p}}. \tag{2.32}$$

C_{cs1} is the collector-substrate capacitance of Q_1, and C_{out,I_p} is the output capacitance of the current source I_p. If $I_{p,\max} = 0$, ω_{p2} is not dependent on the gain variations, and can be indeed neglected in the analysis of the phase shift variation. However, if $I_{p,\max} \neq 0$, ω_{p2} shifts to lower frequencies as the gain is reduced, since now $I_{C3} + I_{C5}$ is not constant as the gain (and thus I_p) is changed (cf. (2.14)). Hence, a negative phase shift is introduced. This effect partly compensates the positive phase shift due to ω_z at low gains, such that the overall phase shift variation is not minimized by zeroing I_{C5} in correspondence of the smallest gain setting, but rather setting $I_{p,\max} < I_{\max}/N$ (cf. (2.30)).

The variation of ω_{p2} as the gain is changed is shown in Fig. 2.23. Ω_{p2} is ω_{p2} normalized to its value for $\kappa = 1$. As already discussed, if $I_{p,\max} = 0$, ω_{p2} does not depend on κ. On the contrary, the more $I_{p,\max}$ increases, the larger the variation of ω_{p2} with κ is, and the subsequent phase shift variation introduced in the VGA.

The use of the current source I_p has also an impact on the low frequency current transfer

through the steering stage. The term κ in (2.31), in fact, is written as:

$$\kappa = \frac{\kappa'}{1 - N\frac{I_{p,\max}}{I_{\max}}(1-\kappa')}, \tag{2.33}$$

where $\kappa' = I_{\exp}/I_{\max}$. The maximum attainable gain is unchanged, as at high gains $\kappa \approx \kappa'$. However, at lower gains the presence of the denominator term in (2.33), i.e., of I_p, limits the minimum gain that is obtained. For a given lower value of I_{ctrl}, $I_{\text{ctrl,min}}$, corresponding to a minimum value of κ', $\kappa'_{\min}$, the gain is boosted by a factor approximately equal to $1/(1 - NI_{p,\max}/I_{\max}) \geq 1$. The choice of $I_{p,\max}$ is hence dictated by a tradeoff between the compensation of the effects of ω_z and ω_{p2} on the VGA phase shift variation, and the reduction of the achievable gain variation range. As it will be shown in Section 2.5.5, in practice, the decrease in the gain range is limited to a few dB, while the reduction in the phase shift variation obtained by employing the compensation circuit I_p is substantial.

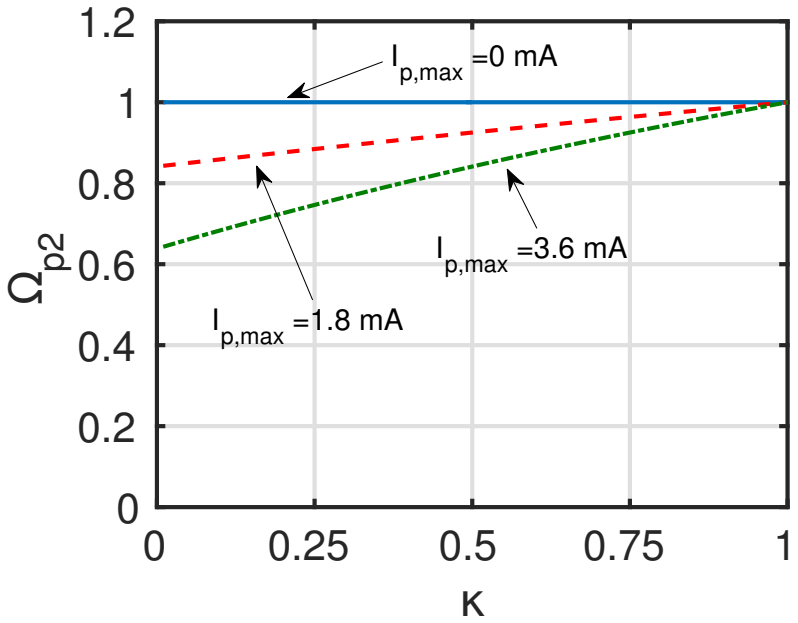

Fig. 2.23 Normalized frequency $\Omega_{p2} = \omega_{p2}/\omega_{p2}(\kappa = 1)$ of the pole in (2.31).

2.5.5 Measurement Results

The proposed VGA was implemented in Infineon SiGe bipolar technology. A microphotograph of the chip is shown in Fig. 2.24. The die area is $1 \times 0.7\,\text{mm}^2$ including the pads. The chips have been assembled in chip-on-board fashion for testing. All the dc pads have

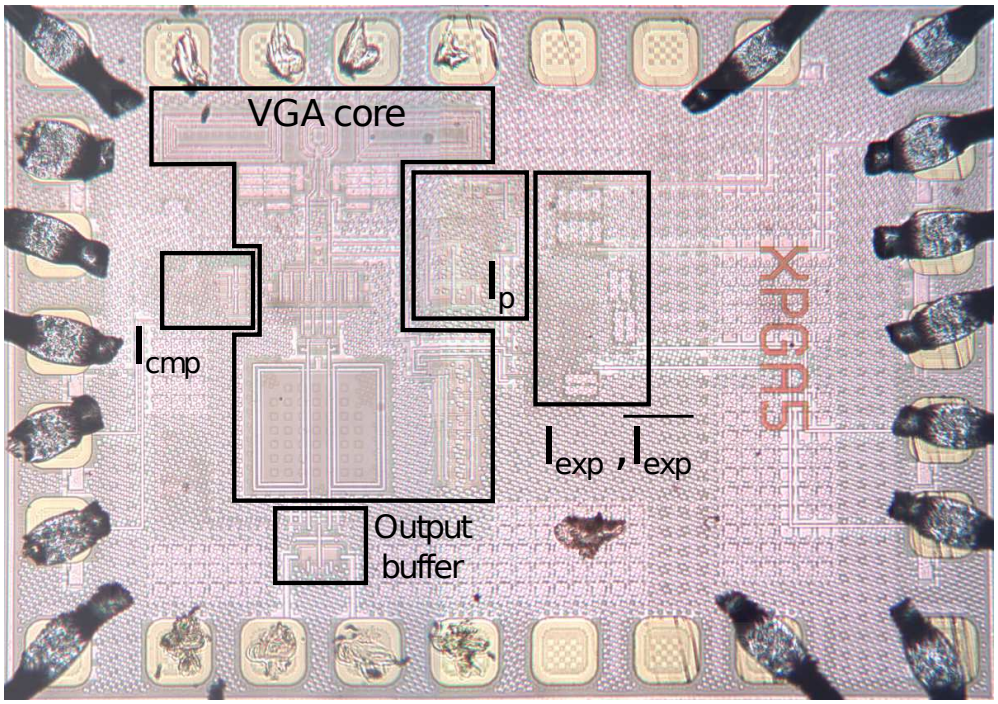

Fig. 2.24 Microphotograph of the VGA chip. Die area is 0.7 mm^2.

been wire-bonded, while the input/output RF interfaces have been assessed by using GSSG differential probes. All the following experimental results refer to the VGA core plus output buffer cascade. The VGA core, including all bias circuits, draws 17.6 mA from the 3.3 V supply, the compensation circuitry up to 7.7 mA, the output buffer 22 mA.

The measured input reflection coefficient is illustrated in Fig. 2.25, as the gain is changed. The amplifier is well matched ($S_{11} < -11$ dB) over the entire 10 to 14.4 GHz band. The input match is not affected by the gain control. The measured frequency response of the VGA is shown in Fig. 2.26 for a variety of gain settings. The center frequency is about 12 GHz, the 3-dB bandwidth spans from 10 to 14.4 GHz, and the maximum gain is 13 dB. The control current, I_{ctrl}, is uniformly changed in 3 μA steps. The corresponding gain variation is constant in dB, when the gain is changed from its maximum value down to about -7 dB (cf. Fig. 2.26), validating the designed linear-in-dB control. For lower gain values, the gain control tends to flatten out. The overall gain variation is $\Delta G = 22$ dB. The effectiveness of the phase shift compensation circuitry is illustrated in Fig. 2.27, where the measured phase shift variation, $\Delta\phi$, is shown as a function of gain. The measurement is performed at 12 GHz. When the compensation circuits are off (dashed line) $|\Delta\phi|$ is as large as 23° over the entire gain variation range. Notice that $\Delta\phi$ is negative and increases in magnitude as the gain is decreased, in agreement with the analysis in Section 2.5.3. When I_{cmp} is turned on, but $I_{p,\max} = 0$ mA, the overall phase shift variation is reduced to 8°. The residual $\Delta\phi$ is positive;

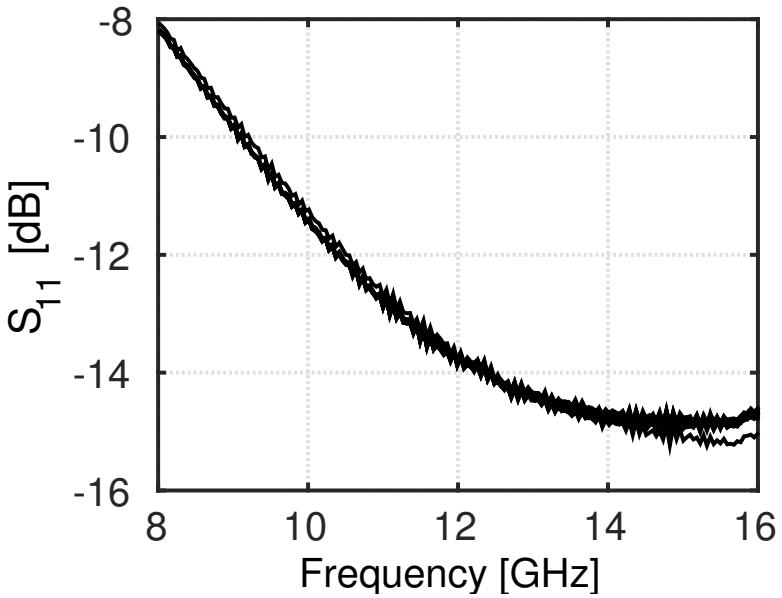

Fig. 2.25 Measured input match for various gain settings.

it increases with a decrease in the gain. This means that the compensation circuit I_{cmp} has effectively neutralized the variation of the pole in (2.24). The remaining phase shift variation is thus due to the change of the zero in (2.24). The results are again in agreement with the discussion in Section 2.5.3.

As $I_{p,\max}$ is increased, $\Delta\phi$ decreases. For $I_{p,\max} = 1.8\,\text{mA}$ the overall $\Delta\phi$ is reduced to 1.5°. When $I_{p,\max} > 1.8\,\text{mA}$, we notice $\Delta\phi$ becomes negative and increasingly larger in magnitude as the gain decreases and/or $I_{p,\max}$ increases. The reason for this is the dependence of the additional pole (ω_{p2} in (2.31)) on the gain variation when I_p is employed, as analyzed in Section 2.5.4. For small values of $I_{p,\max}$ this effect is negligible. However, if $I_{p,\max}$ becomes too large, the phase shift variation introduced by the additional pole is not negligible any more. Overall, the results in Fig. 2.27 show that the compensation approach is effective and robust to variations of $I_{p,\max}$, as $\pm 50\%$ changes in $I_{p,\max}$ with respect to the optimal 1.8 mA value still guarantee $|\Delta\phi| < 4°$.

In Fig. 2.27, one can also note the reduction in the gain variation range discussed in Section 2.5.4, and formulated in (2.33). As $I_{p,\max}$ is increased, the gain variation range decreases. However, such a decrease is quite limited. At the optimal value of $I_{p,\max} = 1.8\,\text{mA}$, the penalty in the gain variation range is just 1 dB.

The robustness of the design and of the proposed compensation techniques across temperature is reported in Fig. 2.28. The measured phase shift variation, $\Delta\phi$, is shown as a function of gain. The measurement is repeated at three different temperatures, namely 27°C, 55°C,

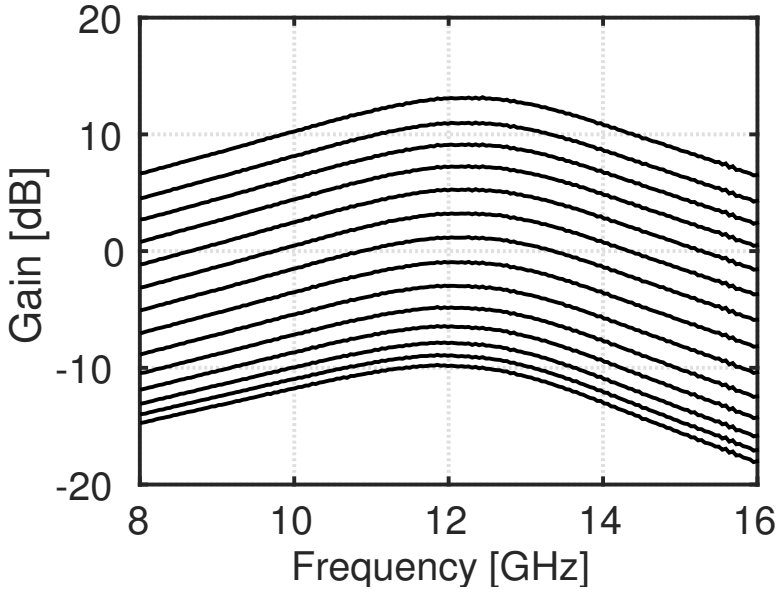

Fig. 2.26 Measured gain for various gain settings (I_{ctrl} changed in 3 μA steps).

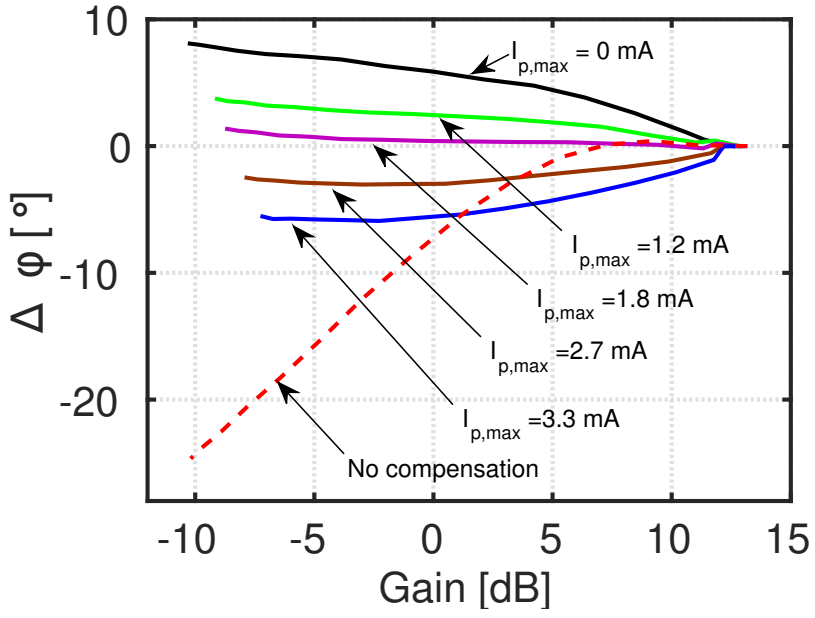

Fig. 2.27 Measured phase shift variation, $\Delta\phi$, as a function of gain with compensation circuits off (dashed line) and on (solid lines) for various settings of $I_{p,\text{max}}$. The measurement is performed at 12 GHz.

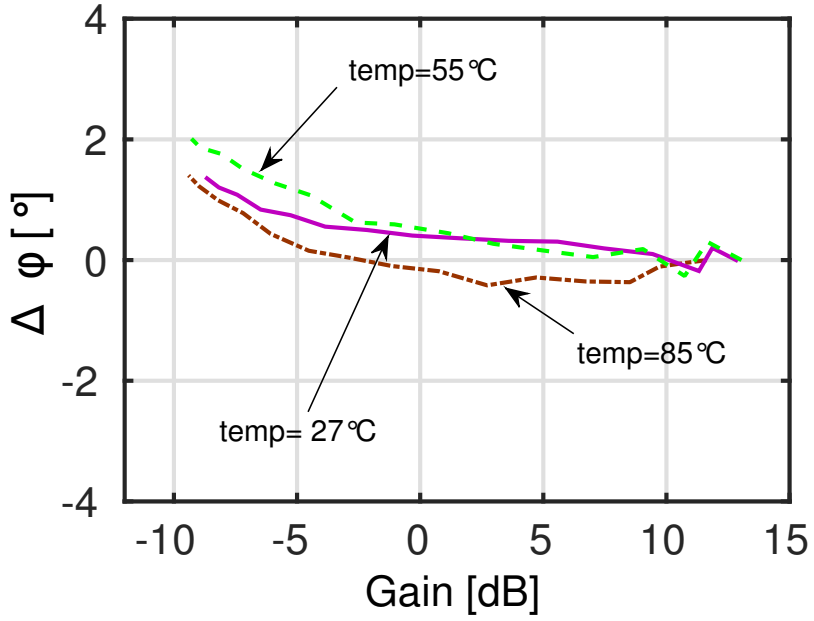

Fig. 2.28 Measured phase shift variation, $\Delta\phi$, as a function of gain for $I_{p,\max} = 1.8$ mA at different temperatures: 27°C (solid line), 55°C (dashed line), and 85°C (dash-dot line). The measurement is performed at 12 GHz.

and 85°C. The proposed compensation circuitry is on, and $I_{p,\max}$ is set to 1.8 mA. As clear from Fig. 2.28, little performance variation is observed as the temperature is changed. In any case, $|\Delta\phi| \leq 2°$.

To show the robustness of the proposed compensation technique across frequency, the measured $\Delta\phi$ in the 8 to 16 GHz span is reported in Fig. 2.29 for various gain settings. $I_{p,\max}$ is set to 1.8 mA. Within the amplifier 3-dB band, $|\Delta\phi|$ is limited to $\leq 2°$.

The measured group delay variation, $\Delta\tau_g$, is shown in Figs. 2.30–2.32 for a variety of gain settings and across temperature, i.e. at 27°C, 55°C, and 85°C. $I_{p,\max}$ is set to 1.8 mA. At ambient temperature (cf. Fig. 2.30), $\Delta\tau_g$ is limited to ± 0.2 ps in the 10 to 14.4 GHz band, which is an excellent result. At higher temperatures, a slight degradation in the group delay variation is observed for frequencies above 13 GHz (cf. Figs. 2.31 and 2.32). In any case, $|\Delta\tau_g| < 0.3$ ps over the entire measured 8–16 GHz frequency range and across the measured temperature range.

The measured noise figure is reported in Fig. 2.33 with compensation circuits off (dashed line) and on (solid lines). $I_{p,\max}$ is set to 1.8 mA. The compensation circuits have an almost negligible impact on the noise performance of the VGA. With the compensation on, the minimum noise figure is 5.1 dB; it is < 7 dB within the amplifier pass-band. When used in a receiver chain, the VGA is supposed to follow a fixed-gain low noise amplifier. As such, its

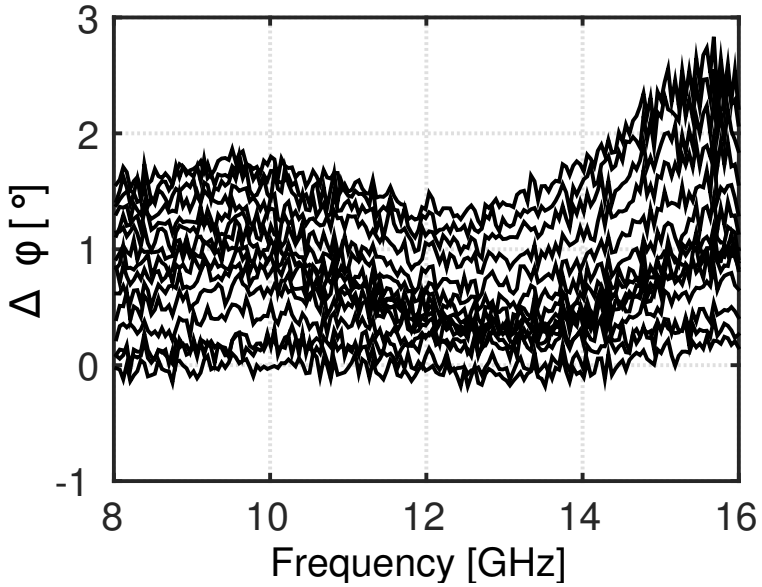

Fig. 2.29 Measured phase shift variation, $\Delta\phi$, for various gain settings and $I_{p,\max} = 1.8\,\text{mA}$.

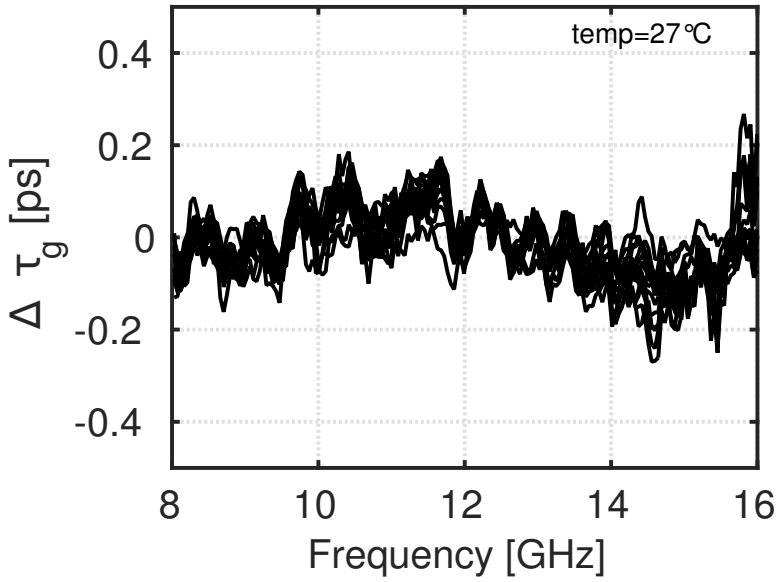

Fig. 2.30 Measured group delay variation, $\Delta\tau_g$, for various gain settings and $I_{p,\max} = 1.8\,\text{mA}$. The measurement is performed at a temperature of 27°.

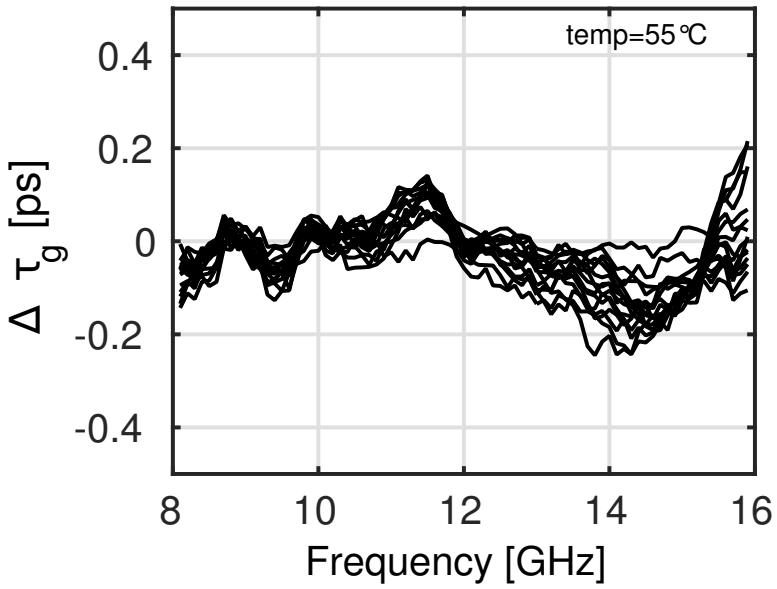

Fig. 2.31 Measured group delay variation, $\Delta\tau_g$, for various gain settings and $I_{p,\max} = 1.8\,\text{mA}$. The measurement is performed at a temperature of 55°.

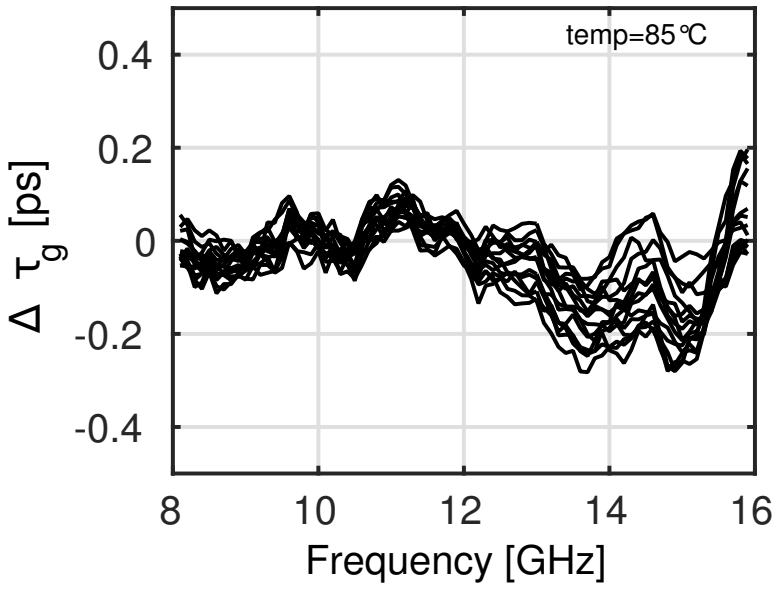

Fig. 2.32 Measured group delay variation, $\Delta\tau_g$, for various gain settings and $I_{p,\max} = 1.8\,\text{mA}$. The measurement is performed at a temperature of 85°.

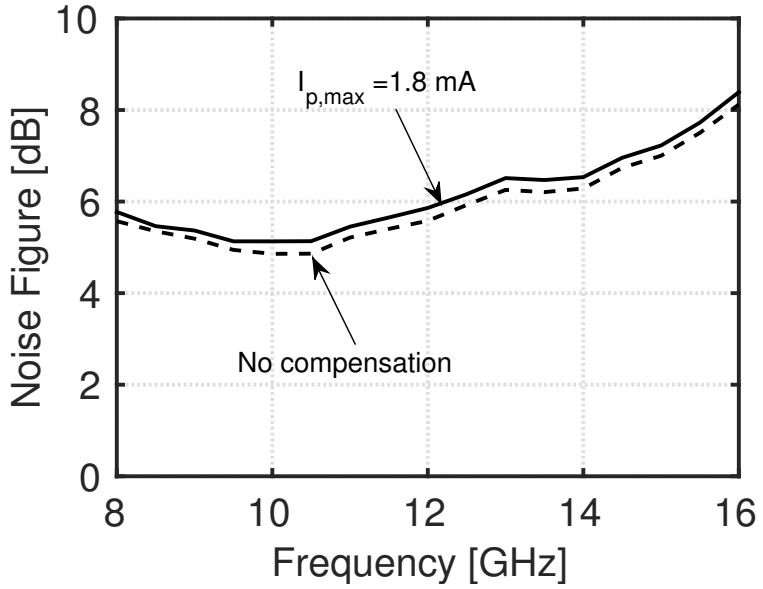

Fig. 2.33 Measured noise figure with compensation circuits off (dashed line) and on (solid lines) with $I_{p,\max} = 1.8\,\mathrm{mA}$.

noise performance seems to be adequate not to impair the overall receiver noise figure. The measurement of the input-referred third-order intercept point (IIP3) is shown in Fig. 2.34. The measurement is performed at 12 GHz. The measured IIP3 is -3 dBm. The performance of the proposed VGA is summarized in Table 3.2, and compared with the state-of-the-art: the reported VGA shows the larger gain variation, and the smaller phase shift variation.

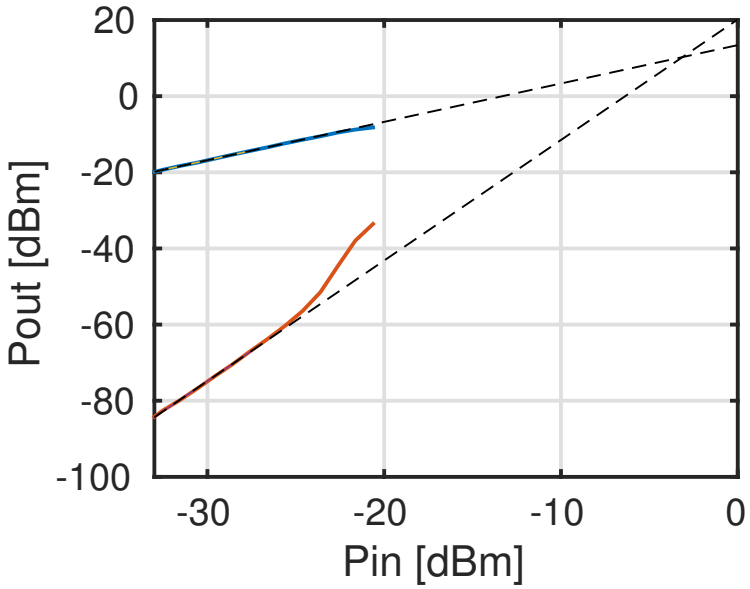

Fig. 2.34 Measured input-referred third-order intercept point. The measurement is performed at 12 GHz.

Table 2.2 Comparison with the state-of-the-art.

	This work	[40]	[41]	[42]	[43]	[31]
Tech.	SiGe HBT	SiGe HBT	SiGe BiC-MOS	SiGe BiC-MOS	SiGe HBT	SiGe BiC-MOS
Freq. [GHz]	10-14.4	32-34	13-15	35	7-11	5.2-5.9
Gain [dB]	13	20	2.5‡	-2	12.5	7
ΔG [dB]	22	11	17.6	7.5	16	20
$\Delta\phi$ [°]	2	4	5	20	25	6
NF [dB]	5.1	3.4	10†	9†	–	3.2
IIP3 [dBm]	-3	-19	-6†	-6†	8.5	-10
P_{dc} [mW]	83	33	119‡	35†	400	1.6

†Entire RX chain. ‡Stages with variable gain feature.

2.6 BiCMOS Wide Band VGA with Current Control Relative Group Delay Error Compensation

Both commercial and military wireless-communication applications require systems that can operate over multi-frequency bands. Wideband phased-array antenna transceiver system has been looked at as a potential solution [31].
Building a phased-array antenna system that operates in multi-frequency bands demands a wideband transmit/receive module, wideband antenna element, wideband phase shifter and control circuit. Such blocks trade flexibility with selectivity; the latter would thus be guaranteed by other building blocks in the transceiver chain.
This Section presents a wideband variable gain amplifier whose pass-band spans the 15.5-39 GHz band. Such a VGA can be employed in transceivers operating at most of the $5G$ carrier frequencies proposed so far in the K_u to K_a bands [10].
The proposed VGA makes use of ladder reactive networks to ensure wideband input matching and have the capability of directly driving a $50\,\Omega$ load without requiring an additional buffer. The input and output broadband networks embed magnetic transformers, such that single-ended to differential conversion is also performed. The VGA thus offers the possibility of being driven from a single-ended source (e.g. an external LNA), or drive a $50\,\omega$ load (single-ended or differential), such as, e.g., a transmission line-based phase shifter or a PA.
Compensation circuits are used to greatly reduce the phase shift variations as the gain is changed. The techniques introduced in Section 2.5 for a narrow-band VGA are shown to be effective over a broad bandwidth as well [44]. Prototypes of the proposed VGA have been implemented in a BiCMOS technology.
Section 2.6.1 presents the design of the Wideband VGA focusing on the input and output wideband networks. Measurement results are then described in Section 2.6.2.

2.6.1 Design

A simplified schematic of the proposed wideband VGA is shown in Fig. 2.35. The amplifier makes use of a reactive network to expand the operation frequency range of an inductively degenerated input stage, as in [45]. At the output, a multi-section reactive network is also employed, similarly to [46]. The gain control is based on a current steering quad, which is isolated from the load by a cascode stage ($Q_9 - Q_{10}$). The gain control voltages, V_B and $\bar{V_B}$ in Fig. 2.35, are generated by a translinear circuit as in the one described in Section 2.5. Between the current steering stage and the cascode stage, a differential peaking inductor is used to compensate for the intrinsic frequency roll-off of the current gain of the input stage

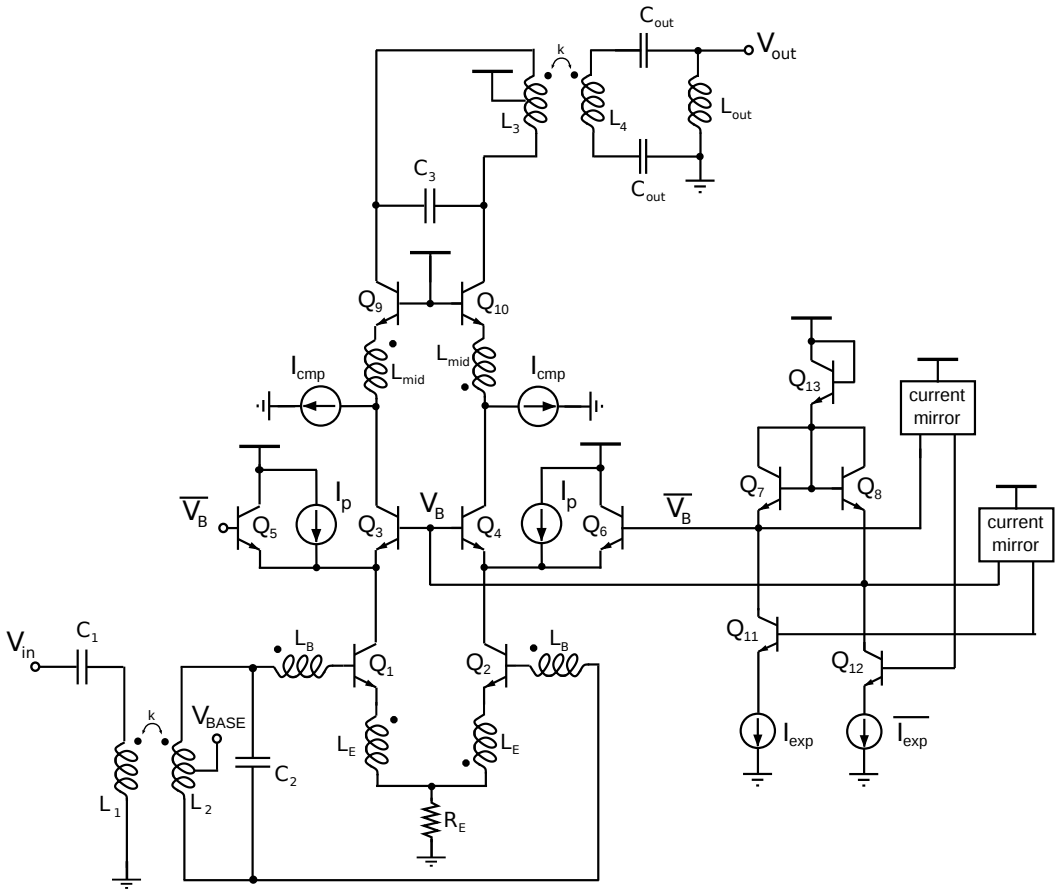

Fig. 2.35 Simplified schematic of the wideband VGA.

$(Q_1 - Q_2)$.

Two compensation circuits, namely dc current sources I_{cmp} and I_p in Fig. 2.35, are employed to effectively decrease the phase shift variation as a function of the gain. As discussed in Section 2.5, these circuits desensitize the frequencies of some poles and a zero in the transfer function of the signal current through the steering and cascode stages from the variation of the gain. In particular, the role of I_{cmp} is to keep the transition frequency, f_T , of $Q_9 - Q_{10}$ constant. I_p aims instead at limiting the value of the base-emitter capacitances of $Q_5 - Q_6$ when the VGA gain is decreased and the collector current in $Q_5 - Q_6$ is thus increased. As a result, the variation of the input-output phase shift as a function of the gain is remarkably reduced.

The employed techniques rely on dc current sources that do not adversely affect the signal path, while the values of I_{cmp} and I_p are automatically set by the same mechanism that

Table 2.3 Input Network Parameters from Tchebyscheff filters with 0.2 dB ripple and R=50 Ω.

L_A	391 pH
L_B	288 pH
L_C	391 pH
C_A	108 fF
C_B	147 fF
C_C	108 fF

controls the gain [44]. The simplicity of the adopted compensation scheme, together with the use of the reactive broadband networks, proves to be effective in a very wideband fashion.

The input reactive network is based on a doubly-terminated three section band-pass Chebyshev ladder filter prototype. Similarly as in [45], where a two section filter is however

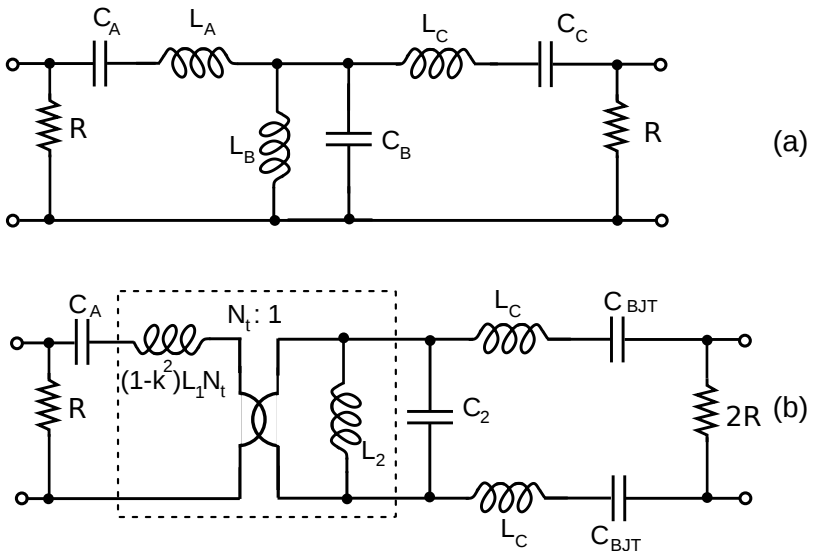

Fig. 2.36 Input network transformation: (a) Before transformation; (b) After transformation through input transformer.

featured, a magnetic transformer is embedded in the network to additionally perform single-ended to differential signal conversion. The prototype of the filter is depicted in Fig. 2.36, the values of the filter components are described in Table 2.3. It is a Tchebyscheff filters with 0.2 dB ripple and R=50 Ω. Transformer $L_1 - L_2$ performs an impedance transformation by 2 then $N_t = \frac{1}{\sqrt{2}}$. The values of the transformer components are the extracted by Equations 2.34 and 2.35 :

$$\begin{cases} N_t = k \cdot \sqrt{\frac{L_1}{L_2}} = \frac{1}{\sqrt{2}} \\ L_2 = 2 \cdot L_B \\ L_A = \left(1 - k^2\right) \cdot L_1 \end{cases} \tag{2.34}$$

$$\begin{cases} k = 0.65 \\ L_1 = 681\,pH \\ L_2 = 576\,pH \end{cases} \tag{2.35}$$

The leakage flux inductance of the coupled inductors L_1 and L_2 is employed together with capacitor C_A to make up the input (series) section. The layout of the transformer $L_1 - L_2$ is optimized to achieve both limited capacitive parasitics and a relatively large magnetic coupling factor. Transformer layout is depicted in Fig. 2.37. Both L_1 and L_2 are two-turn coils laid out in an interleaved fashion. The external and innermost turn use the top metal layer, while the other turns are in the second-top metal layer. Turns in different metal layers can be placed closer, which increases the magnetic coupling, without the penalty of a too large parasitic capacitance between the inductors. Capacitor C_1 is slighly greather than C_A to taking into account the parasitic capacitance of the input PAD. The emitter degeneration

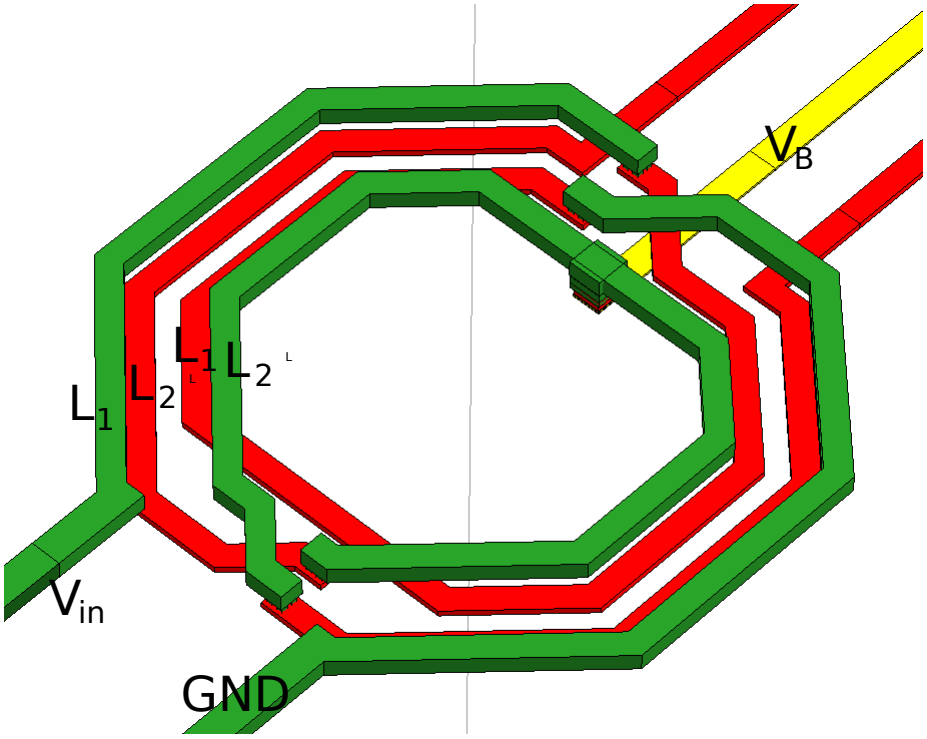

Fig. 2.37 Layout of input transformer.

inductors, L_E , and the base inductors, L_B , are implemented as symmetric coils. Moreover, they are concentrically laid-out and thus magnetically coupled. This arrangement allows to increase the inductance for a given silicon area [46] and also greatly simplifies the layout of the interconnects. The combination of the inductor $L_E - L_B$ give the ladder series element L_C in Fig. 2.36. The layout of $L_E - L_B$ is depicted in Fig. 2.38.

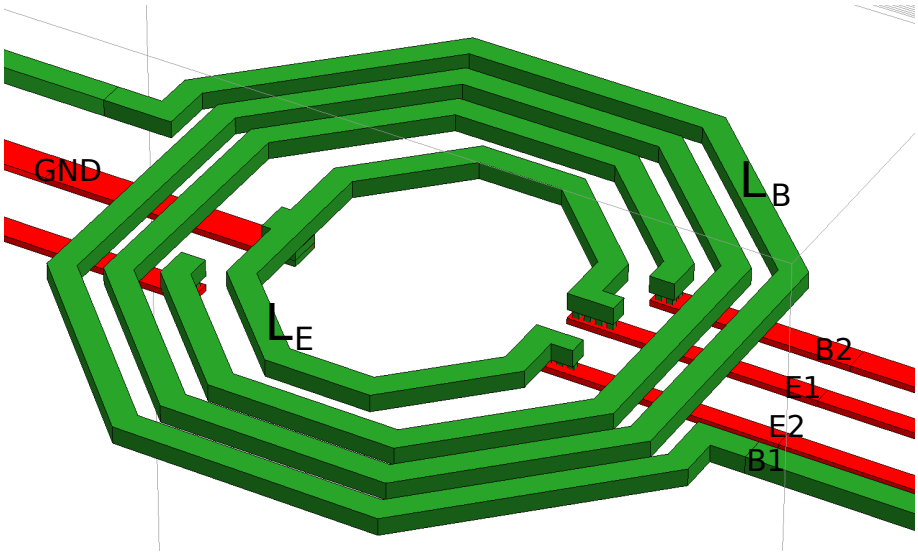

Fig. 2.38 Layout of transformer $L_B - L_E$.

The interstage peaking inductors Lmid (cf. Fig. 2.35) are also implemented as a symmetric differential inductor, leveraging the layout discussed in [45]. The output reactive network is used to extend the pass-band of the amplifier. As opposed to [46], where the network design is based on a coupled-resonator filter, here it follows from a singly-terminated three section band-pass Butterworth prototype. The components value of the Butterworth filter are in Table 2.4. Several topological transformations are adopted for a variety of goals.

Table 2.4 Output Network Parameters from Tchebyscheff filters with 0.2 dB ripple and R=50 Ω.

L_A	423 pH
L_B	221 pH
L_C	663 pH
C_A	191 fF
C_B	100 fF
C_C	63 fF

First of all, an impedance transformation is embedded in the filter structure to increase the impedance seen at the output of the cascode stage ($Q_9 - Q_{10}$) and increase the amplifier gain.

Moreover, a magnetic transformer is included in the network to perform the differential to single-ended conversion. Finally, the network is arranged to absorb as many parasitics as possible in the actual filter elements. The first transformation is illustrated in Fig. 2.39. The starting ladder filter prototype is shown in Fig. 2.39 (a), where $R_{LOAD} = 50\Omega$ is the load resistor. Norton transformation is applied to inductances $L_A - L_B$, resulting in the network shown in Fig. 2.39 (b). The transformation ratio is $n_l^2 = \left(\frac{L_A+L_B}{L_A}\right)^2 = 8.4$. The value of the capacitor C'_A is then $C'_A = \frac{C_A}{n_l^2}$, $L'_A = L_A \cdot n_l$, $L'_B = L_B \cdot n_l$. Second transformation is a Norton capacitive transformation, illustrated in Fig. 2.40. Transformer ratio is $n_c^2 = 1.21$. Inductors L'_A and L'_B are then divided by n_c^2 and capacitor C'_A is then multiplied by n_c^2. Before transformation, the capacitance C_C has been splitted in two parts, emphasizing that some of it is made up by the parasitic pad capacitance, C_{PAD}. Finally, L''_A and L''_B are implemented as

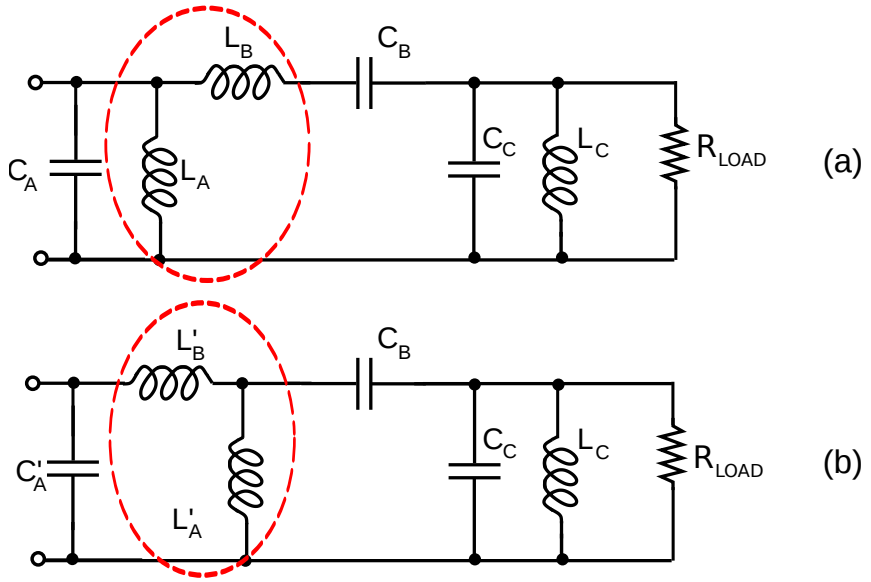

Fig. 2.39 First transformation to output network: (a) Singly terminated Maximally flat filter; (b) Norton transformation on inductors.

a magnetic transformer ($L3$ -L_4 in Fig. 2.35), whose equivalent circuit is shown in Fig. 2.41. in the dashed box. Notably, the parasitic capacitances of the coils L_3 -L_4 are absorbed in C_3, which is also made of the output capacitance of Q_9 -Q_{10} and of an explicit device. Layout of transformer is illustrated in Fig. 2.42. The capacitor C'_B is implemented as the series combination of two capacitors C_{OUT} to have a more symmetrical layout.

Inductor L_{out} is divided in two inductor and it is layouted in such a way the two inductor toghether have minimum magnetic coupling with the transformer L_3 -L_4 because in one inductor the current flows in clockwise and in the other the current flows in counterclockwise,

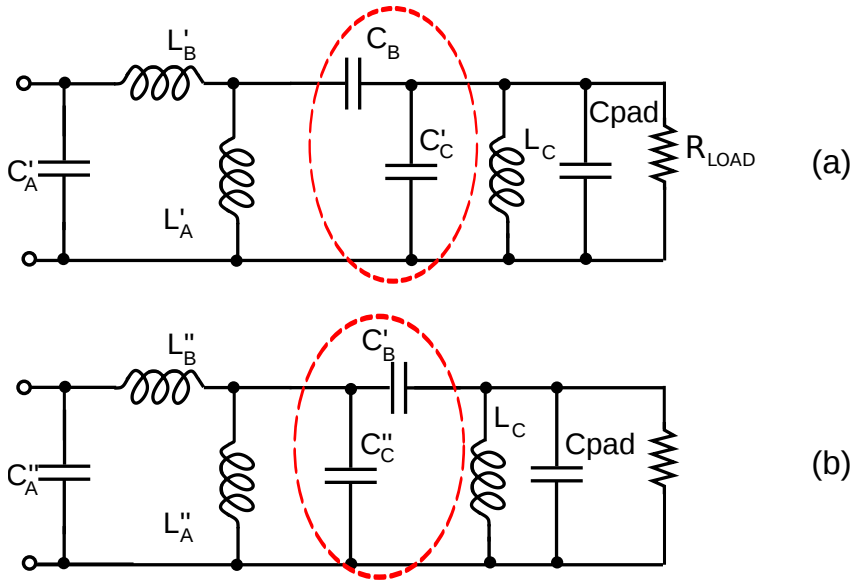

Fig. 2.40 Second transformation to output network: (a) After first transformation; (b) Capacitive Norton transformation.

then the currents generated by the magnetic field of L_3 -L_4 have opposite sign. Layout of L_{out} is depicted in Fig. 2.43.
The components in the final network are related to those in the filter prototype as:

$$\begin{cases} C_3 = \frac{C_A n_c^2}{n_l^2 n_t^2} \\ L_3 = \frac{L_B n_l n_t^2}{(1-k^2) n_c^2} \\ L_4 = \frac{L_A n_t}{n_c^2} \\ C_{out} = 2 C_B n_c \end{cases} \tag{2.36}$$

where $n_l^2 = \left(\frac{L_A+L_B}{L_A}\right)^2 = 8.4$, $n_c^2 = \left(\frac{C_B+C_C'}{C_B}\right)^2 = 1.21$ and $n_t^2 = k^2 \cdot \left(\frac{L_3}{L_4}\right) = 0.72$. Within the network passband, the resistance seen from the output of the cascode stage, R_{out} in Fig. 2.41 (b), is related to R_{LOAD} as: $R_{out} = n_l^2 \cdot n_t^2 / n_c^2 = 5 \cdot R_{LOAD}$. This make the amplifier to attain a large gain while directly driving an external $50\,\omega$ load.

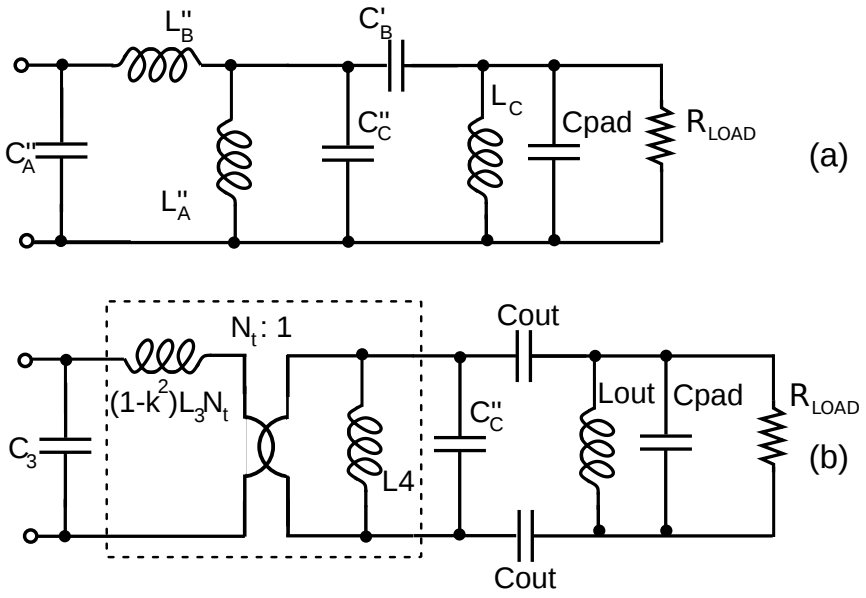

Fig. 2.41 Third transformation to output network: (a) After second transformation; (b) Use of a transformer to realize differential to single-ended transformation.

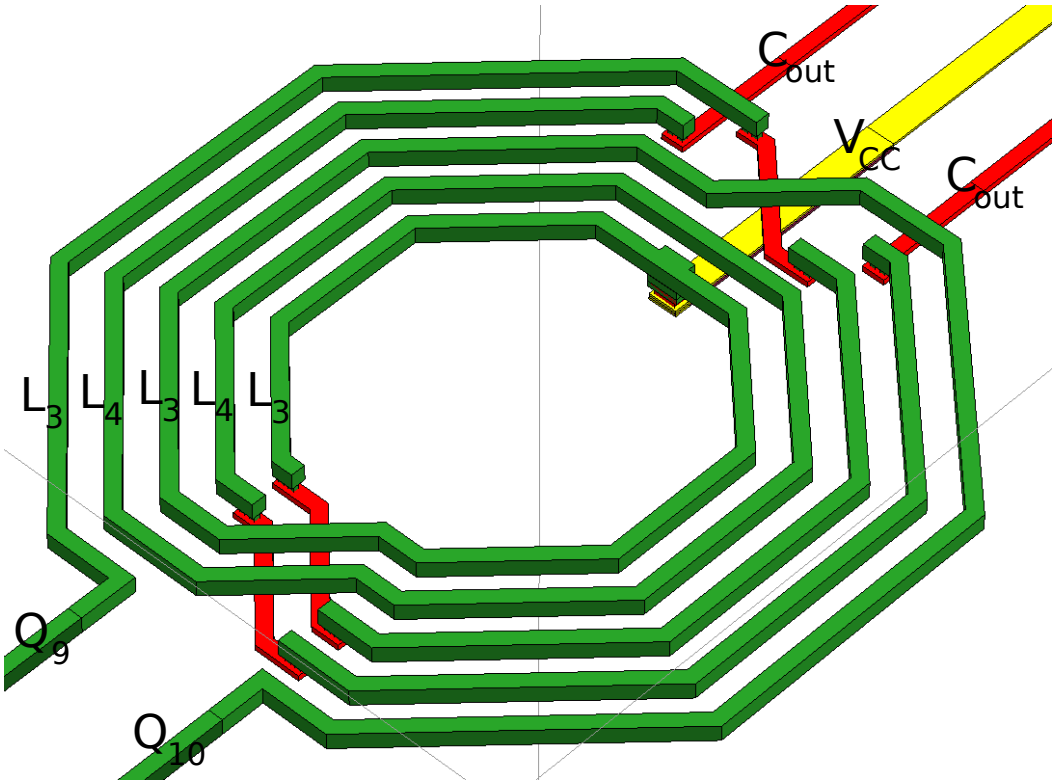

Fig. 2.42 Layout of the output transformer (L_3-L_4).

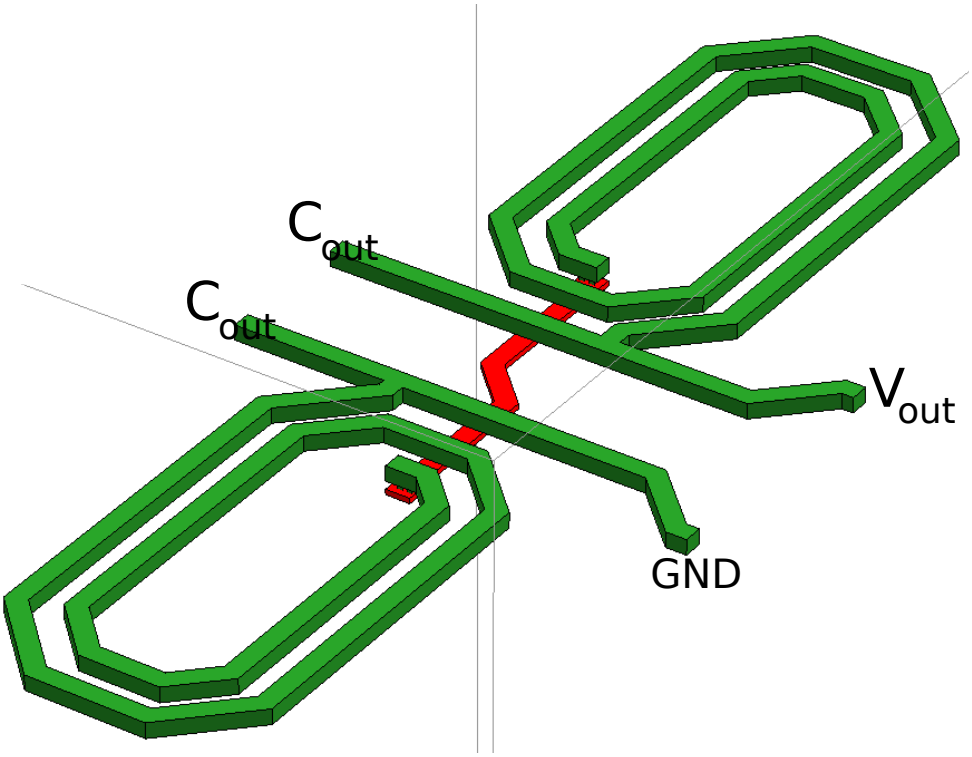

Fig. 2.43 Layout of the output inductor L_{out}.

2.6.2 Measurement Results

Prototypes of the proposed VGA have been implemented in Infineon BiCMOS technology. The micrograph of the chip is shown in Fig. 2.44. The VGA core occupies 760x240 μm^2, while the compensation and gain control circuits need an extra 220x200 μm^2 area.

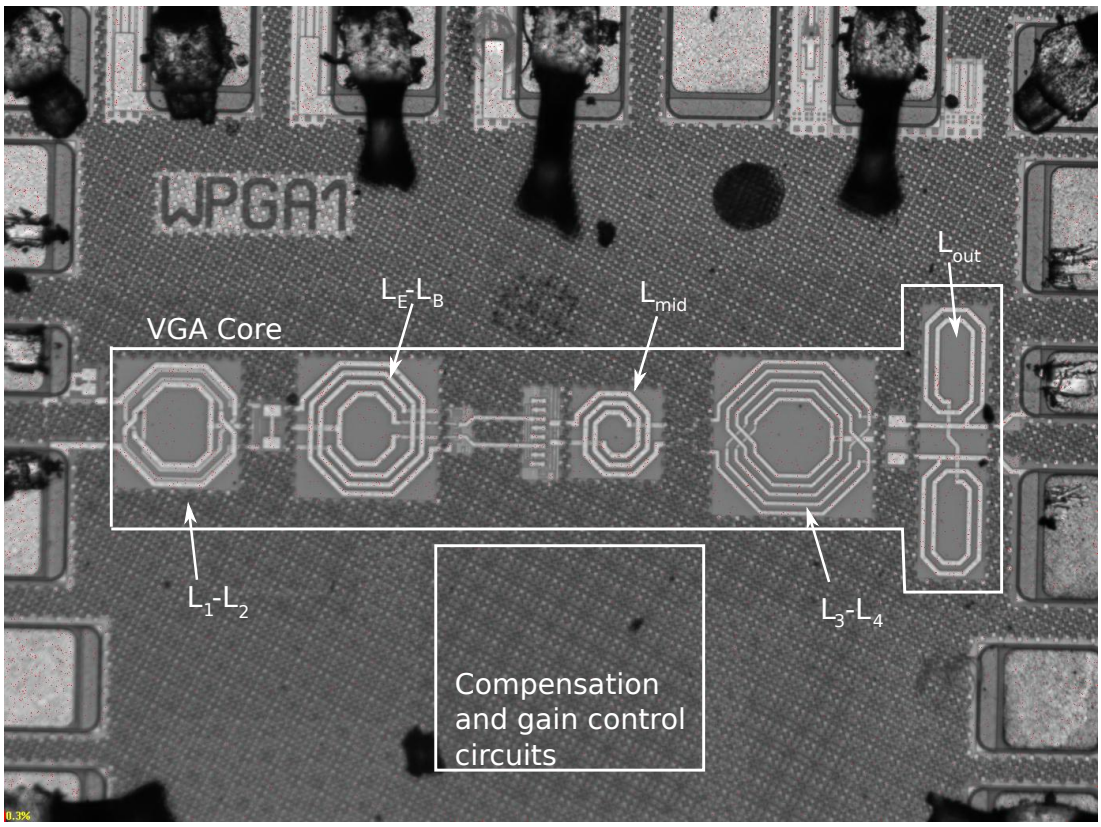

Fig. 2.44 Chip micrograph of the wideband VGA.

The measured input reflection coefficient is shown in Fig. 2.45 for various gain settings. There is a quite good matching ($S_{11} \leq -9$ dB) across the band. The measured amplifier gain is reported in Fig. 2.45. The gain at various gain setting without compensation circuits is plotted in Fig. 2.45 (a). Notice that if the gain is decreased, the current on $Q_9 - Q_{10}$ decreases and the drain capacitance change affecting the wideband behavior of the output network. Fig. 2.45 (a) shows instead the gain when the controls are ON (the current flowing through cascode stage is constant at various gain settings) and $I_{p,max} = 2.5$ mA (optimum phase error compensation configuration).

Maximum gain is 17 ± 2.6 dB from 15.5 to 39 GHz. The maximum attainable gain variation is as large as 43 dB. Some excess gain ripple is observed within the amplifier pass-band due to a higher than expected gain peaking around 35 GHz. However, as the VGA is expected

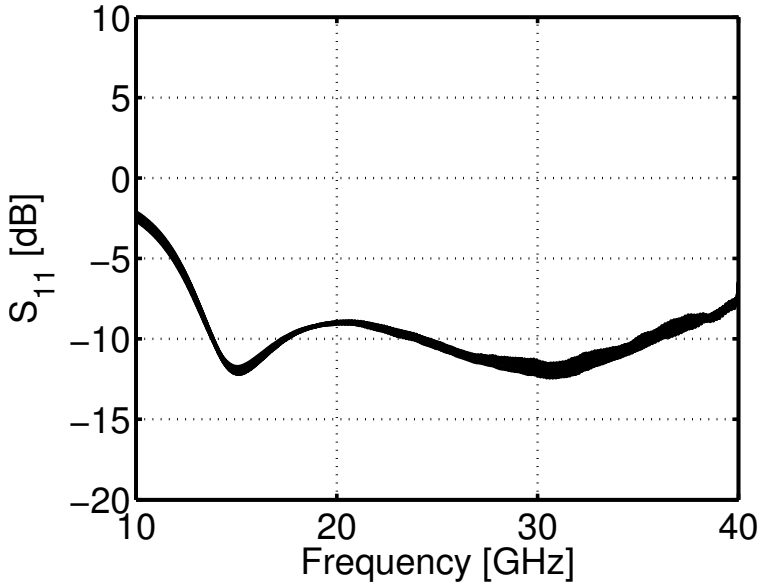

Fig. 2.45 Measured input reflection coefficient.

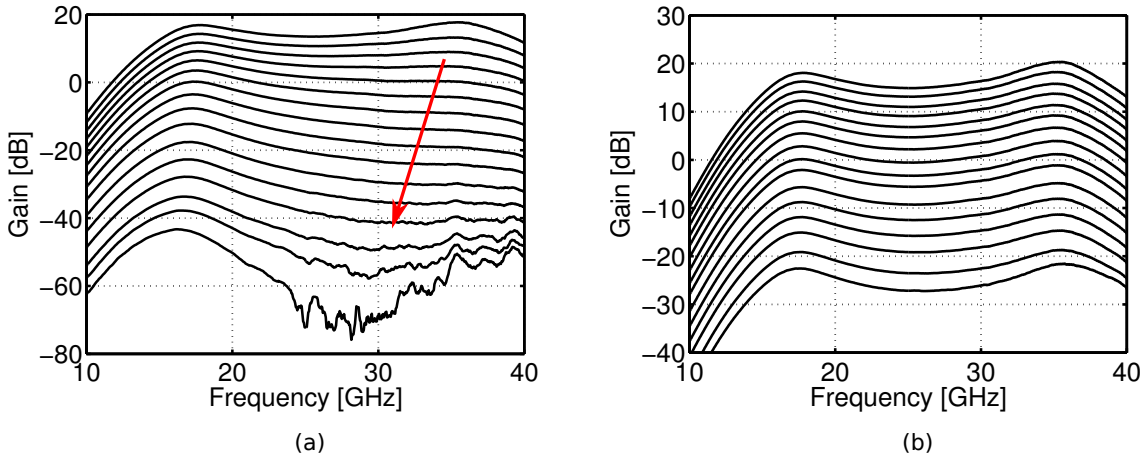

Fig. 2.46 Measured gain at various settings: (a) Without phased controls; (b) With both phase controls activate and $I_{p,max} = 2.5$ mA.

to be operated in several narrow-band systems, avoiding the use of the entire instantaneous bandwidth at once, this does do not seem to be a paramount issue.

The effect of the compensation circuits is shown in Fig. 2.47, where the measured phase shift variation, $\Delta\phi$, is plotted as a function of the gain. Both the case without any compensation, and with the two compensation circuits on are reported; in the latter case, for a few values of the maximum value of I_p , $I_{p,max}$. The more $I_{p,max}$ is increased, the smaller is the maximum value $C_{\pi 5}$ achieves, and the least the impact of the variation of the

zero $\omega_z = \frac{1}{C_{\mu 5}+C_{\pi 5}r_{b5}}$ on $\Delta\phi$. However, if $I_{p,max}$ is too large, then the time constant at the emitter of $Q_3 - Q_5$ increases too much, adversely affecting $|\Delta\phi|$. Figure 2.47 shows that $\Delta\phi < 30^\circ$ in the native VGA, while the use of the proposed compensation techniques with the optimal $I_{p,max} = 2.5$ mA choice reduces the phase shift variation to $< 3^\circ$ for a gain variation $\Delta G = 23$ dB. The effectiveness of the proposed compensation techniques in a wideband

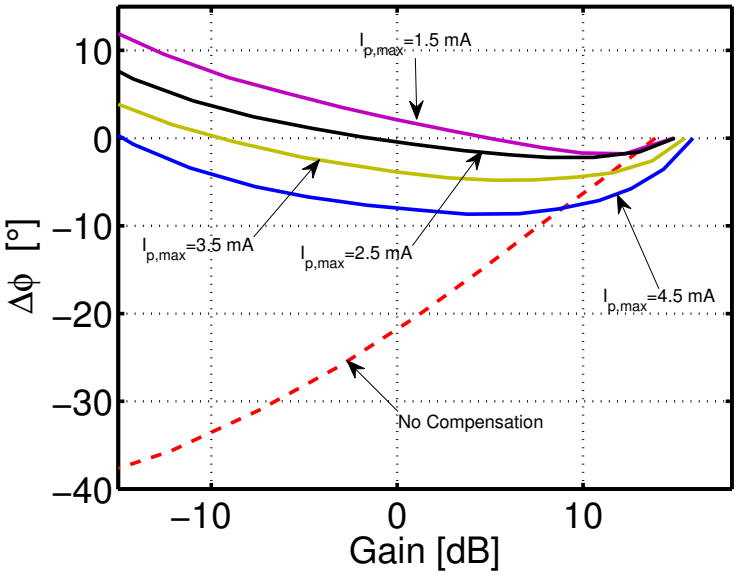

Fig. 2.47 Phase error at 28 GHz at various values of I_{pmax} and with no phase compensations.

fashion is supported by the measurement results reported in Fig. 2.48. For an overall gain variation of $\Delta G = 23$ dB, $< 3^\circ$ for frequencies up to 30 GHz, while in the $30-40$ GHz range $< 5^\circ$ if $\Delta G$is limited to 19 dB. The group delay results are plotted in Fig. 2.49, here the positive contribute of the compensations is well visible. In Fig. 2.49 (a) the group delay is plotted for $\Delta G = 23$ dB, it is grater than 10 ps at 28 GHz without phase error compensations. The group delay enabling the compensation circuity is plotted for a gain variation of 23 dB in Fig. 2.49 (b). Here $\Delta\tau_g < 4$ ps.
Some measurements at high temperature has been done, in Fig 2.50 the phase error at 28 GHz is depicted when all the compensations are enabled and $I_{p,max} = 2.5$ mA for two different temperature, 25° and 75°. Phase error is still less than 5° for a gain variation grater than 25 dB. This is to prove that the phase error compensations are robust versus temperature variations.

The measured and simulated noise figure of the amplifier, when the compensation circuits are on and the gain is maximum, is shown in Fig. 2.51 in solid, and dashed line, respectively.

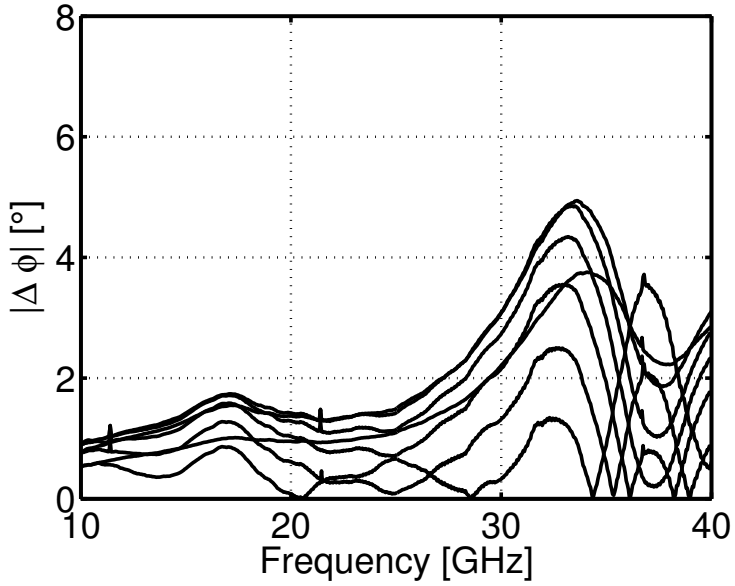

Fig. 2.48 Phase error in the bandwidth of the amplifier for 19 dB of gain variation.

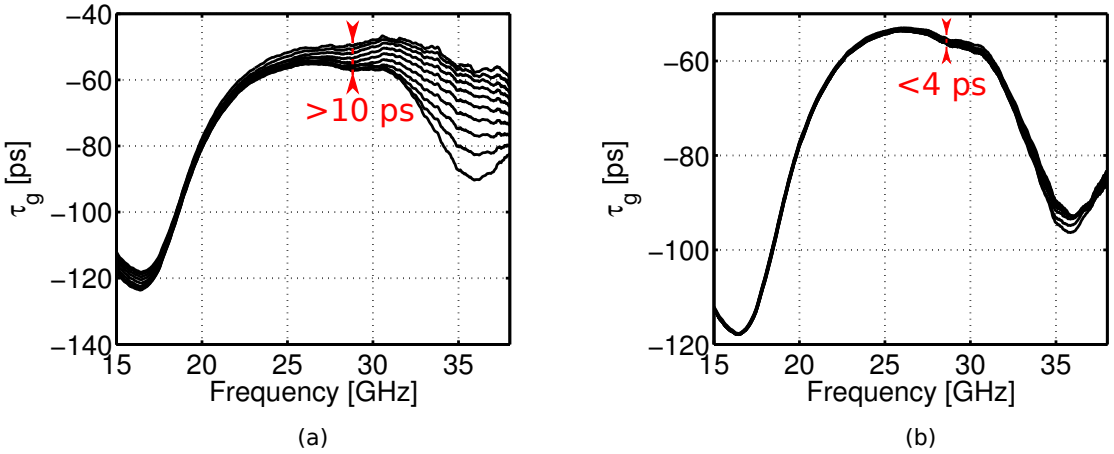

Fig. 2.49 Group delay: (a) Without compensations; (b) With both compensation circuits activated and $I_{p,max} = 2.5$ mA.

The NF spans from 3.6 to 9 dB in the VGA band. There is a good agreement between the measurement and the simulation results. The measured input-referred intercept point of the VGA is $IIP3 = -1$ dBm at 18 GHz and 0 dBm at 28 GHz. The amplifier core draws 15.7 mA, inclusive of the bias and gain control circuitry, while the compensation circuits draw up to 15.8 mA. The supply voltage is 3.3 V.

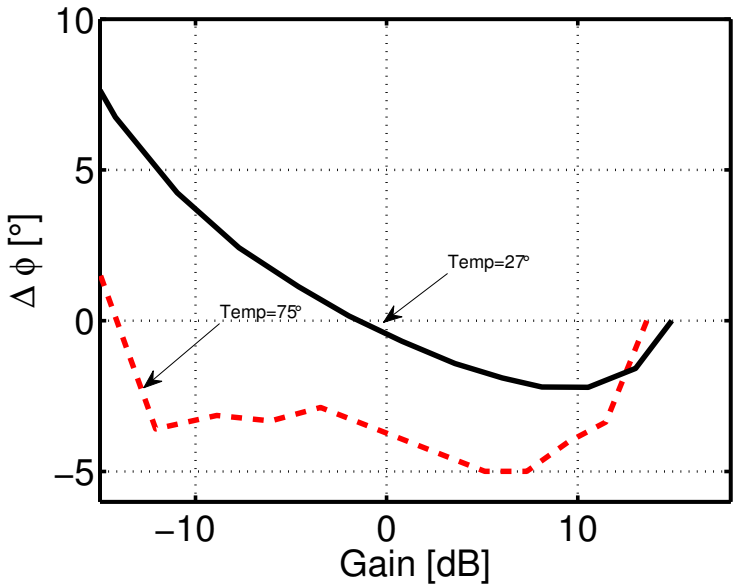

Fig. 2.50 Phase error with both compensations enabled, $I_{p,max} = 2.5$ mA at 27° (solid line) and at 75° (dash line).

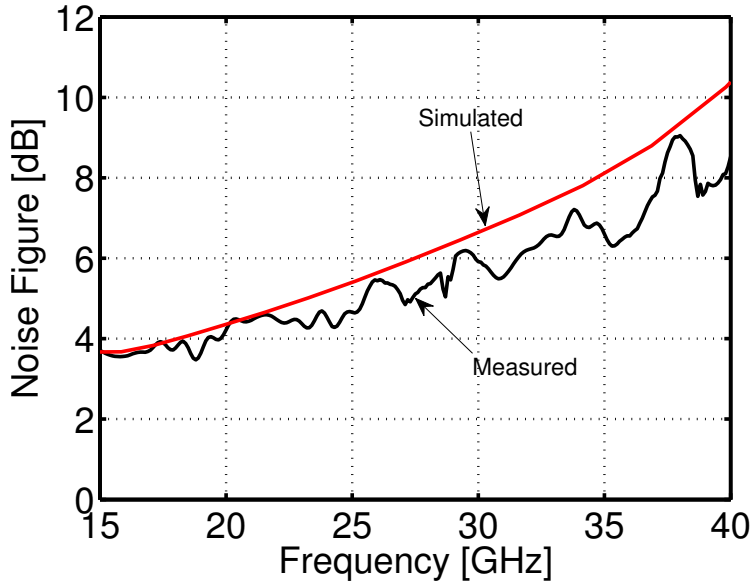

Fig. 2.51 Siumulated and measured noise figure.

The performance of the amplifier is summarized and compared to other VGA designs operating in the $K_u - K_a$ bands in Table 2.5. The proposed VGA shows the smaller phase error for the larger gain variation, while being broadband.

Table 2.5 Comparison with the state-of-the-art.

	This work	[40]	[41]	[42]
Tech.	SiGe BiCMOS	SiGe HBT	SiGe BiCMOS	SiGe BiCMOS
Freq. [GHz]	15.5-39	32-34	13-15	35
Gain [dB]	17	20	2.5‡	-2
ΔG [dB]	23	11	17.6	7.5
$\Delta\phi$ [$^{\circ}$]	3$^{\sharp}$	4	5	20
NF [dB]	3.6-9	3.4	10†	9†
IIP3 [dBm]	-1	-19	-6†	-6†
P_{dc} [mW]	104	33	119‡	35†

$^{\sharp} \leq 30$ GHz, †Entire RX chain. ‡Stages with variable gain feature.

2.7 CMOS VGA for $5\,G$ Networks

One of the possible frequency bands that could be used in $5\,G$ communication system is K_a band $(26.5-40)$ GHz [10]. Several works have been already done to demonstrate the feasibility of the systems and to evaluate the performances [47], [48] .
Till some years ago SiGe bipolar technology have been widely used for sub-millimeter and millimeter wave transceivers [49], [50]. However it is expensive and challenging to integrate SiGe bipolar analog components with digital part implemented in CMOS. A complete CMOS transceiver is also challenging at mm-wave due to the lower f_T compared with the SiGe devices, however CMOS offers low cost, higher level of integrability and technology scaling. Technology evolution trend lead now to a CMOS devices with f_T about 300 GHz then suitable for frequency operation till $80-90$ GHz [48].
This Section presents a variable gain amplifier operating at 28 GHz in 40-nm CMOS technology and suitable for phased array system.
The design of the VGA is described in Section 2.7.1, and the simulated results are described in Section 2.7.2.

2.7.1 Design

A simplified schematic of the VGA is shown in Fig. 2.52. The amplifier is based on a three stage inductive degenerated folded cascode topology to provide low voltage operation coupled to a sufficient gain as well as low noise figure [51]. The first stage is used for the input-matching, second stage is a digital current steering to feature the gain variation and the third stage is a cascode device used to desensitize the output impedance from the gain variation. Allowing CMOS devices to operate rail-to-rail, this topology brings a great benefit in terms of linearity too [52]. Drawback of this configuration is the power consumption but usually it is not a major requirement in phased array system.
First stage is an inductively-degenerated transconductor optimized for low noise figure. CMOS deices work at f_T current density and the input reactive network is based on a doubly-terminated two section band-pass Bessel ladder filter prototype.
A transformer is used to bias the gate of the transistor M_1 and M_2 at the voltage V_G. The transformer ratio is $N_t = 1$, $L_1 = 330$ pH and $L_2 = 920$ pH, the coupling factor is $k = 0.61$. The leakage flux inductance of the coupled inductors L_1 and L_2 is employed with the gate-source capacitance of M_1 and M_2 as series elements of the ladder filter. The input capacitance C_1 is the parallel of a MoM capacitor and the parasitic capacitance of the input PADs.
First stage is connected to the second stage by the inductor $L_{C1} = 540$ pH that resonate with the parasitic capacitance of the devices at the operating frequency. Inductor L_C is divided

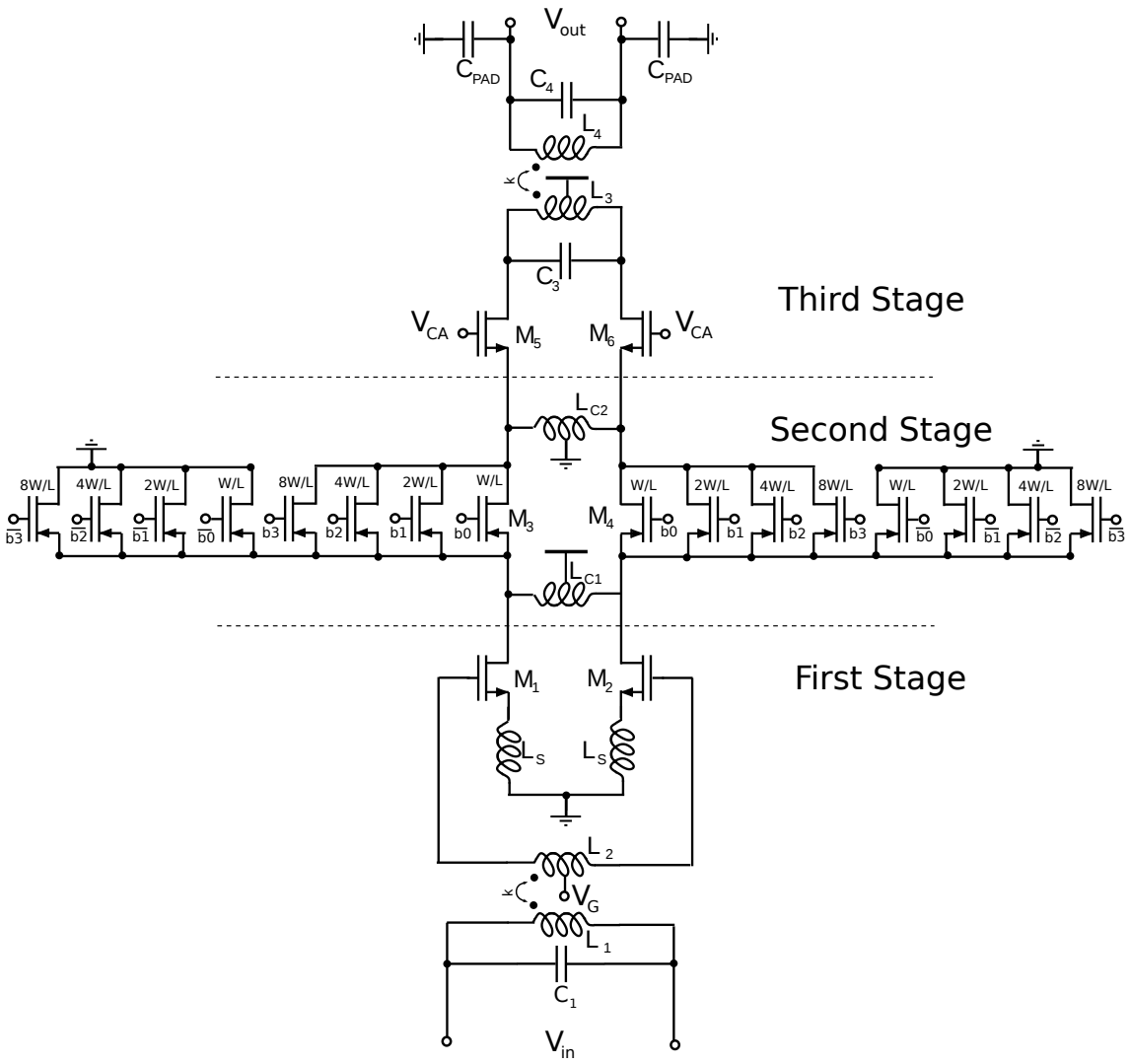

Fig. 2.52 Simplified schematic of the CMOS VGA.

in two inductor and it is layouted in such a way the two inductor together have minimum magnetic coupling with the close by inductive element because in one coil the current flows in clockwise and in the other the current flows in counterclockwise.

Second stage of the circuit features the gain variation by digital current steering, the transistors are used as switches. The aim of this circuit is to steer the current through the load (increase the gain) or through ground (decrease the gain). In order to do not change the impedance seen from the first stage when the gain is varied, the switches are controlled in such a way the current and the transconductance of the second stage is constant at the different gain settings. Looking at Fig. 2.52 (Second stage), for example, the settings for the maximum gain is ($b0 = 1$, $b1 = 1$, $b2 = 1$, $b3 = 1$), all the signal current floes through the third stage.

If the first LSB is switched off, ($b0 = 0$), hence ($\bar{b0} = 1$), a small part of the current goes at ground and the gain is decreased but the sum of the current that flows through the drain of all the p-MOS switches is constant (switches controlled by the signal b_i and $\bar{b_i}$ have the same $\frac{W}{L}$). In this way the impedance seen from the first stage is quite independent from the gain variation. If it were not so , the Miller effect (C_{gd} of M_1, M_2) would make the input impedance of the amplifier dependent from the gain variation thus possible a increment of the phase error. The input word that gives the gain variation is communicated by a serial to parallel interface.
Second stage communicates with third stage through the inductor L_{C2} that resonate with the capacitances of the devices (L_{C2} is designed as the inductor L_{C1}). M_4 and M_5 feature a common gate amplifier. This stage is used as buffer to isolate the load from the digital current steering stage, hence to avoid modulation of the output tank resonance by the output capacitance of the current steering stage (possible cause of phase error). Furthermore it is used to increase the output impedance, hence the gain. M_4 and M_5 are biased at V_{CA} optimum point for high linearity of the amplifier. A transformer (L_3, L_4) is adopted to transform the output impedance of the load by 4. The values of the primary and secondary coils inductances are respectively $L_3 = 76$ pH, $L_4 = 370$ pH and the coupling factor is $k = 0.64$. Capacitance C_3 and C_4 absorb the parasitic capacitance of the primary and secondary respectively, the leakage flux inductance of the transformer ($(1-k^2)L_4$) resonates with the parasitic capacitance of the PADs at a frequency slighly higher than the operating frequency.
The simulated results of the CMOS variable amplifier are described in the Section 2.7.2.

2.7.2 Simulation Results

The proposed VGA have been implemented in 40-nm CMOS technology. The layout of the chip is shown in Fig. 2.53. The VGA core occupies 490x290 μm^2.
The current consumption is 64 mA and the supply voltage is 1.1 V. The simulated gain variation is plotted in Fig. 2.54. The center frequency is 28 GHz and the bandwidth is 5 GHz, from 25.4 to 30.4 GHz. The gain is varied from -12.5 dB to 10 dB. The gain is digitally controlled by an amplitude word through a serial-to-parallel interface. Gain variation is not linear-in-dB but since the control is digital, an algorithm can feature the right conversion. Last state is the isolation state, the simulated attenuation is -46 dB. Simulated input matching is depicted in Fig. 2.55. Amplifier is well matched, S_{11} is less than -15 dB from 25 to 34 GHz and it is independent from the gain variation.
The simulation of the noise figure varying the gain is plotted in Fig. 2.56 (a). The minimum noise figure is 3.6 dB. The noise figure when the amplifier gains -12.5 dB is 17.5 dB. In Fig. 2.56 (b) the maximum gain is depicted at different values of the amplitude word.

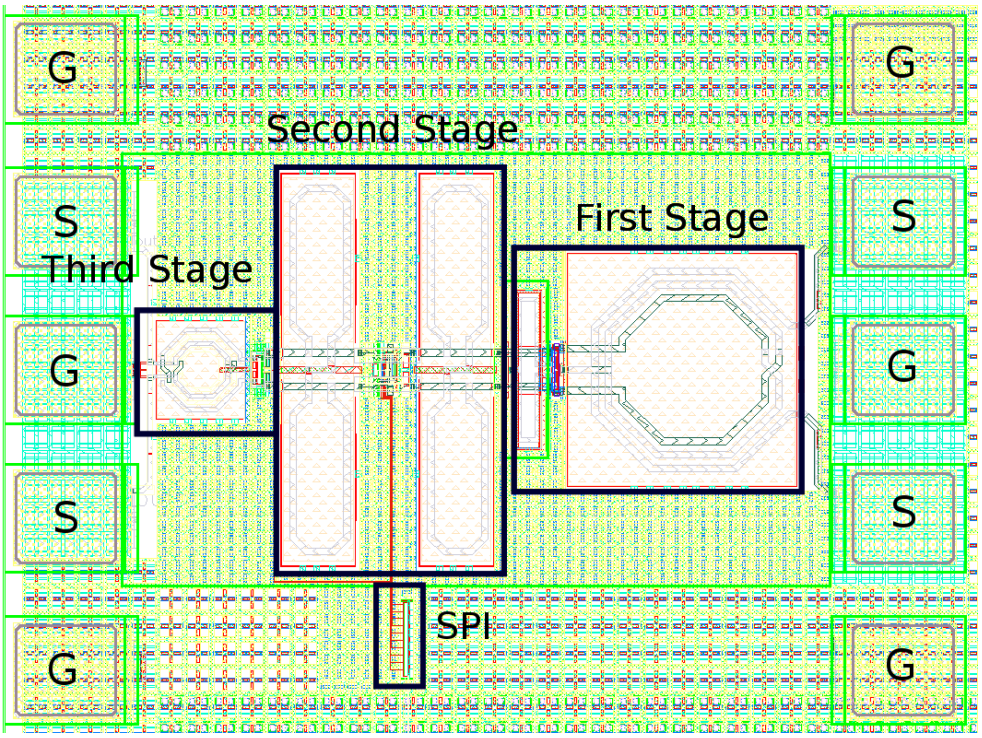

Fig. 2.53 Layout of the CMOS VGA.

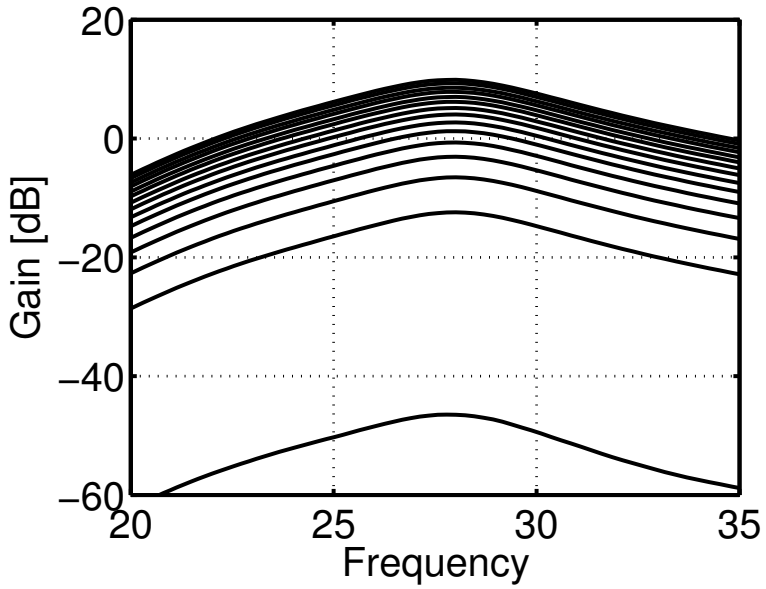

Fig. 2.54 Simulated S_{21} at different gain states.

Linearity characterization is described in Fig. 2.57. OIP3 is plotted in Fig. 2.57 (a) at the various gain states. Maximum gain (10 dB) corresponds to amplitude word 1, minimum gain (−12.5 dB), corresponds to amplitude word 14. IIP3 is depicted in Fig. 2.57 (b) at various

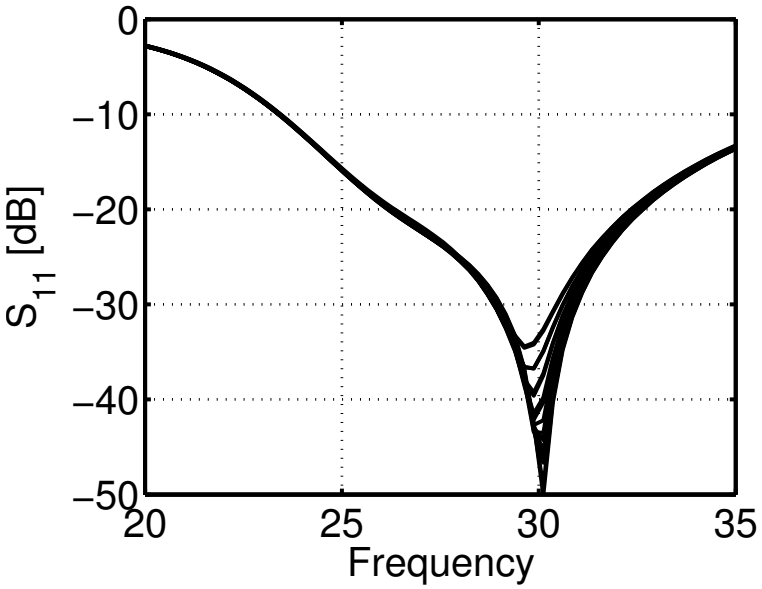

Fig. 2.55 Simulated S_{21} at different gain states.

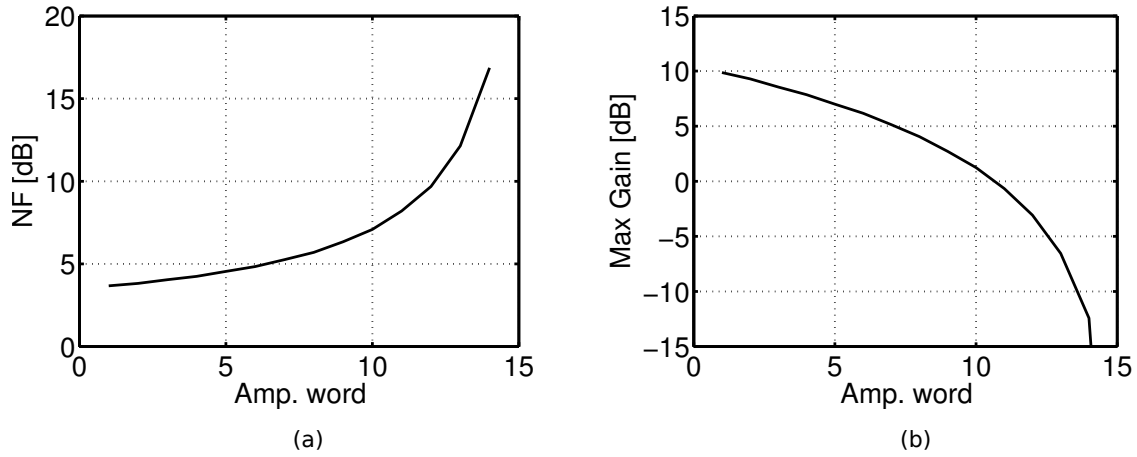

Fig. 2.56 (a) Simulated NF at different gain states; (b) Maximum gain at different gain states.

gain settings. At maximum gain, IIP3 is 5.9 dBm, this is a good results if compared with the state-of-the-art.

Phase behavior is described by Fig. 2.58 at two different frequencies. Fig. 2.58 (a) shows the phase error respect to the state at maximum gain at center frequency (i.e. 28 GHz). Fig. 2.58 (b) instead shows the phase error at 31 GHz. In both the cases, phase error is less than 2° then the phase of the amplifier is quite independent from the gain variation. The simulated group delay variation $\Delta\tau_g$ for various gain setting is described by Fig. 2.59. The maximum variation is about 3 ps close to the center frequency of the amplifier. This is due to the fact

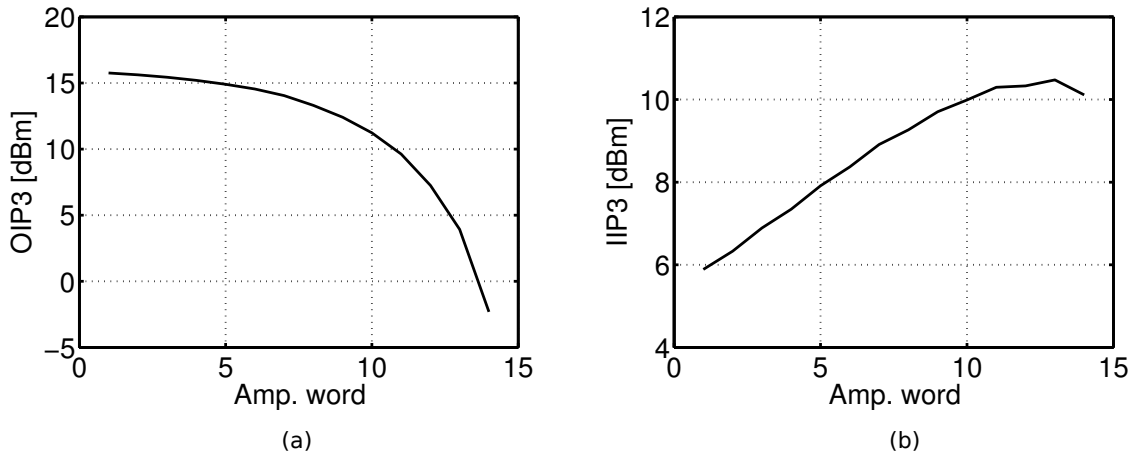

Fig. 2.57 (a) Simulated OIP3 at different gain states; (b) Simulated IIP3 at different gain states.

that the VGA is narrow band (resonant load has high Q) and the center frequency of the reactive load has a small sensitivity to the gain variation. Since in a narrow band phased array application phase shifters are used to control the phase of each channel, the phase error is the most important parameter in this case.

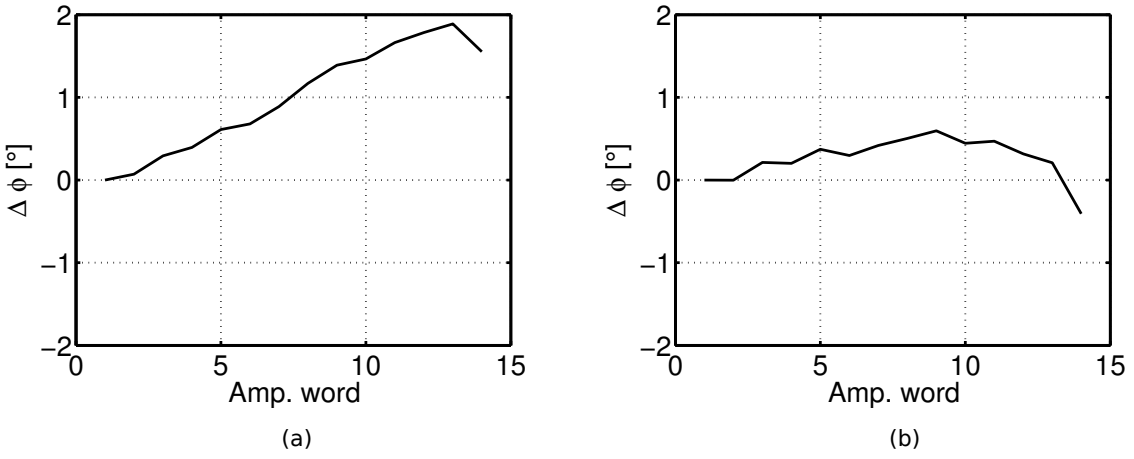

Fig. 2.58 Simulated phase error respect to the state at maximum gain: (a) at 28 GHz; (b) at 31 GHz;

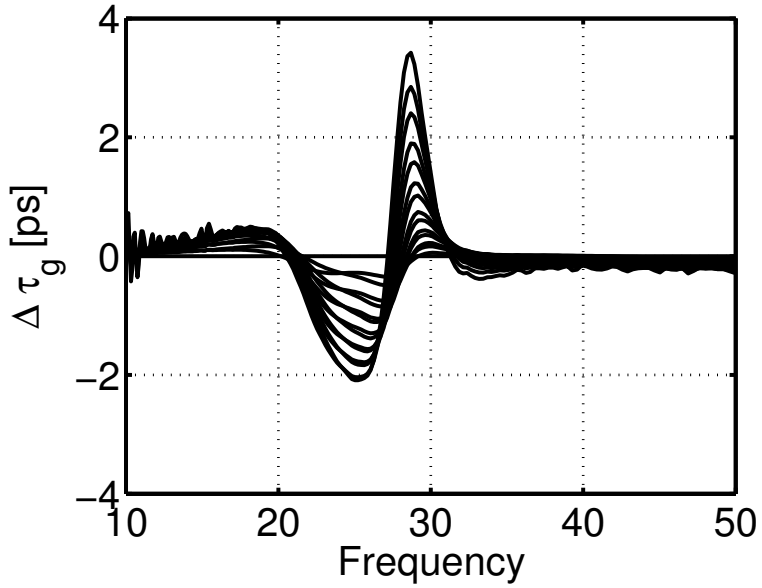

Fig. 2.59 Simulated group delay variation, $\Delta\tau_g$, for various gain settings.

2.8 Conclusion and Comparison

In this Chapter four different VGAs for phased array systems have been presented. An investigation on the phase error caused by a gain variation is presented and some compensations have been implemented. Table 2.6 summarizes all the results.

CMOS (simulated) and SiGe VGAs show similar performances in terms of power consumption, OIP3 and noise figure. CMOS implementation features less maximum gain than SiGe VGAs but higher IIP3.

Table 2.6 Comparison with the state-of-the-art.

	Cap. compensation	Curr. compensation	Curr. compensation	Switch-steering
Tech.	SiGe	SiGe	SiGe BiCMOS	CMOS 40 nm
Freq. [GHz]	8-12.5	10-14.4	15.5-39	25.5-30.4†
Gain [dB]	16	13	17	10†
ΔG [dB]	24	22	23	22.5†
$\Delta\phi$ [°]	6	2	3	2†
NF [dB]	4.6	5.1	3.6-9	3.6†
IIP3 [dBm]	-	-3	-1	5.9†
P_{dc} [mW]	60	83	104	70.4†

†Simulated results.

In terms of compensation circuitry, capacitive compensation is the simplest solution and does not increase the power consumption but the phase error is not completely eliminated. Current compensation is a robust solution that compensates almost completely the phase variation (at list for a substantial gain range $\Delta G > 20\,\mathrm{dB}$) at the expense of an increment in terms of power consumption due to the compensation mechanisms.

Chapter 3

Low Phase Noise VCO Design

3.1 Motivation

The continuous growth of personal wireless communications demands high-bandwidth front-end systems. Recently, many research efforts have focused on the development of millimeter wave communications systems. In order to reduce the complexity of the transceiver, the local oscillators run at frequencies close to the RF signal. The design of VCOs capable of achieving simultaneously low phase noise and wide tuning range is a challenging task, especially when frequencies are $> 10\,\text{GHz}$ and the capacitive parasitics give an important contribution. The upcoming fifth generation (5G) wireless communications technology demand for a further increase of communication data-rate and flexibility [53]. The use of more complex modulation schemes allows higher data-rate but the requirements in terms of signal-to-noise ratio become stronger as described in Fig. 3.1.
SNR is directly related to the VCO phase noise, therefore VCOs will play a really important role in these high data-rate communication systems. Chapter 3 describes some VCOs in K-band. The K-band refers to the frequencies close to $f = 20\,\text{GHz}$ and it is one of the possible candidate for the future 5G. The VCOs can also be used (combined with a frequency multiplier) in the 60 GHz or even higher bands (E-band), as other possible solutions for 5G network [53]. Moreover, the VCOs (combined with a frequency divider) could be employed in conventional cellular base stations operating in the 1-3 GHz range.
In the section 3.2, several embodiments of the K-band VCO are considered. The focus is on the theoretical and practical limits of the minimum achievable phase noise for a given tank quality factor and supply voltage. The design strategies and techniques used to achieve a low phase noise performance without sacrificing tuning range are reported. Some VCO designs are described in detail in section 3.3. Dynamic biasing is investigated to ensure robust start-up of the proposed class-C VCOs. In addition, a characterization of the phase noise performance across temperature variations is reported in section 3.4.

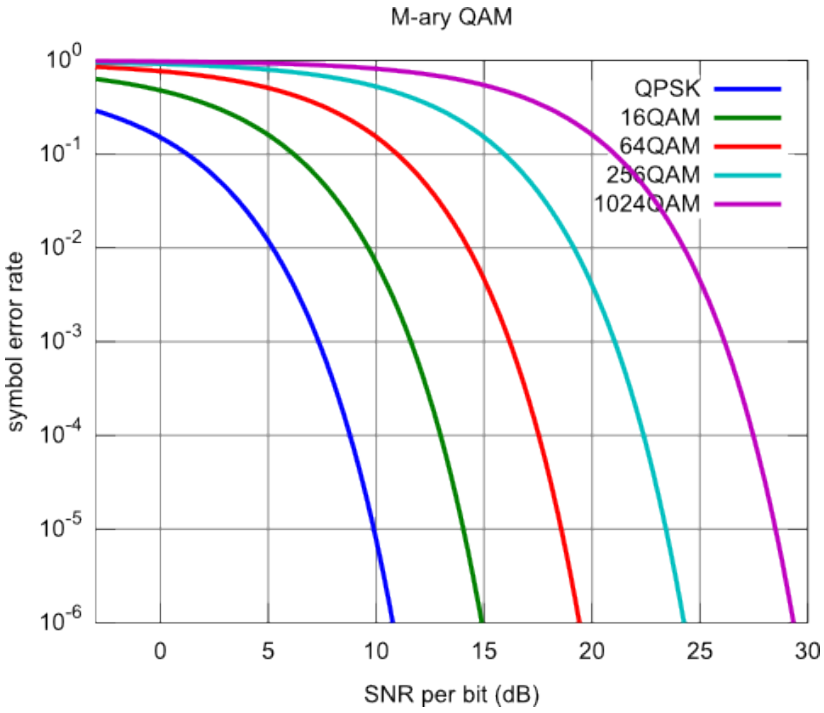

Fig. 3.1 BER vs. SNR at different modulations.

3.2 Minimization of Phase Noise

The main goal of this work is to investigate the minimum achievable phase noise in K-band bipolar VCOs, while guaranteeing a wide tuning range to address process, supply voltage, and temperature variations. It is well known that the phase noise sideband at an offset $\Delta\omega$ from the carrier frequency ω_0 is described by the Leeson's equation [24][1]:

$$\mathscr{L}(\Delta\omega) = 10\log_{10}\left[\frac{kTFR_T}{V_0^2}\cdot\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{3.1}$$

where Q is the overall tank quality factor, R_T is the equivalent parallel tank resistance, V_0 is the amplitude of oscillation, and F is the oscillator excess noise factor. To achieve a low phase noise, a high tank quality factor is essential. Moreover, a low tank impedance at resonance (i.e. a low value of R_T), and a large swing help reduce the phase noise. Finally, an oscillator topology yielding a low F is beneficial.

[1] In this formulation of the Leeson's equation the $1/f^3$ noise sidebands are neglected.

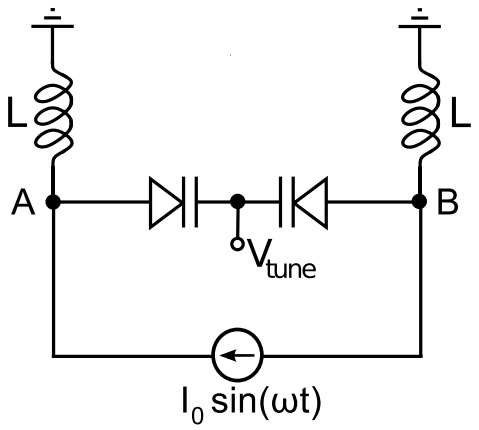

Fig. 3.2 Test bench to simulate Q_C at large signal operation.

3.2.1 Optimization of the tank quality factor

In general, the Q of an LC tank depends on the quality factor of both reactive elements [54], i.e. $Q = (Q_L^{-1} + Q_C^{-1})^{-1}$, where Q_L is the inductor quality factor, and Q_C is the capacitor quality factor. Typically, in the low-GHz range, the main source of tank losses is the integrated inductor. In the K-band, however, the contribution of the capacitive part of the tank is significant. This is particularly the case in pure bipolar technologies, where only *pn*-junctions are available as varactors, and switched capacitor banks are not easily implemented. At large amplitudes of oscillation, the varactor can be forward biased for part of the oscillation cycle, resulting in a dramatic degradation of Q_C. Simulations of the varactor quality factor have been carried out by means of the circuit shown in Fig. 3.2. The dc bias voltage across the junctions is set by V_{tune} (the inductors in Fig. 3.2 are large ones acting as chokes). Ac-wise, the varactor is current-driven to emulate the actual condition occurring when it is part of a parallel tank operated at resonance. The time-domain result of the large-signal simulation is reported in Fig. 3.3, where the waveform of the voltage $V_A(t)$ (see Fig. 3.2) is shown. At large ac-currents, the positive voltage half-wave exceeds V_{tune} plus the junction turn-on voltage, and it gets chopped. On the contrary, the negative half-wave swings to a peak labeled V_{pk} (in absolute value).

The simulated varactor quality factor at $f = 20\,\text{GHz}$ is shown in Fig. 3.4 as a function of both V_{tune}, and V_{pk}. At small values of V_{pk}, the small-signal value of Q_C is observed. It is larger for larger values of V_{tune}, as the varactor capacitance is smaller for larger values of V_{tune}, while the losses are basically unaltered by V_{tune}. For larger values of V_{pk}, simulations show a slight degradation of Q_C, probably due to an increase in the junction dynamic conductance. The degradation becomes dramatic when the junction is completely forward-biased during part of the cycle and the voltage waveform gets chopped. The technique used to couple the

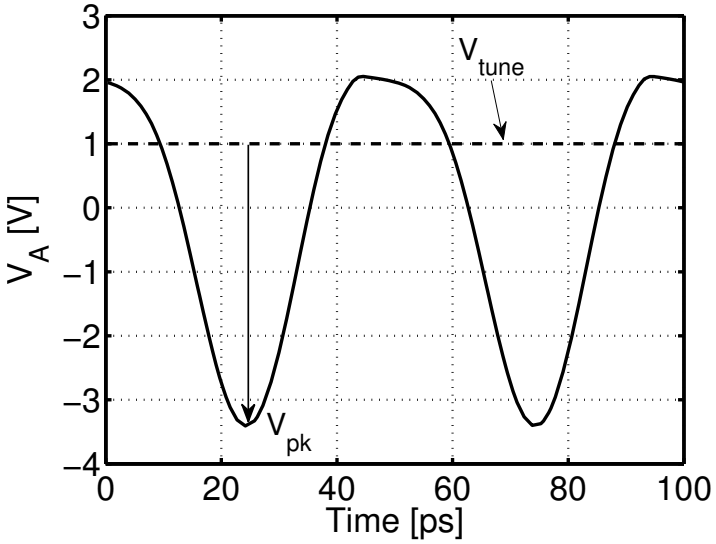

Fig. 3.3 Large signal simulation across the tank.

varactor to the tank is therefore essential to limit the forward-biasing of the junction during the oscillation cycle, without impairing its frequency tuning capabilities.

There are several possible approaches to combine the varactor with an inductive element and make the LC tank. The most straightforward one is direct coupling, as depicted in Fig. 3.5(a). The drawback of this configuration is that V_{tune} is required to be higher than the supply voltage V_{CC} to limit the forward biasing of the diode. Although the use of such large tuning voltages is somehow cumbersome (and not required) in CMOS technologies where MOS varactors are available, it is quite common practice in the context of bipolar technologies [55–57], and also in products based on compound semiconductors [58].

Another design option is to add series bias capacitors, C_C, in order to bias the anode of the varactor to ground, as depicted in Fig 3.5(b). However, such a choice trades with either reduced tuning range, or worse phase noise performance. Small capacitors C_C reduce tuning range, as they are placed in series with the varactors. Moreover, small capacitors have a relatively large series resistance (R_{par} in Fig 3.5(b)) and deteriorate the tank Q. On the contrary, large coupling capacitors add large parasitic capacitances (C_{par} in Fig 3.5(b)) at the output nodes, thus limiting the tuning range.

The use of a magnetic transformer is a better alternative to ac-couple the varactor to the tank. The arrangement is shown in Fig. 3.5(c). The advantage of this configuration is twofold. First, the anode of the diodes can be biased to ground and complete tuning range can be achieved for $V_{\text{tune}} < V_{\text{CC}}$. Second, choosing an appropriate turn ratio, the swing across the

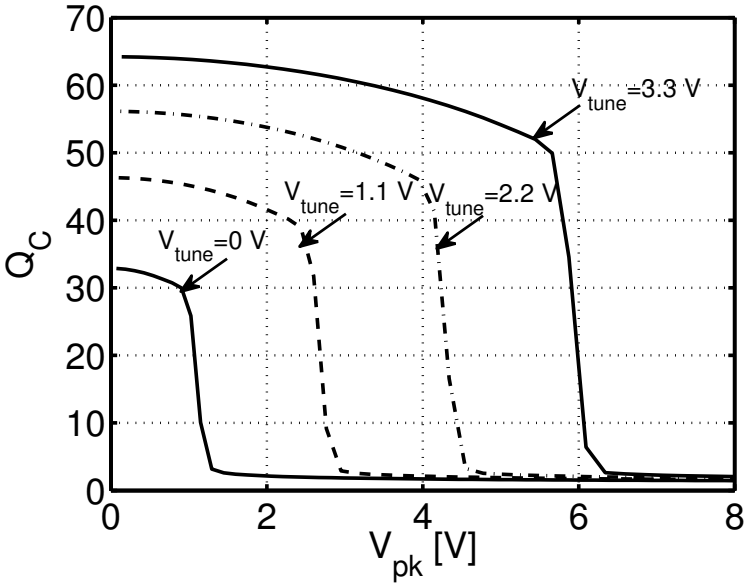

Fig. 3.4 Simulated varactor quality factor at $f = 20\,\text{GHz}$.

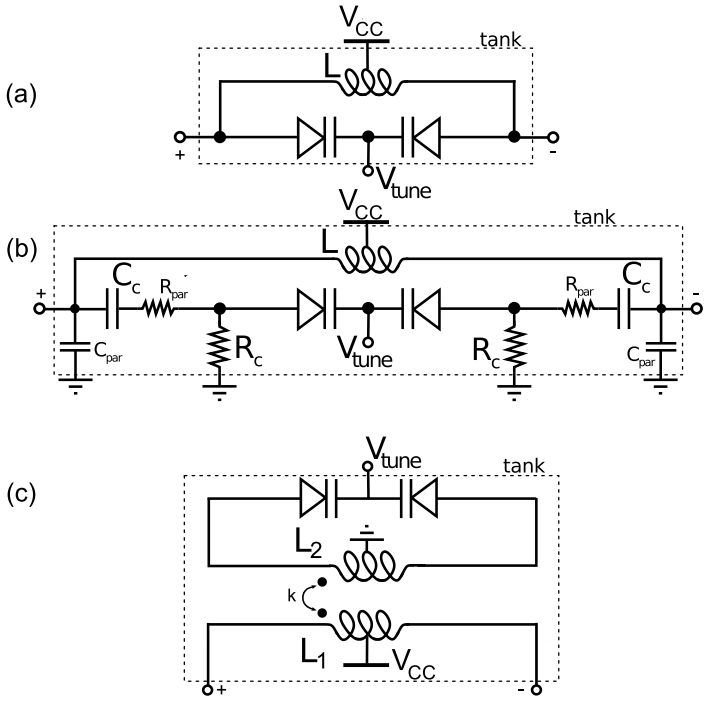

Fig. 3.5 (a) Direct coupled varactor. (b) Capacitive ac-coupled varactor. (c) Transformer-coupled varactor.

varactor can be reduced as compared to the output swing of the VCO, further limiting the possibility that the junction turns on even for large oscillation amplitudes.

3.2.2 Biasing the active elements: class-C versus class-B and Colpitts oscillator

From (3.1), it is clear that both the output voltage amplitude V_0 and the noise factor F play an important role in the optimization of the phase noise performance. An appropriate choice of the oscillator topology and bias circuitry can significantly decrease the oscillator phase noise.

A typical oscillator arrangement makes use of a cross-coupled differential pair to synthesize a negative resistance, able to compensate the losses of a parallel LC tank and sustain the oscillations, as depicted in Fig. 3.6. Since bipolar devices are used in this design, care must be taken such that the transistors do not enter the saturation region of operation. If the base-collector junctions of the cross-coupled pair devices turn on, the output voltage is clipped, limiting the oscillator output swing. In order to extend the output voltage swing and prevent the transistor to operate in the saturation region, the base and collector terminals of the cross-coupled devices can be ac-coupled by means of capacitors C_{bias} (see Fig. 3.6). Consequently, the dc level of the base voltage (V_B) can be set lower than V_{CC}. This arrangement is quite common in oscillators using bipolar transistors to avoid clipping the output swing. However, depending on the presence of a significant capacitance (C_{tail}) at the common emitter node of Q_1 and Q_2, the oscillator operates in class-C or class-B [59]. Class-C operation results in a better conversion of the bias current into the first harmonic of the tank current, leading to a higher oscillator efficiency, that is the same level of phase noise can be achieved with a lower power consumption.

Another oscillator topology that is commonly used, especially in the implementation of bipolar oscillators at higher frequencies ($>$10 GHz), is the Colpitts oscillator (see e.g. [60]). A schematic of the Colpitts oscillator is depicted in Fig. 3.7.

A comparison between the Colpitts and the class-B differential LC oscillator is carried out in [61], while in [59], a comparison between class-B and class-C operation is discussed. The comparison is performed for a given tank impedance, and bias current, with the assumption the oscillator is in the current-limited regime. However, it is interesting to extend the discussion to the case where the amplitude of oscillation is maximized to yield minimum phase noise, regardless of the current efficiency. In other terms, the question is which of the aforementioned topologies allows to maximize V_0 and reach the minimum phase noise for a given tank impedance, frequency of oscillation, and supply voltage. We will see that the class-C differential LC oscillator is preferable over both the class-B and Colpitts topologies.

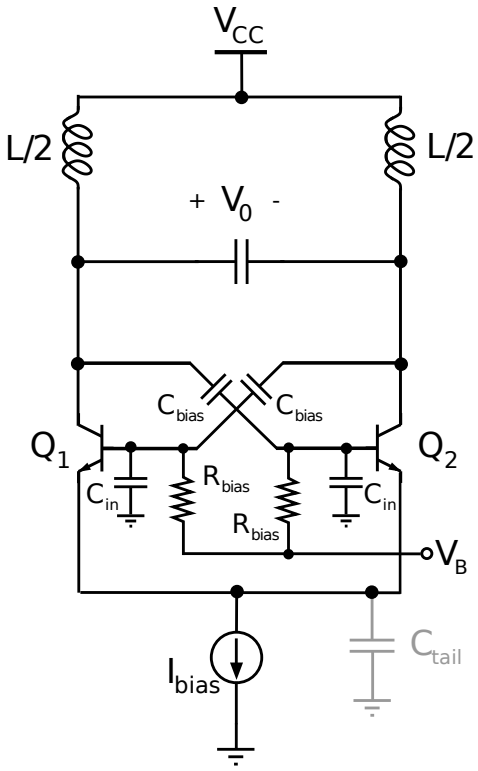

Fig. 3.6 Schematic of differential LC oscillator (class-C or class-B operation is obtained whether a large C_{tail} is present or not).

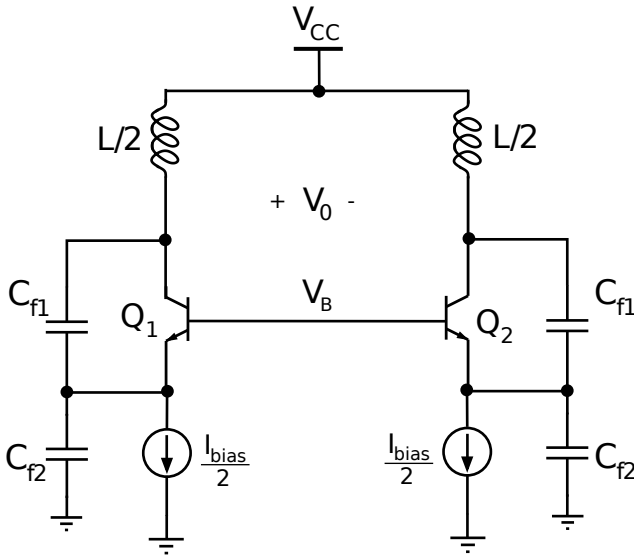

Fig. 3.7 Schematic of differential Colpitts oscillator.

Apart from the issues related to the use of the varactor described in Section 3.2.1, the amplitude of oscillation is limited by the onset of the saturation in the bipolar transistors sustaining the oscillations. In the differential LC oscillator (see Fig. 3.6(a)), in order to avoid the saturation regime, the base-collector voltage cannot exceed a certain limit value $V_{bc,\max}$:

$$V_{bc}(t) = V_B - V_{CC} + \frac{V_0}{2}(1+n)\cos(\omega_0 t) \leq V_{bc,\max} \tag{3.2}$$

where

$$n = \frac{C_{\text{bias}}}{C_{\text{bias}} + C_{\text{in}}} \tag{3.3}$$

and C_{in} is the input capacitance of Q_1 and Q_2. As a consequence, the maximum amplitude of oscillation is:

$$V_{0,\max} = \frac{2V_{\text{lim}}}{1+n} \tag{3.4}$$

where $V_{\text{lim}} = V_{CC} - V_B + V_{bc,\max}$. Substituting (3.4) in (3.1), using the results in [59, 61, 62], and taking into account (for the moment) only the tank losses and the collector shot noise current of Q_1 and Q_2, we recast (3.1) as

$$\mathscr{L}(\Delta\omega) = 10\log_{10}\left[\frac{kTR_T(1+n)^2}{(2V_{\text{lim}})^2}\left(1+\frac{1}{2n}\right)\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{3.5}$$

Clearly, (3.5) shows there is an optimum value of n that minimizes the phase noise. By differentiation, such a value is found to be:

$$n_{\text{opt}} = \frac{\sqrt{17}-1}{8} \approx 0.39. \tag{3.6}$$

It must be noted that there is a small variation in (3.5) if n ranges in the 0.3 to 0.6 span.

The foregoing discussion applies both to class-B and class-C operation. However, since the average base-emitter voltage of Q_1 and Q_2 is much smaller in class-C as compared to class-B operation, the maximum attainable value of V_{lim} is larger for class-C operation. In other words, with the dynamic biasing scheme detailed in Section 3.3.2, V_B can be set to a lower value in a class-C oscillator as compared to a class-B oscillator. Therefore, the minimum phase noise achievable with the class-C oscillator is lower than the one achievable with the class-B oscillator.

Simulations have been carried out to verify this result. To have full control of the simulation parameters, simple ideal models of the bipolar transistors have been used, along with an ideal noiseless tail current source. The inductor ($L = 150\,\text{pH}$) is the only lossy element in the tank, with $Q = 20$ at 20 GHz. The oscillation frequency is 20.4 GHz. The

Table 3.1 Simulated phase noise for class-B and class-C differential LC oscillators and Colpitts oscillator.

	V_{CC} [V]	V_0 [V]	I_{bias} [mA]	n	$\mathscr{L}(1\,\text{MHz})$ [dBc/Hz]
class-B	3.3	3	11.0	0.4	-122.6
class-C	3.3	4	10.5	0.4	-125.2
Colpitts	3.3	4	16.0	0.3	-125.6
class-B	5	5.5	22.5	0.4	-128.5
class-C	5	7	18.5	0.4	-130.1
Colpitts	5	7	29.0	0.3	-130.4

simulations are performed with two different values of supply voltage, namely 3.3 and 5 V. The amplitude of oscillation is maximized, with the constraint that $V_{bc,\max} = 0\,\text{V}$, while leaving a 0.5 V headroom for the tail current generator. The results, reported in Table 3.1, show that indeed class-C operation is both more efficient in terms of current consumption as compared to class-B operation, and also allows for larger amplitudes of oscillations, yielding lower phase noise.

In the case of the Colpitts oscillator (see Fig. 3.6(b)), the maximum oscillation amplitude is

$$V_{0,\max} = 2V_{\text{lim}}. \tag{3.7}$$

Correspondingly, combining (3.7) with the results in [61], the phase noise can be written:

$$\mathscr{L}(\Delta\omega) = 10\log_{10}\left[\frac{kTR_T}{(2V_{\text{lim}})^2}\left(1+\frac{1-n}{2n}\right)\left(\frac{\omega_0}{Q\Delta\omega}\right)^2\right] \tag{3.8}$$

where

$$n = \frac{C_{f1}}{C_{f1}+C_{f2}}. \tag{3.9}$$

For a given value of V_{lim}, the phase noise of the Colpitts oscillator decreases increasing n, at the cost of a larger bias current [61]:

$$I_{\text{bias}} \approx \frac{V_0}{R_T(1-n)}. \tag{3.10}$$

It must be noted that, despite the Colpitts oscillator operates itself in class-C regime, V_B cannot be set as low as in the class-C differential LC oscillator. Therefore, the maximum attainable value of V_{lim} is larger in the class-C differential LC oscillator than in the Colpitts oscillator, i.e.:

$$V_{\text{lim, diff. LC}} \geq V_{\text{lim, Colpitts}} \tag{3.11}$$

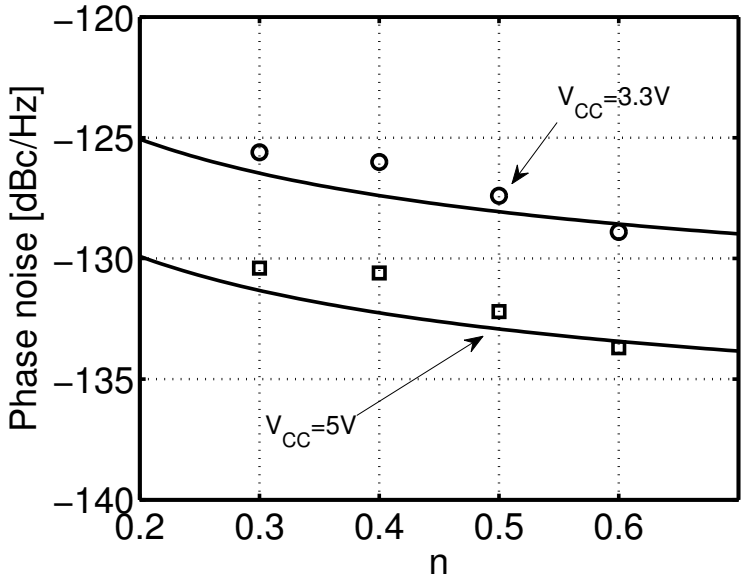

Fig. 3.8 Simulated (circles) and calculated (solid line) phase noise at 1 MHz offset from the carrier for Colpitts oscillator.

This is because, in the Colpitts oscillator, the voltage at the emitters of Q_1 and Q_2 has a significant ac component. Hence the minimum emitter voltage (as opposed to the average emitter voltage) must be large enough to leave an adequate voltage headroom to the current sources. Consequently, the maximum amplitude of oscillation achievable in the class-C differential LC oscillator and in the Colpitts oscillator is similar (see (3.4), (3.7), and (3.11)):

$$V_{0,\max,\text{diff.LC}} \approx V_{0,\max,\text{Colpitts}} \tag{3.12}$$

This is confirmed by the simulation results reported in Table 3.1, obtained in the same conditions as previously described for the differential LC oscillators. The results in Table 3.1 refer, in the case of the Colpitts oscillator, to $n = 0.3$, which corresponds to the best trade-off between current efficiency and phase noise [61]. As shown in Fig. 3.8, a marginal improvement of the phase noise is achievable in the Colpitts oscillator at larger values of n for a fixed amplitude of oscillation, although the increase in the current consumption, as predicted by (3.10), is substantial.

In summary, in bipolar differential LC oscillators, class-C operation results in an improved performance as compared to class-B biasing, both in terms of current efficiency and lower phase noise, allowing to obtain larger amplitudes of oscillation for a given supply voltage. The Colpitts oscillator shows a comparable performance to the class-C differential LC oscillator in terms of phase noise if the feedback factor n is set for the optimal phase noise

versus current consumption trade-off. Even in this case, however, the current efficiency of the class-C differential LC oscillator is superior. Increasing n, the Colpitts oscillator allows to further decrease the phase noise for a given supply voltage, but at the cost of a higher power consumption and lower efficiency. The class-C differential LC oscillator substantially achieves the same phase noise performance of the Colpitts oscillator, but at a remarkably lower power consumption. Hence, in the following, class-C differential LC oscillators are proposed to achieve low levels of phase noise, and, simultaneously, good current efficiency.

Finally, other sources of noise, neglected so far, can be very significant and even dominant, as pointed out in [61–63]. Class-C biasing, leveraging the presence of a capacitance at the output node of the tail current source, has a strong advantage compared to class-B operation, and to the Colpitts oscillator, in that the tail capacitance is very effective at filtering out the noise from the bias circuitry. Simulations of the designs reported in Section 3.3 show that the relative contribution to the phase noise of the tail current source is reduced to an almost negligible $< 5\%$ in class-C oscillators, while in class-B operation it can be one of the primary sources of phase noise [62, 63]. Similar to the class-B case, in the Colpitts oscillator, the tail current source can significantly contribute to the overall phase noise, especially for larger values of n [63]. The base resistance is another important source of noise in bipolar technologies. Its relative impact is proportional to the bias current [61], suggesting an edge of the highly current-efficient class-C differential LC oscillator as compared to the other topologies.

3.3 K-Band SiGe VCO Design

Two K-band VCOs have been designed in a pure SiGe bipolar process implementing the concepts illustrated in Section 3.2. First, the use of a transformer-coupled varactor is explored. This design uses transistors with higher breakdown voltage in an attempt of increasing the oscillation amplitude, and decreasing the phase noise, by increasing the supply voltage. Next, the robustness of the topology using the transformer-coupled varactor with respect to start-up is assessed. A feedback loop is used to control the base voltage of the cross-coupled transistors and guarantee the oscillator start-up. The design of the control loop, and its impact on the phase noise performance are discussed in detail.

The designed VCOs are loaded by a differential test buffer made of a resistively-degenerated cascode amplifier with resistive load. The buffer is required to directly drive the $50\,\Omega$ measurement setup.

3.3.1 VCO with transformer-coupled varactor

The schematic of the proposed K-band VCO with transformed-coupled varactor and higher breakdown voltage transistors (VCO-XCV) is shown in Fig. 3.9. The use of the transformer allows to set the dc value of the anode voltage to ground. As a consequence, the complete tuning range is obtained while keeping $V_{\text{tune}} \leq V_{\text{CC}}$. The transformer turn ratio ($N = 1.3 : 1$) is chosen such that the swing across the varactor is reduced as compared to the output swing of the VCO, further limiting the possibility that the junction turns on for larger amplitudes of oscillation. The transformer is characterized by means of 2.5-D electro-magnetic simulations, from which a compact model is extracted to run transistor-level simulations, in a similar fashion as in [54]. An essential point to adopt the transformer-coupled varactor configuration is making sure that the use of a transformer does not impair the quality factor of the inductive element, ultimately degrading the overall tank Q. To this goal, the layout of the transformer is essential. The transformer layout is sketched in Fig. 3.10. It is made of two single-turn coils. The primary inductor, connected to the oscillator output nodes, is the outer coil. Its inductance is $L_1 = 180\,\text{pH}$. It is made of a sandwich of the two top metal layers to lower the series resistance. Moreover, the one but the top layer has been extended in the area under the secondary coil, as illustrated in the cross-section view in Fig. 3.10. As a consequence, we have a combination of a vertical and a planar transformer, resulting in a relatively large magnetic coupling factor ($k \approx 0.6$ in simulation). The secondary coil ($L_2 = 105\,\text{pH}$) is connected to the varactor. It is realized with the top metal layer. An oscillator with a transformer-based resonator has two possible modes of oscillation [64, 65]. Since this is an undesired feature for this design, the possibility of exciting a higher frequency

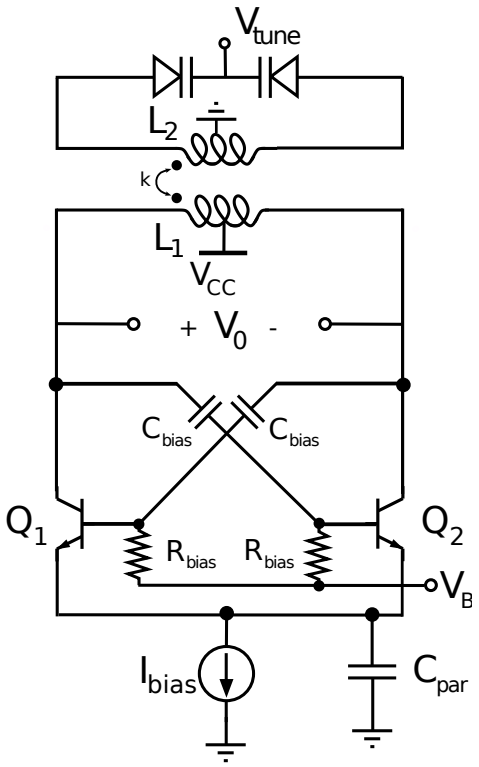

Fig. 3.9 Schematic of the VCO with transformer-coupled varactor.

mode of oscillation is largely suppressed by having a quite large k [64]. The frequency of oscillation can be expressed as [64]:

$$\begin{aligned}\omega_0 &= \sqrt{\frac{1+\xi-\sqrt{(1+\xi)^2-4\xi(1-k^2)}}{2(1-k^2)}}\cdot\omega_2 \\ &= \Omega_0(\xi,k)\cdot\omega_2\end{aligned} \tag{3.13}$$

where $\omega_1^2=(L_1C_1)^{-1}$, $\omega_2^2=(L_2C_2)^{-1}$, $\xi=(\omega_1/\omega_2)^2$, and C_1 is the total (parasitic) capacitance connected to the primary terminals, while C_2 is the total capacitance connected to the secondary terminals, i.e. the varactor capacitance (plus the parasitics). The frequency sensitivity to variations in the varactor capacitance is calculated as:

$$\frac{\partial\omega_0}{\partial C_2}=\frac{\partial\omega_2}{\partial C_2}\cdot\left(\Omega_0-2\xi\frac{\partial\Omega_0}{\partial\xi}\right) \tag{3.14}$$

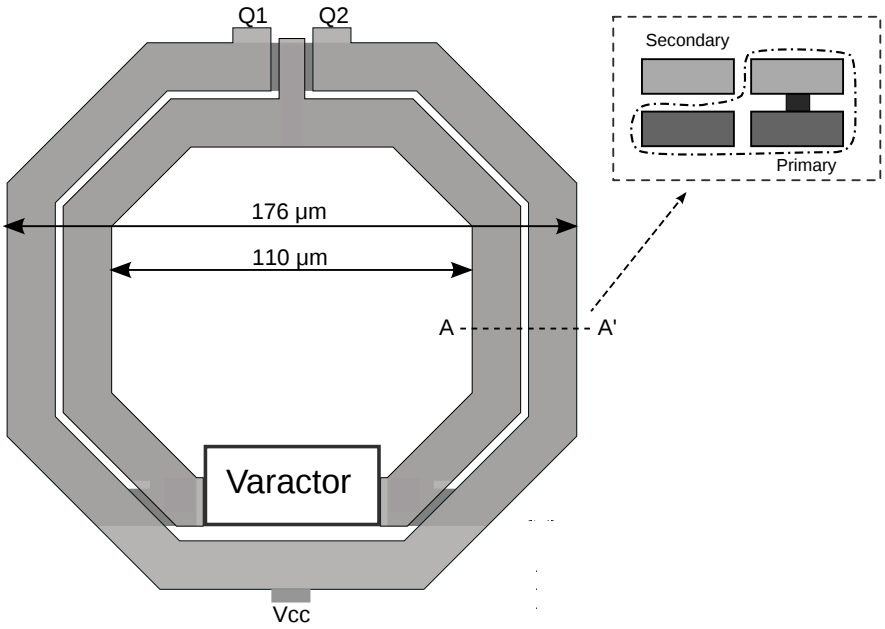

Fig. 3.10 Transformer layout.

With the parameters of our design ($\xi \approx 2$, $k \approx 0.63$, thus $\Omega_0 \approx 0.89$), the term within parenthesis in (3.14) evaluates almost unity, such that (3.14) can be approximated as:

$$\frac{\partial \omega_0}{\partial C_2} \approx \frac{\partial \omega_2}{\partial C_2} \tag{3.15}$$

Hence, at the design level, there is not any particular issue in sizing the varactor in the transformer-coupled arrangement, as compared to the direct coupling case. The active devices are arranged in a classic cross-coupled pair configuration; class-C biasing is used. The value of the coupling capacitance is set to $C_{\text{bias}} = 320\,\text{fF}$ such that n is in the optimal range from 0.3 to 0.6, as discussed in Section 3.2.2, while $R_{\text{bias}} = 10\,\text{k}\Omega$, such that $1/(R_{\text{bias}}C_{\text{bias}}) \ll \omega_0$. Since lower phase noise is achieved for larger amplitudes of oscillation, in this design devices with higher breakdown voltage ($f_T = 35\,\text{GHz}$) are used [66]. Such devices feature larger emitter area and hence have larger capacitive parasitics, but allow the oscillator to be operated at a higher (5 V) supply voltage as compared to the standard 3.3 V supply. Combined with an increase of the bias current, the use of a higher supply voltage allows to achieve a larger V_0, as discussed in Section 3.2.2, and hence lower phase noise.

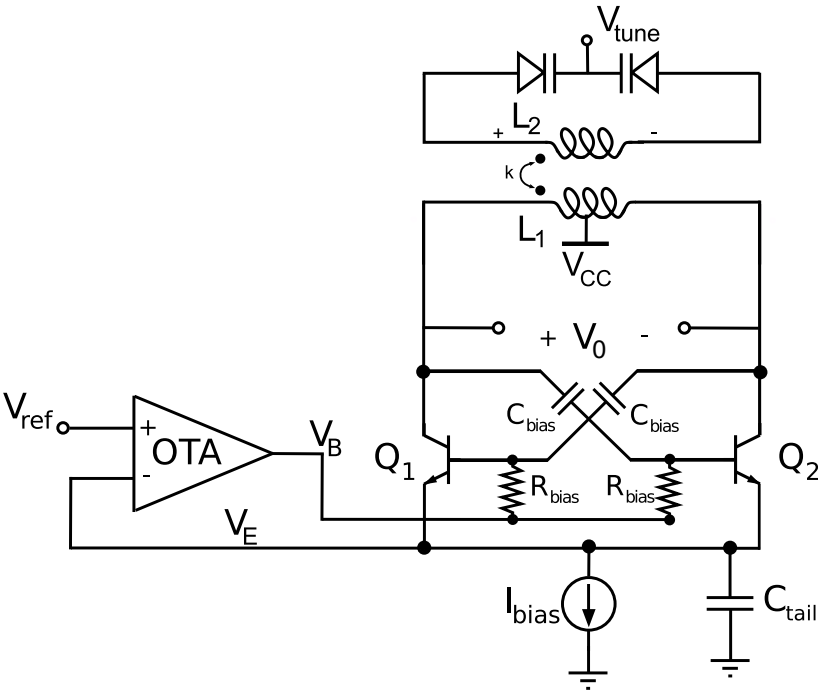

Fig. 3.11 Schematic of the VCO with transformer-coupled varactor and dynamic biasing.

3.3.2 VCO with transformer-coupled varactor and dynamic biasing

In class-C oscillators, the desired steady state average value of the base voltage of the cross-coupled devices (V_B in Fig. 3.9) may be too low to ensure robust start-up of the oscillations, especially in presence of PVT variations. A control loop is therefore explored to dynamically bias the oscillator. The employed biasing scheme was originally proposed in [67, 68] for a CMOS technology. Its use is here extended to a pure bipolar technology.

The schematic of the VCO with transformed-coupled varactor and dynamic biasing (VCO-XDB) is depicted in Fig. 3.11. The LC tank is the same as in the design described in Section 3.3.1. Unlike the design proposed in Section 3.3.1, regular breakdown devices [66] have been used here; the oscillator is supplied by the standard 3.3 V voltage.

The biasing control loop regulates the dc voltage (V_E) of the common emitter node between Q_1 and Q_2 to a reference voltage $V_{\text{ref}} = 0.5\,\text{V}$. This guarantees the start-up of oscillations as follows. If oscillations do not start, Q_1 and Q_2 are off, and V_E will drop to ground. Therefore, the control loop reacts raising V_B, hence starting up the oscillations. As the oscillations build up (the oscillator operating in class-B during this initial transient), Q_1 and Q_2 act as (large signal) emitter followers with respect to V_B, C_{tail} integrating the ac common-mode current through Q_1 and Q_2. Hence, V_E follows the increase in V_B. The negative feedback loop then reacts by decreasing V_B (and V_E), settling V_E to its steady-state

value. The simulated transient voltage waveforms are shown in Fig. 3.12. The initial increase of V_B and V_E takes place very quickly. The increase in V_E forces the OTA used in the control loop to slewing condition, which determines the settling time. Note that in steady state the average base-emitter voltage of the cross-coupled transistors Q_1 and Q_2 is negative, underlining the operation of the oscillator is deeply in class-C.

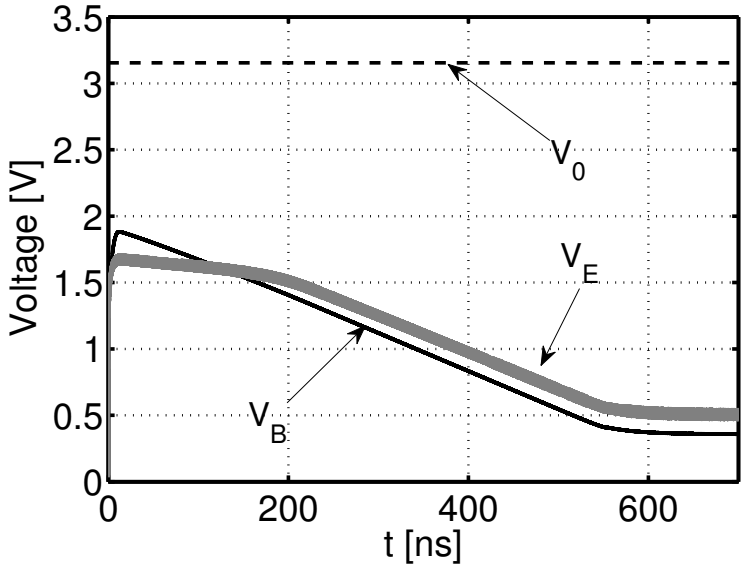

Fig. 3.12 Simulated transient voltage waveforms in the VCO with the dynamic biasing control loop.

The schematic of the OTA used in the control loop is shown in Fig. 3.13. The amplifier is a two-stage design with Miller compensation (compensation capacitance is $C_{\text{Miller}} = 5\,\text{pF}$). The dominant pole is set at low frequency, at about 1.8 kHz, to ensure the loop stability. The loop stability is mainly endangered by the pole due to the R_{bias}-C_{bias} network (R_{bias} is here decreased to 3 kΩ), and the relatively large intrinsic gain of the bipolar transistors. In addition, the OTA must be able to provide the base bias current to the cross-coupled transistors in the oscillator. Thus, the bias current of the OTA cannot be decreased to keep the unity gain frequency of the amplifier low, and guarantee stability[2]. Taking all these constraints into account, the two-stage design is chosen, as it gives quite some design flexibility. In contrast, a single-stage OTA would have required a much larger compensation capacitance. The OTA draws 220 μA from the 3.3 V supply.

[2] The current the OTA must source is $I_{\text{bias}}/(1+\beta_F) = 20\,\mu\text{A}$, β_F being the dc current gain of the transistors.

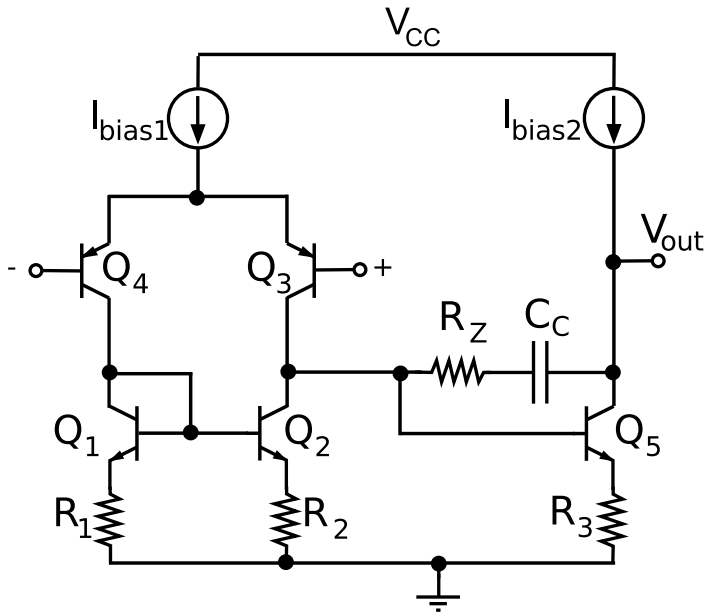

Fig. 3.13 Schematic of the OTA used in the dynamic biasing control loop.

3.4 Measurement Results

The designed VCOs have been implemented in the Infineon SiGe bipolar technology [66] with a nominal 3.3 V supply voltage. The microphotographs of the fabricated prototypes of VCO-XCV, and VCO-XDB are shown in Figs. 3.14 (a), and 3.14 (b), respectively.

The active area occupied by all VCO cores is roughly the same, $200 \times 240\,\mu\text{m}^2$. The OTA used in VCO-XDB occupies an additional area of $170 \times 170\,\mu\text{m}^2$, mainly due to the relatively large C_{Miller}. All the prototypes have been assembled and directly wire-bonded on connectorized PCBs in a chip-on-board fashion for testing. The VCO employing the transformer-coupled varactor (VCO-XCV) is biased with a current of $I_{\text{bias}} = 7\,\text{mA}$ when supplied with 3.3 V. The bias current is then increased to $I_{\text{bias}} = 10\,\text{mA}$ to take advantage of the additional voltage headroom when the supply voltage is raised to 5 V. The measured and simulated frequency of oscillation of VCO-XCV is reported in Fig. 3.15 for both values of the supply voltage. The measured frequency of oscillation of VCO-XCV spans from 18.7 to 21.2 GHz when $V_{CC} = 3.3\,\text{V}$, and from 18.6 to 21.2 GHz when $V_{CC} = 5\,\text{V}$[3]. Due to the transformer-coupled arrangement, the tuning characteristic is basically independent on the dc value of the supply voltage. As discussed in Section 3.3.1, this design makes use of transistors with higher breakdown voltage. Such devices feature larger emitter area, and thus larger capacitive parasitics. Due to overestimated parasitics, the frequency range is slightly higher than the simulated one (compare simulations and measurements in Fig. 3.15). The

[3] $V_{\text{tune}} \leq 3.3\,\text{V}$ even with $V_{CC} = 5\,\text{V}$.

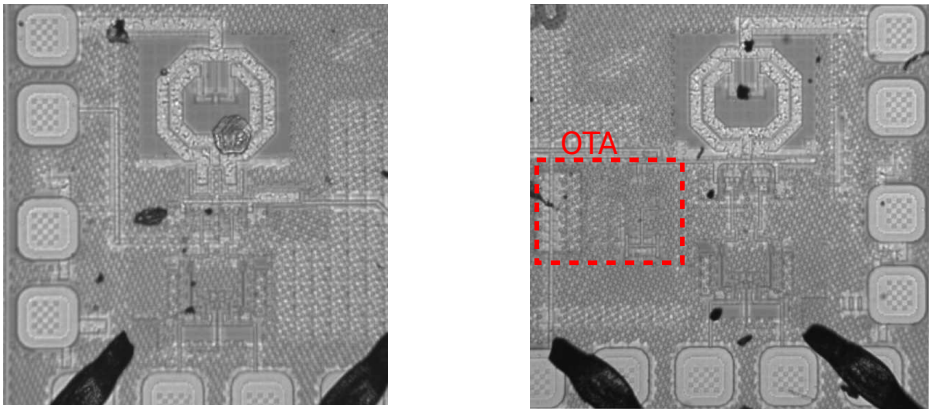

Fig. 3.14 Chip micrographa: (a) VCO-XCV and (b) VCO-XDB.

measured tuning range is TR=13.0%. The measured phase noise spectrum of VCO-XCV is reported in Fig. 3.16 for three carrier frequencies: 18.7, 19.7, and 21.2 GHz when the oscillator is supplied with 3.3 V. The $1/f^3$ corner frequency is at a 150 kHz offset from the carrier. The use of the transformer coupling and the consequent decrease of the voltage swing across the varactor help mitigate the phase noise degradation at lower frequencies (i.e., when the dc bias across the varactors is 0 V).

The impact of raising the supply voltage (and consequently the bias current) on the phase noise performance is clear in Fig. 3.17, where the measured phase noise at 10 MHz offset from the carrier is reported for VCO-XCV. At larger V_{tune} values, the larger oscillation amplitude obtained at $V_{CC} = 5$ V results in a lower phase noise, as one may expect from (3.1). However, at lower V_{tune} values, the same increase in V_0 means a larger swing across the varactor, and a consequent stronger degradation of the tank quality factor, and thus of the phase noise performance. This suggests that operation at $V_{CC} = 5$ V calls for a scaling of the transformer turn ratio to further decrease the voltage swing across the varactor.

The VCO with dynamic biasing features the same tank as the VCO-XCV, but regular high-speed devices with an f_T of 180 GHz. The latter have a smaller emitter area compared to the transistors used in VCO-XCV, and thus smaller parasitic capacitance. VCO-XDB is hence designed to operate at higher frequencies, therefore requiring a slightly reduced bias current ($I_{\text{bias}} = 5.5$ mA). The decreased amount of parasitics is also beneficial for the tuning range. The measured and simulated frequency of oscillation for VCO-XDB is reported in Fig. 3.18. A very good match between measurements and simulations is observed. The tuning range spans from 20.4 to 24.2 GHz, i.e. a relatively wide TR=17%.

The measured phase noise spectrum of VCO-XDB is reported in Fig. 3.19 for three carrier frequencies: 20.4, 23.0, and 24.2 GHz. The $1/f^3$ corner frequency is at a 200 kHz

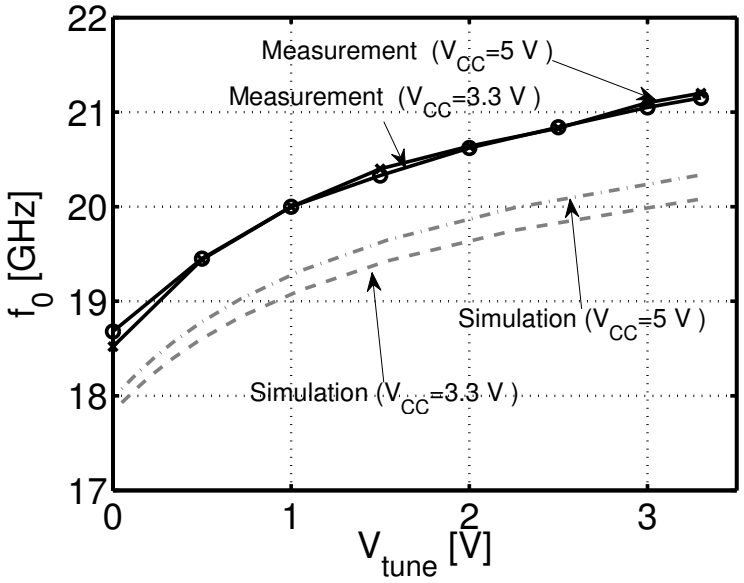

Fig. 3.15 Measured (solid line) and simulated (dashed line) oscillation frequency versus tuning voltage for VCO-XCV.

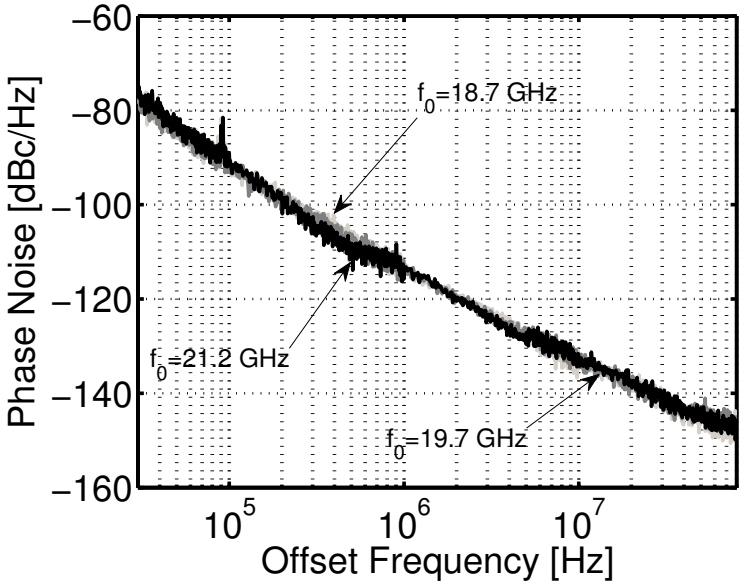

Fig. 3.16 Measured phase noise spectra at 18.7, 19.7, and 20.4 GHz carrier frequency for VCO-XCV ($V_{CC} = 3.3\,\mathrm{V}$).

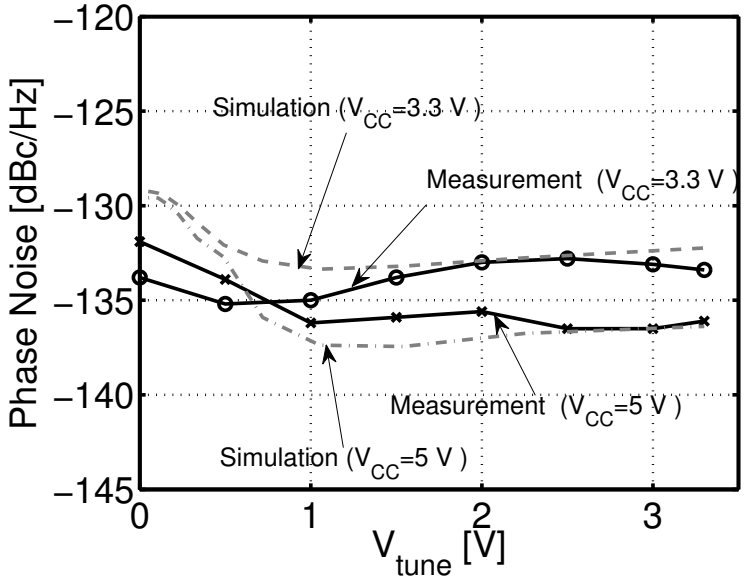

Fig. 3.17 Measured (solid line) and simulated (dashed line) phase noise at 10 MHz frequency offset from the carrier versus tuning voltage for VCO-XCV for $V_{CC} = 3.3\,\mathrm{V}$ and $V_{CC} = 5\,\mathrm{V}$.

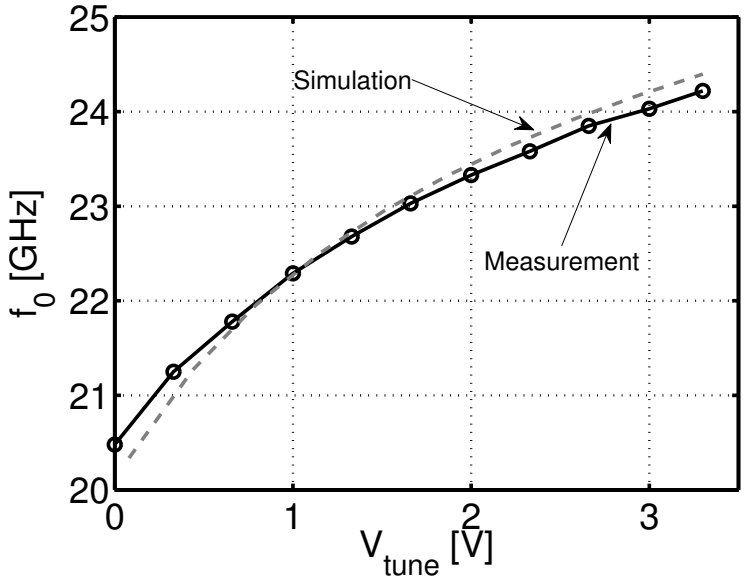

Fig. 3.18 Measured (solid line) and simulated (dashed line) oscillation frequency versus tuning voltage for VCO-XDB.

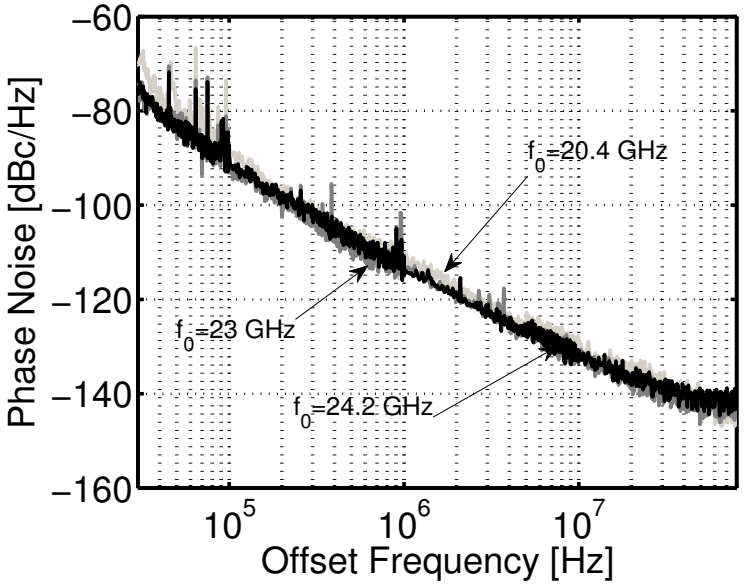

Fig. 3.19 Measured phase noise spectra at 20.4, 23.0, and 24.2 GHz carrier frequency for VCO-XDB.

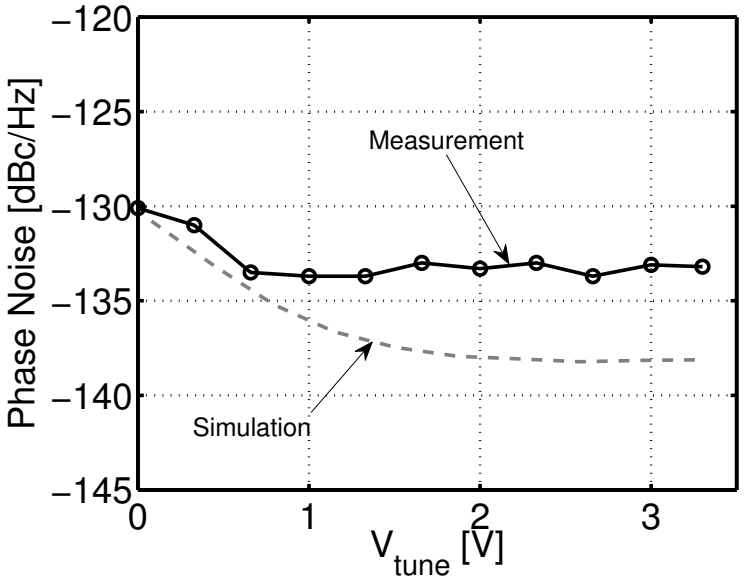

Fig. 3.20 Measured (solid line) and simulated (dashed line) phase noise at 10 MHz frequency offset from the carrier versus tuning voltage for VCO-XDB.

offset from the carrier. In Fig. 3.20, the measured phase noise at at 10 MHz offset from the carrier is reported for VCO-XDB. The results are similar to those reported for the VCO-XCV operated at $V_{CC} = 3.3$ V, suggesting that the dynamic biasing loop does not degrade the phase noise performance.

Phase noise measurements have been carried out on VCO-XCV and VCO-XDB at different temperatures (25, 60, 85, and 100°C) to further verify the robustness of the use of the transformer-coupled varactor, class-C biasing and dynamic biasing circuitry. The measurement results are reported in Figs. 3.21, and 3.22 for VCO-XCV, and VCO-XDB, respectively. We observe a degradation of about 3 dB at 100°C as compared to ambient temperature.

	Tech.	f_0 [GHz]	TR [%]	V_{CC} [V]	$\mathscr{L}$(1 MHz) [dBc/Hz]	P_{dc} [mW]	FOM [dBc/Hz]	FOM_T [dBc/Hz]
[69]	Si bipolar	18.5	23	3	-109	36	-179	-186
[27]	SiGe HBT	33	3	2.5	-99	2.6	-184	-174
[55]	SiGe HBT	43	26	4	-91	392	-158	-166
[70]	SiGe HBT	81	30	5	-109†	240	-171	-180
[60]	SiGe:C BiCMOS	38.4	9.7	3.3	-107	105.6	-180	-180
[56]	InGaP/GaAs HBT	16.3	53	3	-102	45	-170	-184
[71]	InGaP/GaAs HBT	25.7	2	9	-130	90	-195	-179
[72]	InGaP/GaAs HBT	17.9	2	3	-110	13	-184	-165
[58]	InGaP/GaAs HBT	23	13	5	-115	1000	-172	-174
[73]	0.18 μm CMOS	20	2	1.8	-111	32	-182	-170
[74]	0.18 μm CMOS	21.4	5	0.6	-110	3.5	-191	-185
[75]	0.18 μm CMOS	18.9	4	1.3	-111	3.3	-191	-182
[57]	SiGe HBT	22.1	16	3.3	-116	33	-188	-192
This work VCO-XCV	SiGe HBT	20/21	13/13	3.3/5	-115/-117	23/50	-187/-186	-189/-188
This work VCO-XDB	SiGe HBT	22.7	17	3.3	-114	18	-189	-193

†Referred to $f_0/4$.

Table 3.2 Measured performance of the designed oscillator compared to state-of-the-art K-band VCOs.

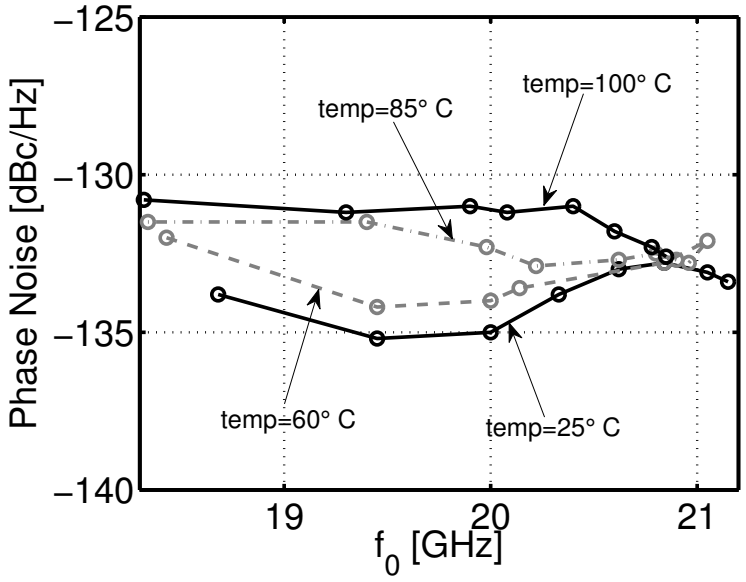

Fig. 3.21 Measured phase noise at 10 MHz frequency offset from the carrier across temperature for VCO-XCV for $V_{CC} = 3.3$ V.

A thorough comparison of the performance of the designed VCOs with respect to state-of-the-art oscillators operating in the *K*-band is shown in Table 3.2. The VCOs reported in this work compare very well with the other oscillators, be they implemented in silicon or SiGe bipolars, composite semiconductors, or CMOS technology. In particular, a previous design in the same technology as the VCOs proposed in this work shows a similar performance [57]. However, it must be noted that a standard LC tank is used in [57], resulting in tuning voltages as large as 8 V. The transformer-coupled varactor addresses this issue in this work. The phase noise performance of the VCO-XCV is outperformed only by the work in [71]. Besides taking advantage of the superior characteristics of the InGaP/GaAs HBT devices, the VCO in [71] displays a tiny tuning range, which may further explain its exceptional phase noise performance.

In terms of figure-of-merit (FOM)

$$FOM = \mathscr{L}(f_{\text{off}}) - 10\log_{10}\left[\frac{1}{P_{\text{DC}}}\left(\frac{f_0}{f_{\text{off}}}\right)^2\right], \tag{3.16}$$

where P_{DC} is the oscillator power consumption normalized to 1 mW, f_0 is the oscillation frequency, $\mathscr{L}(f_{\text{off}})$ is the phase noise, and f_{off} is the offset from the carrier, the proposed VCOs compare well with the state-of-the-art. To this regard, the CMOS implementations [74, 75] seem to take advantage of the much reduced supply voltage compared to the bipolar technolo-

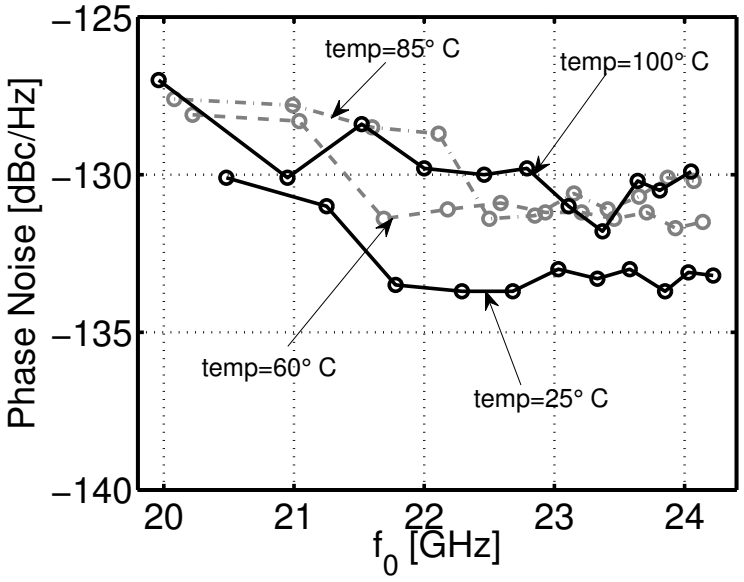

Fig. 3.22 Measured phase noise at 10 MHz frequency offset from the carrier across temperature for VCO-XDB.

gies. Note that VCO-XDB shows a better FOM compared to the other proposed VCO, due to the lower power consumption. Finally, in terms of power-frequency-tuning-normalized figure-of-merit, $FOM_T = FOM - 10\log_{10}[(\mathrm{TR}/10\%)^2]$, the VCO with the dynamic biasing shows a $FOM_T = -193$ dBc/Hz: This result outperforms the state-of-the-art.

3.5 Conclusions

This chapter presents an optimization of the phase noise performance of SiGe bipolar VCOs tailored for operation in the K-band. A thorough theoretical investigation formulates the ultimate lower limit of the achievable phase noise for a given tank quality factor, and supply voltage. The specific challenges related to the use of a pure bipolar technology are discussed. Coupling the varactor diodes to the oscillator tank by means of a magnetic transformer is shown to concurrently solve many of them. The proposed approach allows to keep the tuning voltage below the supply voltage, and to reduce the swing across the varactor. Two VCOs are implemented, that consistently show state-of-the-art phase noise and figure-of-merit.

Chapter 4

Conclusion

In this thesis some integrated building blocks for phased array systems are presented. The work is divided into three parts, first part gives an introduction to phased array system, second part concerns the design of variable gain amplifiers whit low phase error and third part provides a discussion on the minimization of phase noise performance in integrated voltage controlled oscillators with some design realizations.

Brief description of the phase array antenna functioning is presented in Chapter 1 with an overview of the main applications ad developments such as military and automotive radars, satellite communications, point-to-point wireless link and base station. Devices with more than 300 GHz of f_T operate well in the range of millimeter wave and sub-millimeter wave frequencies, (i.e. $f > 10$ GHz) then, transceiver system can transmit/receive several Gb/s. Air attenuation at these frequencies becomes a crucial parameter hence phased array systems help to increase the directivity of the transmitted signal hence reduce the constrains of the PA, increase the efficiency of the system and increase the resilience to the interfeers. Moreover, since the wavelength is in the order of some millimeter, the possibility to integrate a larger number of channels will decrease the complexity and costs of the system. Integrated building blocks have certainly less performances than discrete ones, in this work we analyzed the silicon technology limitations and we focus on how it is possible to achieve performances as close as possible to the discrete or higher technology costs implementations.
The issues of the phase error caused by non ideal behavior of the phased array building blocks is treated in Chapter 1. Phase error between the radiating elements of the antenna array causes reduction of spatial efficiency and possible beam pointing error.
Second part of the thesis focuses on the design of variable gain amplifiers for phased array systems. In particular we analyzed the phase behavior of the VGAs in order to understand the mechanisms that generate phase error. The aim is to realize an ideal building block, i.e. the phase of the signal must not vary when the gain is varied. Some new solution to

compensate the phase error are presented and four VGAs for X-band and K-band applications have been prototyped. The results in terms of phase error versus gain variations outperform the sate-of-the-art if compared with the other works in the same frequency bands.
The best results achieved is a phase variation of less than 2° for a linear-in-dB gain variation of 22 dB. VGA works in the frequency range from 10 to 14.4 GHz, the maximum gain is 13 dB and the power consumption is 83 mW. Input referred intercept point is -3 dBm and the minimum noise figure is 5.1 dB. The robustness of the phase compensation circuits is verified with some measurements at high temperature, the results illustrate that the phase error is well compensated also at 85°.
A Wide band VGA has been realized with the same compensation techniques reported for the X-band VGA, it operates from 15.5 to 39.5 GHz (possible allocation of frequencies for 5G standars) and the results show that the compensations are functional also in this wide frequency range.

In the third part of the thesis a discussion of the phase noise minimization for voltage controlled oscillators operating in K band is presented. A comparison between Colpitts and differential cross coupled pair VCO is described and the theoretical limit in terms of minimum phase noise achievable is calculated fro both the topologies. Two SiGe VCOs in K band have been prototyped, one is operating from 18.7 to 21.2 GHz, the phase noise is -115 dBc/Hz at 1 MHz from the carrier $f_c = 20$ GHz. Second VCO features a dynamic biasing that ensure robust start-up, it operates from 20.4 to 24.2 GHz and the phase noise measured at 1 MHz offset from the carrier $f_c = 22.7$ GHz is -114 dBc/Hz. The figure FOM (FOM_T) is respectively -187 (-189) dBc/Hz and -189 (-193) dBc/Hz for the two VCOs.

To conclude, this work presents the design of state-of-the-art integrated building blocks for phased array systems. Solutions presented in the thesis will help to develop high performance phased array systems that will allow for example to download-upload several Gb/s with a smartphone or to recognize several obstacles in front of your car reducing the car accidents percentage. This systems will definitely improve the life quality of the people.

List of Publications

Conference

Padovan, F.; Tiebout, M.; Mertens, K.; Bevilacqua, A.; Neviani, A., "A SiGe bipolar VCO for backhaul *E*-band communication systems," in *ESSCIRC (ESSCIRC), 2012 Proceedings of the* , vol., no., pp.402-405, 17-21 Sept. 2012

Padovan, F.; Bevilacqua, A.; Neviani, A., "A 20 Mb/s, 2.76 pJ/b UWB impulse radio TX with 11.7 % efficiency in 130 nm CMOS," in *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th* , vol., no., pp.287-290, 22-26 Sept. 2014

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