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CICLO XXII

EFFECTS OF IONIZING RADIATION IN FLASH MEMORIES

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Sommario

Le memorie a semiconduttore che operano al livello del mare sono costantemente bombardate dalla radiazione ionizzante. Particelle alfa, emesse dai contaminanti radioattivi che sono inevitabilmente presenti nei materiali dei componenti e delle saldature, possono raggiungere le aree sensibili dei chip e generare cambiamenti indesiderati dello stato logico dei bit di memoria. Inoltre, una continua pioggia di neutroni causata dalle interazioni dei raggi cosmici con gli strati esterni dell'atmosfera costituisce una seria minaccia per il corretto funzionamento dell'elettronica in ambiente terrestre. L'elettronica che opera nello spazio deve funzionare in un ambiente ancora più critico dal punto di vista delle radiazioni ionizzanti, data la presenza massiccia di protoni, elettroni e ioni pesanti.

Le memorie Flash sono sensibili agli effetti di radiazione. Essendo componenti sfaccettati, con blocchi funzionali eterogenei, la loro risposta alle radiazioni ionizzanti è variegata e talvolta la sua interpretazione può risultare complessa. Le SRAM, dal canto loro, sono il benchmark più comune per valutare la sensibilità al soft error di una data generazione tecnologica CMOS, nonchè dispositivi presenti virtualmente in tutti i circuiti integrati, non da ultimo nel page buffer delle memorie Flash.

Questo lavoro di tesi contiene dei contributi originali nel campo degli effetti delle radiazioni sulle memorie Flash e SRAM. E' stato effettuato uno studio completo, sperimentale e teorico, di memorie Flash commerciali, usando raggi x, ioni pesanti e neutroni, per simulare sia l'ambiente spaziale che quello terrestre.

Per quanto riguarda gli effetti di dose totale, si studiano le diverse dosi di fallimento della matrice di celle Floating Gate, delle pompe di carica e del decoder di riga, irraggiando

selettivamente i vari blocchi funzionali del dispositivo, in contrasto con la metodologia più comune di esporre alla radiazione l'intero chip.

Nel Capitolo 3, dedicato agli effetti da evento singolo, si chiarisce il ruolo del page buffer nel determinare la sensibilità a ioni pesanti di una memoria NAND, studiando anche la dipendenza dei diversi tipi di errori (page buffer vs celle Floating Gate) dalle condizioni operative del dispositivo. Si propone quindi una 'sezione d'urto efficace' allo scopo di tenere conto di questi parametri.

Negli ultimi anni sono stati discussi gli effetti di annealing post-irraggiamento degli errori osservati nelle celle Floating Gate, ma, apparentemente, le spiegazioni fornite collidevano con le teorie di perdita di carica dal Floating Gate. In questo lavoro di tesi si presentano risultati nuovi su questo fronte (Capitolo 4), che dimostrano come le teorie di perdita e intrappolamento di carica nel Floating Gate possano in realtà coesistere e spiegare in modo efficace i dati sperimentali.

Il Capitolo 5 mostra, per la prima volta, che i neutroni atmosferici sono in grado di indurre errori in memorie Flash avanzate, cosa che fino a poco fa si riteneva possibile solo per memorie SRAM e DRAM. Questi risultati rivelano l'importanza di una nuova tematica connessa all'uso questi dispositivi in ambito terrestre.

Infine, il Capitolo 6 illustra i fattori principali che determinano la dipendenza dalla temperatura del tasso di soft error in una memoria SRAM. Si presentano i risultati sperimentali, di simulazioni SPICE e modellizzazione analitica, per evidenziare la complessa miscela di parametri in gioco, molti dei quali fortemente dipendenti dalle caratteristiche tecnologiche del dispositivo.

Abstract

Semiconductor memories operating at sea level are constantly bombarded by ionizing radiation. Alpha particles, emitted by the radioactive contaminants that are inevitably present in the package and solder materials, may reach the sensitive areas of the chips and generate bit upsets. Furthermore, a shower of neutrons caused by interactions of cosmic rays with the external atmospheric layers can be a serious threat for the correct operation of electronics in the terrestrial environment. Satellite and spacecraft electronics must work reliably in an environment that is much harsher, because the huge presence of ionizing radiation, in particular protons, electrons, and heavy-ions, constantly threatens its correct behavior.

Flash memories are susceptible to radiation effects. They are multifaceted devices with a large number of miscellaneous building blocks, hence their response to ionizing radiation features different signatures, which may sometimes be very complex to interpret. SRAM memories, for their part, are the most common benchmark to evaluate the sensitivity to soft error of a given CMOS generation. In addition, they are present virtually everywhere in integrated circuits, for instance in the page buffer of Flash memories.

This thesis provides several original contributions to the field of radiation effects in Flash memories and SRAMs. A complete study, both experimental and modeling work, has been performed on Flash memories, using x-rays, heavy ions, and neutrons, to emulate both the space and terrestrial environments.

Concerning total ionizing dose results, the failure doses of the floating gate memory matrix, the charge pump circuitry, and the row decoder are assessed by selectively irradiating the device building blocks, in contrast to the common procedure of exposing the whole device.

As far as single event effects are concerned, the role of the page buffer is elucidated and the dependence of page buffer errors on the operating conditions (e.g., the read activity) during heavy-ion irradiation is clarified. An 'effective' device cross section is proposed that measures the device sensitivity, accounting for the main usage patterns.

During last years annealing effects in floating gate errors have been discussed several times after heavy-ion exposure, but apparently collided with observations on the floating gate charge loss. New results are presented in this work, which proves that the existing theories of charge loss and charge trapping can actually coexist.

This work shows for the first time that atmospheric neutrons are able to induce errors in advanced Flash memories, an effect that until a short time ago was believed to exist only in SRAMs and DRAMs. These results highlight new issues for the use of Flash in the terrestrial environment.

Finally, last section illustrates the main factors determining temperature dependence of the soft error in SRAMs. Experimental results, simulations, and analytical modeling are presented to show the complex mixture of parameters at play, most of them strongly dependent on the technological features of the devices.

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Preface

The purpose of this thesis is to study the two broad categories of radiation effects that may occur in Flash memories, total ionizing dose and single event effects, focusing both on the floating gate array and on the peripheral circuitry. In general, Chapters 2, 3, and 4 describe effects that are peculiar to the space environment, while the final chapters are mainly focused on neutron sensitivity, which is one of the most common concerns in the terrestrial environment. The last chapter presents some insights on how temperature can influence the neutron and alpha particle susceptibility of an SRAM cell.

In more detail, this thesis work is organized in the following way:

- Chapter 1 presents the state-of-the-art concerning radiation effects in Flash memories, including total ionizing dose and single event effects on both the floating gate array and the peripheral circuitry, with particular attention to post-radiation annealing phenomena and neutron effects. The final section of the chapter describes the state-of-the-art concerning the temperature dependence of soft error rate in SRAMs. For both Flash memories and SRAMs, the issues that are still open in the literature are presented, laying the basis for the results that will be presented in the following chapters.

- Chapter 2 is dedicated to total ionizing dose effects in a commercial, 90-nm NAND Flash memory. The sensitivity of the different device building blocks (floating gate array, charge pumps, and row decoder) is examined by performing selective x-ray irradiation and using dedicated test mode routines. The failure signature peculiar to each functional block is explored with the device operated in different conditions.

- Chapter 3 illustrates single event effects observed in NAND memories exposed to heavy ions. The features of upsets due to hits in the floating gate array and in the peripheral circuitry, especially in the page buffer, are discussed, together with functional interruptions leading to the failure of erase and program operations. To account for these phenomena, an effective heavy-ion cross section for a NAND memory is proposed, which takes into consideration the dependence on factors such as the program pattern and the operating conditions during irradiation.
- Chapter 4 presents experimental data and discussion on the post-radiation annealing of floating gate errors in Single Level Cell NAND and Multi Level Cell NOR memories, after both heavy-ion and total ionizing dose exposure. The underlying physics is investigated thanks to the use of test mode routines through which the threshold voltage of each memory cell can be followed after irradiation. The dependence on the program level, on the impinging particle linear energy transfer, as well as on the cell feature size are discussed.
- Chapter 5 shows for the first time that atmospheric neutrons can induce threshold voltage shifts, possibly leading to raw bit errors in Flash memories. A comparison between single- and multi level cell devices and between different technology nodes (down to 48 nm) demonstrates that the neutron cross section is increasing with decreasing feature size, even though significant differences are present in devices manufactured by different vendors. However, the neutron-induced bit error rate is (and will likely remain in the foreseeable future) abundantly within the limits of the capabilities of error correction code schemes.
- Finally, Chapter 6 is devoted to the investigation of the main factors that affect the temperature dependence of soft error rate. Experimental data on neutron (both thermal and wide-spectrum) and alpha-particle irradiations are presented for SRAM devices manufactured by different vendors. SPICE simulations and analytical modeling are used to interpret the experimental data and to demonstrate that soft error rate temperature dependence is influenced by a complex mixture of parameters that generally go in the direction of increasing the sensitivity to soft error.

Chapter 1

Introduction

"The minimum device size under reasonable conditions is approximately 10 μm, which is not far from devices now in the planning stage and within reach of existing techniques". This pessimistic prediction was made by from Wallmark and Marcus in 1962 [Wallmark,Marcus1962]. According to them, one of the factor threatening the evolution of CMOS technology was the "*influence of cosmic rays"*. What Wallmark and Marcus theorized nearly 50 years ago, the possible occurrence of either *"temporary failures due to cosmic ray ionization"* or *"permanent failures induced by cosmic rays through atomic displacements"*, could not be more relevant today!

Fatally, in that same year, 1962, the failure of the Telstar communication satellite demonstrated the susceptibility of electronics to ionizing radiation for the first time. Since that time, the radiation effect community has come a long way and a variety of different phenomena have been discovered and carefully studied in several categories of electronic components and systems. However, the continuous evolution of the technology dictated by Moore's law is bringing about more and more miniaturized and high-performance devices, causing an enhanced sensitivity not only to intrinsic variations but also to external disturbances, such as heavy-ion strikes.

This purpose of this first chapter is to provide an overview of the state-of-the-art in radiation effects on Flash memories, which will be the main focus of this work, and, to a lesser extent, on SRAMs. With regards to Flash memories, Single Event Effects and Total Ionizing Dose on both the floating gate memory array and the peripheral circuitry are investigated, and some issues related to the post radiation annealing are presented as well. As far as SRAMs are concerned, the effects of temperature on the Single Event Upset sensitivity of the devices are discussed. The issues that are still open in the literature are highlighted, laying the basis for the motivation of the work that will be presented in the following chapters of this thesis.

1.1 Flash memories: state of the art and scaling trends

Due to their extremely high density and 10-year data retention, nowadays Flash memories are one of the most attractive non-volatile solutions in virtually all applications. The origins of the name 'Flash' date back to the 1980's, when Masuoka *et al.* from Toshiba presented the first 2.0-μm Flash memory cell at IEDM (International Electron Devices Meeting) [Masuoka1984]. In this device the digital information was stored in a Floating Gate transistor, whose threshold voltage was controlled by the injection and removal of charge in a floating electrode. Since the beginning of this decade, Flash memories have experienced a huge growth and, together with DRAMs, they are now dominating the semiconductor memory market. Flash memories can retain information in the Floating Gate cells for many years in the absence of applied power, and they are able to sustain hundreds of thousands of erase/program cycles.

Today, Flash memories are extensively used in the terrestrial environment. Their widespread growth during the last decade has been mainly driven by cellular phones and other portable applications such as digital cameras, MP3 players, palmtops, etc. Flash are also arousing increasing interest with regards to the possibility of mass storage in computers and in the future they will likely replace hard disks. In addition to this, they are also widely used in dependable applications (e.g., automotive, biomedical, banking, etc.) where reliability issues are a vital factor.

Besides ground-level use, commercial Flash are attractive for space and satellite applications. Just to mention a few examples in this field, Flash memories can be used either to store small amounts of mission critical information (e.g., boot codes) or in multi-Gbyte data recorders where large amounts of data are accumulated.

The study of radiation susceptibility is a necessary requirement when using a Flash device in all the above mentioned applications. In fact, electronic chips operating at sea level are constantly bombarded by a shower of wide-spectrum neutrons, which originate in the interactions of cosmic rays with the outer layers of the atmosphere. In addition, inevitable radioactive contaminants in the package and solder materials emit alpha particles, which may reach sensitive device areas and produce errors. Even worse, spacecraft and satellite electronics must operate in an environment that is much more hostile, because the significant presence of ionizing radiation, in the form of protons, electrons, and heavy-ions coming from various sources, constantly threatens the reliability of the devices.

Unfortunately, Flash memories are not immune from radiation effects. Due to their complexity and large number of diverse building blocks, they exhibit quite complex failure signatures when exposed to ionizing particles. This is especially true for the space environment, where mitigation strategies are mandatory due to the severity of the effects. Yet, ionizing radiation issues are becoming a growing concern also at ground level, due to the ever-decreasing feature size, which is making floating gate cells sensitive to even small external disturbances, such as those caused by atmospheric neutrons and alpha particles.

Accurate assessment of radiation sensitivity and identification of root causes are becoming progressively more difficult tasks in state-of-the-art Flash memories. Sensitivity to radiation affects, in different ways, both the floating gate cells, and the peripheral circuitry. As in all integrated circuits, the scaling of technology is causing single event effects to become more and more complex to study, as the feature size has been scaled into the deep submicron realm. In fact, the cell feature size has been shrunk, but the particle track remains the same: nowadays the feature size of a modern transistor is comparable to the size of an ion track. Phenomena that were once confined to a single circuit node can now involve multiple nodes of SRAM or Flash memory cells [Tipton2008] [Cellere2007a] and charge sharing can occur [Castellani-Coulie2001]. This has caused a significant rise in the number of multiple bit upsets, which may, for instance, pose serious problems for the effectiveness of Error Correction Codes in Flash memories.

In addition, due to the introduction of new materials in the fabrication process (e.g., Tungsten), changes in the operation modes and cell architectures (e.g., Multi-Level Cell devices - MLC), new radiation-induced failure modes appear whose comprehension may be not straightforward at all. Quite often it is not easy to identify the exact malfunction during radiation testing, especially when the manufacturer is not willing to provide detailed information on the device architecture.

What to expect from future technologies is a tricky question; recently, Butt and Alam, cast a dark shadow on the scaling of Floating Gate cell memories at sea level, due to the rapid decrease of charge loss tolerance with decreasing feature size [Butt,Alam2008].

In the following sections, the existing literature on the two main broad categories of radiation effects which affect Flash memories, Total Ionizing Dose and Single Event Effects, is presented. After that, post-exposure annealing effects in radiation-induced errors in Floating Gate cells are investigated. The final section will be devoted to the increasing importance of neutron-induced errors in the most advanced Flash technologies.

1.2 Total Ionizing Dose effects

Total Ionizing Dose (TID) effects are peculiar to the space environment, or to applications where intense sources of man-made radiation exist (e.g., nuclear power plants), and are of less concern for the terrestrial environment. These effects can be a serious threat for electronic circuits. Even though TID phenomena are becoming less problematic with technology scaling for low-voltage circuits (which use thin oxide layers that are less prone to charge trapping), this is not necessarily the case for Flash memories.

The scaling of Floating Gate transistor is problematic. In fact, the tunnel oxides cannot be reduced below ~7 nm lest the cell retention properties degrade. This, in turn, means that the voltages that are necessary to erase and program the cells cannot be reduced either, and the oxides in the charge pump circuitry must be thick enough to sustain the high electric fields that are required during program and erase operations. As a consequence, charge

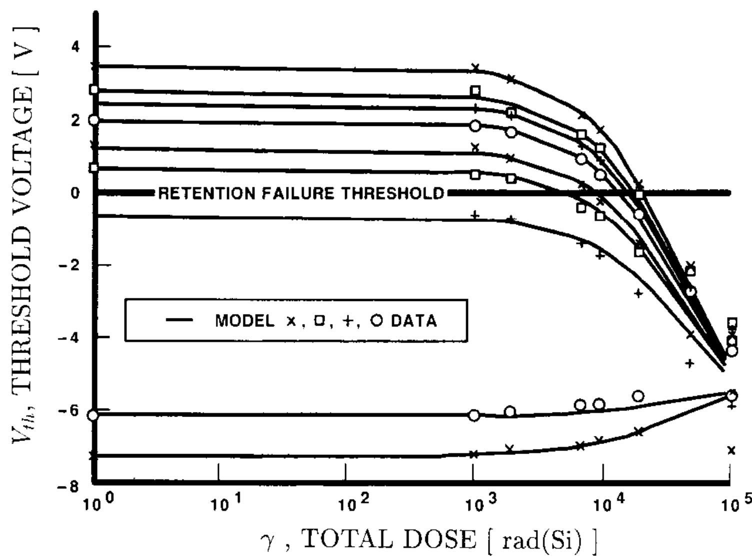


Fig. 1.1. Experimental variations in the threshold voltage of floating gate cells exposed to TID, as a function of the received dose [Snyder1989].

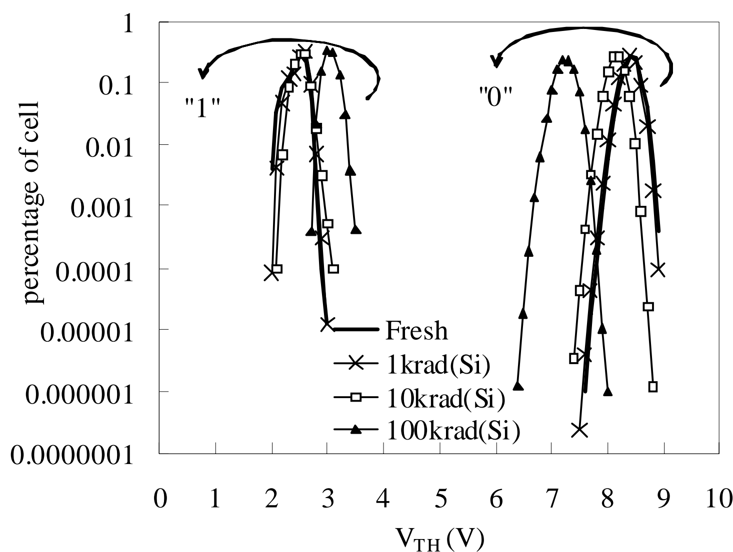


Fig. 1.2. Probability distributions for the threshold voltage of FG cells before and after 10-keV x-ray irradiation. The dose steps are 1 krad(Si), 10 krad(Si), and 100 krad(Si) [Cellere2004a].

trapping in the above mentioned oxides is a concern that must be taken into account when dealing with TID effects in Flash memories.

Let us first examine what happens to the Floating Gate (FG) array when it is exposed to TID. Snyder *et al.* showed for the first time in 1989 that the threshold voltage (V_{th}) of a FG cell can be affected by TID exposure [Snyder1989]. The effect is depicted in Fig. 1.1: as total dose accumulates, the window between the programmed (high V_{th}) and the erased (low V_{th}) status is increasingly reduced, and both erased and programmed cells tend to move

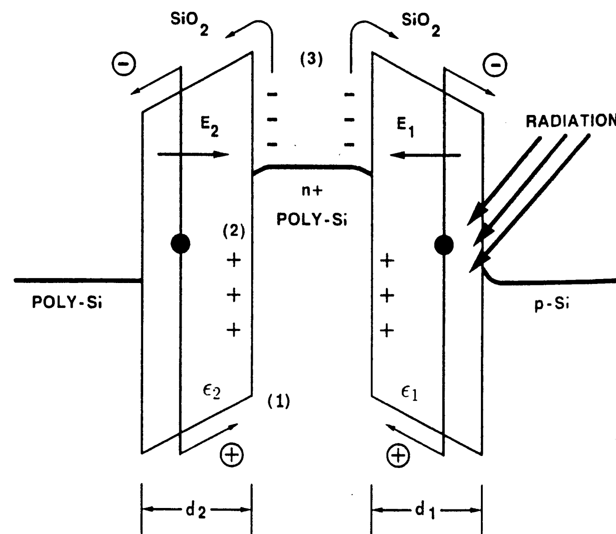


Fig. 1.3. Main contributions to the degradation of the threshold voltage in a FG cell exposed to TID [Snyder1989].

towards the neutral level (corresponding to absence of charge in the FG).

This can also be seen in terms of V_{th} distributions before and after irradiation (Fig. 1.2). After exposure, the erased distribution shifts to higher values of V_{th} due to the loss of holes from the FG, while the programmed peak moves to lower values of V_{th} due to the loss of electrons (note that the neutral level is situated between the erased and programmed distributions) [Cellere2004a].

A physics model to account for these experimental observations was initially developed by Snyder and collaborators [Snyder1989] (see Fig. 1.3) and has recently been developed to account for the changes in the technology that have occurred over the last 20 years [Cellere2004a] [Cellere2005a]. Briefly, charge is generated in the oxides surrounding the FG. Depending on the oxide electric field, part of these carriers recombine [Onsager1938] [Ausman1986]. After recombination, the carriers thermalize, then electrons are quickly swept away from the oxide [Hughes1973] thanks to their high mobility, while holes slowly move toward the FG and may either reach the FG, where they recombine part of the stored negative charge (mechanism (1) in Fig. 1.3), or they are trapped in the oxide (mechanism (2) in Fig. 1.3) [Hughes1975] [Boesch1975]. In both cases, the net effect is a reduction of the cell V_{th}. Furthermore, electrons in the FG may acquire enough energy from the incoming radiation [Katznelson,Frohman-Bentchkowsky1980] to jump over the oxide barrier (mechanism (3) in Fig. 1.3). However, there are several aspects which need to be considered when adapting this model to modern devices, including:

i) the above description of different phenomena occurring in a strict sequential order is not realistic in the tunnel oxide of FG devices, since recombination, thermalization, and electron transit times are of the same order of magnitude in the range of the tunnel oxide thickness (10 nm or less) appropriate for modern devices;

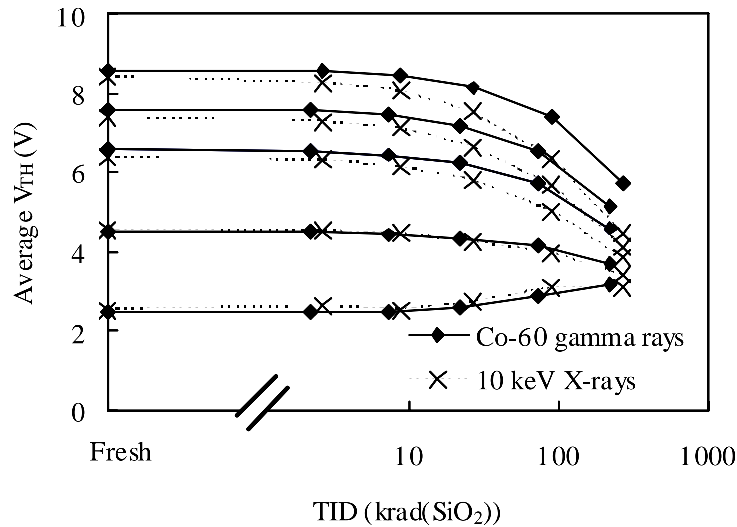


Fig. 1.4. Average threshold voltage of sectors of FG cells irradiated with 10 keV x-rays and with ^{60}Co γ-rays as a function of total dose [Cellere2007b].

ii) the interpoly dielectric is an ONO sandwich in all modern devices, not a SiO_2 layer as in [Snyder1989], so the different dynamics of charge generation and trapping in the nitride layer has to be carefully considered [Raparla2003] [Aozasa1999];

iii) the lateral dimensions of the FGs cannot be neglected.

When all these aspects are taken into account, proper modeling can accurately describe the average V_{th} shift as a function of the received dose, as shown in Fig. 1.4 [Cellere2007b]. In this figure, two data sets are reported. The first one was obtained with ^{60}Co γ-rays, and the second with 10 keV x-rays. It is clear that the degradation induced by x-rays is much larger, likely due to dose enhancements effects. In fact, 1.25 MeV photons generate high energy Compton electrons, whereas low energy photons (< 50 keV) generated by the x-rays source interact with the material through the photoelectric effect, which is particularly effective in presence of interfaces between high-Z and low-Z materials [Oldham,McGarrity1983] [Fleetwood1986]. As a result, the Si/SiO_2 interface enhances the V_{th} degradation observed with x-rays with respect to gamma. Up to now TID effects in the FG cell array have been described. These effects can be observed either by using dedicated test chips, to avoid the interference of the peripheral circuitry, or by performing selective irradiations in commercial, complete devices. However, as mentioned in Section 1.1, the wide variety of effects that may occur during TID exposure of a Flash memory strongly involve the control circuitry as well. In the last decade, several contributions have explored these issues in devices exposed to protons, gamma rays, x rays, among which [Nguyen1998] [Nguyen1999] [Roth2000] [Nguyen,Scheick2002] [Nguyen,Scheick2003] [Langley,Murray2004] [Oldham2006] [Nguyen,Irom2007] [Schmidt2008].

There is no single way to define the radiation hardness of a Flash memory, because the response to radiation strongly depends on how the device is operated during exposure and on

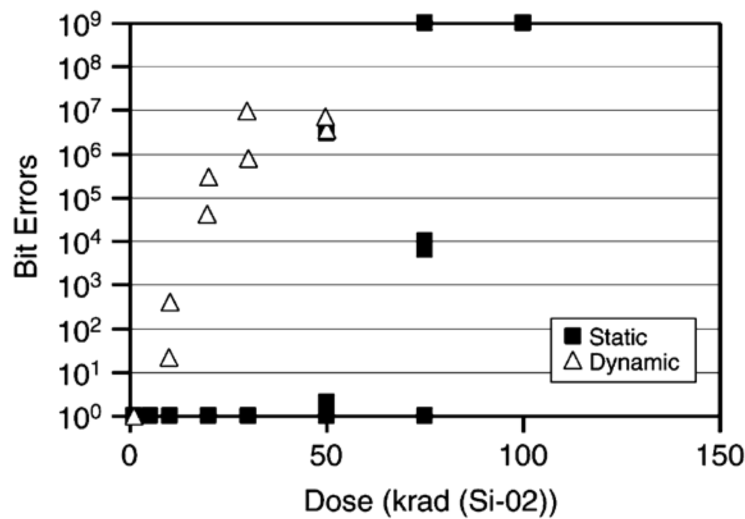


Fig. 1.5. Comparison of static and dynamic bit errors as a function of total dose in a Flash NAND memory irradiated with a Co^{60} gamma source [Oldham2006].

how it is tested after exposure. Fig. 1.5 is an example of a 90-nm SLC NAND memory irradiated with Co-60 and then tested under either dynamic conditions (i.e., with the part exercised with read/erase/program cycles between TID exposures) or under static conditions (programmed with checkerboard initially, and then tested in read-only mode between exposures). The graph shows that the number of dynamic errors can be much larger than static errors [Oldham2006].

As a result, the TID failure dose is usually defined by observing different parameters, according to the particular application one is interested in. To mention some examples, one can be interested in evaluating the programmability (or program time), erasability, read errors, supply (idle or active) current, access time, etc. Obviously, depending on the observed parameter, the experimental procedure may change from case to case. Hence, the maximum total dose that can be withstood by a Flash memory not only varies from device to device [Langley,Murray2004] [Oldham2006], but also strongly depends on the failure criterion. After TID exposure, Flash memories may draw excessive supply current [Nguyen1999] [Layton2005], fail to program and/or erase [Nguyen1999] [Oldham2006], or suffer from reduced operation speed and timing errors.

Charge pump circuitry that provides the high voltages needed during erase and program (and, in more advanced technologies, also during read operations) has always been demonstrated to be one of the weakest parts of the device. The reason for this great radiation sensitivity is related to the high voltages and the thick gate oxides (~ 35 nm) that characterize these circuits. It is known that the damage introduced by TID is strongly reduced when oxide layers are thinned, due to the lower amount of charge that can be trapped in a thinner oxide with respect to a thicker oxide. Moreover, the presence of a high voltage across an irradiated oxide generally causes more TID degradation; in fact, a higher electric field increases the amount of charge yield, that is the amount of charge which can potentially alter the

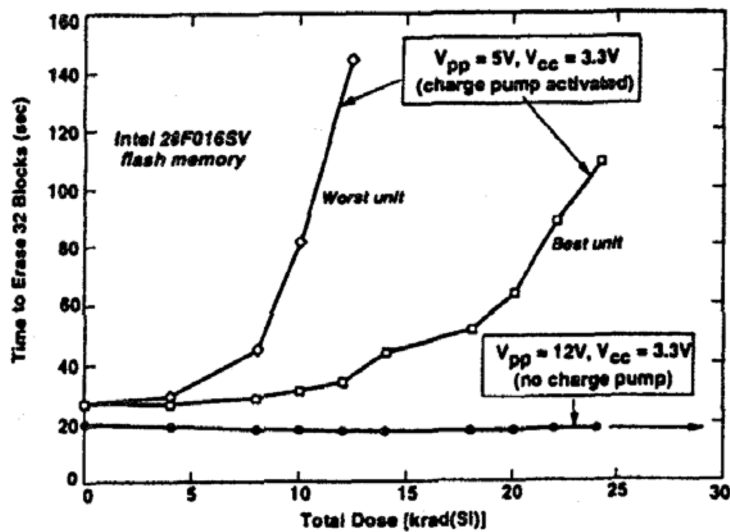


Fig. 1.6. Evolution of the time to erase 32 blocks in a NOR device as a function of the dose. The experiment is performed in two different conditions: device irradiated with activated and disabled charge pump [Nguyen1998].

characteristics of the oxide layers.

About ten years ago, experiments on now obsolete devices, where the use of charge pumps could be disabled by supplying an external voltage, proved that charge pumps played a crucial role for device reliability [Nguyen1998]. Fig. 1.6 shows the time required to erase 32 sectors in a NOR memory as a function of the received dose in two different scenarios: with the charge pump activated and with the charge pump disabled during exposure. In the first case, after a dose of about 5 krad(Si), the time to erase rapidly increases; on the contrary, disabling the pump, the time to erase stays constant even after 30 krad(Si). Nguyen and coauthors attribute the phenomenon to a progressive lowering of the output voltage of the pumps, due to radiation-induced threshold voltage shifts in the PMOS transistors in the charge pump circuitry. The radiation softness of the charge pumps has also been confirmed by more recent work by Oldham *et al.* in 90-nm devices [Oldham2006]. In this work, the authors report that the failure of the charge pump for erase operations is the limiting factor in the TID environment.

However, charge pumps are not the only functional block to display some kind of malfunction during TID exposure. In fact, again in [Oldham2006], rows of bad bits were observed. Fig. 1.7 illustrates the physical locations of bit errors observed during static tests. As seen in the figure, the errors are not randomly distributed in the considered block, but they appear concentrated along given rows (corresponding to given page numbers), so the effect can be attributed to damage to the addressing control circuitry.

To conclude this section, whereas several studies have addressed Total Ionizing Dose issues in Flash memories, much of this work has been limited by the lack of manufacturer information on the internal device structure, without which it is difficult to study in detail

which functional block is responsible for a given behavior. Hence, the limit of the majority of studies is that they cannot unequivocally attribute a given failure signature to one of the different building blocks of Flash memories (even if some guesses can be made, as described in this section).

1.3 Single Event Effects

Differently from Total Ionizing Dose effects, which cause a progressive accumulation of dose hence a progressive degradation in the characteristics of the circuit, Single Event Effects (SEEs) are much more difficult to predict, as they are stochastic events, due to a single ionizing particle that hits the wrong place of the device at the wrong time.

Single event effects occur with high frequency in space, where electronic components are constantly bombarded by a shower of protons and heavy ions, but they are possible also at sea level (although to a lesser extent), due to atmospheric neutrons and alpha particles. In this section the effects of heavy-ion irradiation on Flash memories are described, while neutron issues will be separately covered in Chapter 1.5.

Since the end of the 1990's, scientific reports have shown that the reliability of the control circuitry, and not that of the Floating Gate array, was the most worrying issue concerning Single Event Effects.

More than 10 years ago, NOR and NAND devices produced by different manufacturers showed many types of functional errors [Schwartz1997]. For instance, Fig. 1.8 shows the cross section for functional errors detected during heavy-ion irradiation with the device in static mode (i.e., with no voltage on the charge pumps): these errors are attributed to upsets in memory bits of the microcontroller, for instance failures in individual control bits or control registers in the internal write-state machine. These functional errors

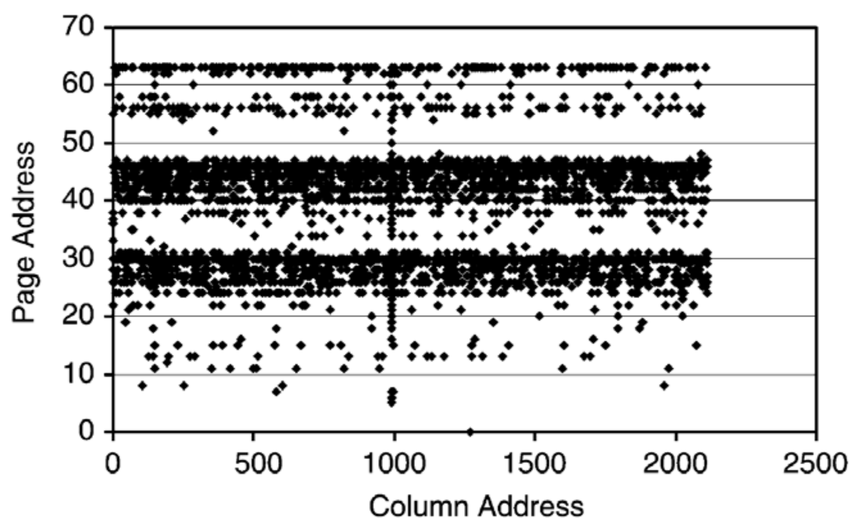


Fig. 1.7. Physical map of the errors featuring a non-random distribution observed during a static test under Co^{60} gamma irradiation of a 90-nm NAND Flash [Oldham2006].

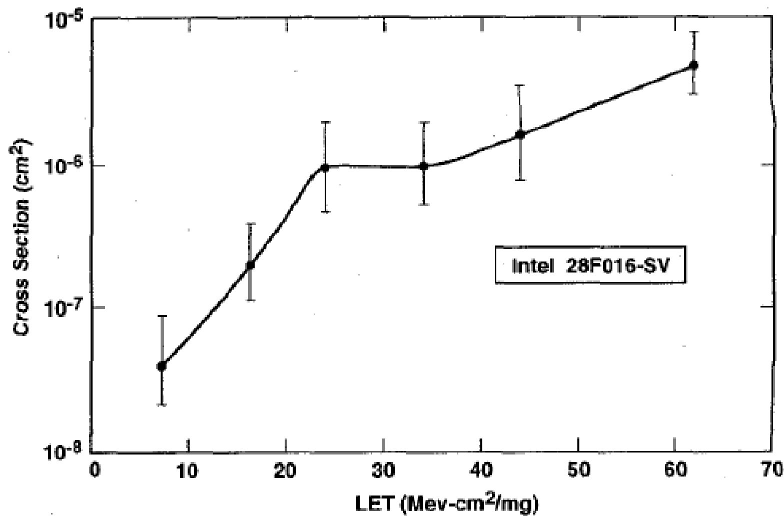


Fig. 1.8. Cross section versus ion LET for functional errors in a NOR memory irradiated in static mode (powered idle device) [Schwartz1997].

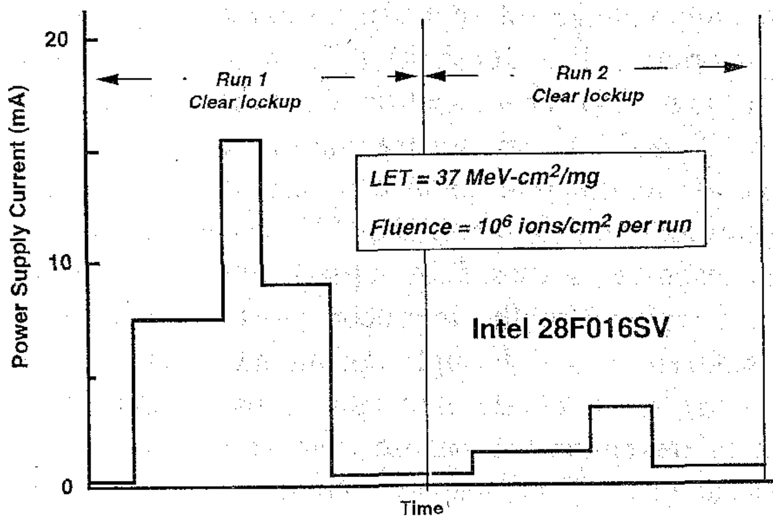


Fig. 1.9. Steps in the power supply current during heavy-ion irradiation for the same device as the one referred in Fig. 1.8. None of these current spikes caused a permanent damage to the device [Schwartz1997].

are frequently accompanied by spikes in the supply current [Schwartz1997]. Fig. 1.9 shows the time evolution of the supply current during exposure to heavy ions. Current jumps sometimes recover without intervention, while at other times they require a power cycle and Schwartz *et al.* attribute them to functional changes in the control- and/or write-state machine, which turn on conflicting logic sections of the device. Therefore, the effects observed in these devices are similar to those that were observed in FPGA devices [Swift,Katz1995].

Besides these functional malfunctions, no FG cell errors were detected neither when the control circuitry was shielded (even at an LET of 60 MeVcm^2/mg), nor when the devices

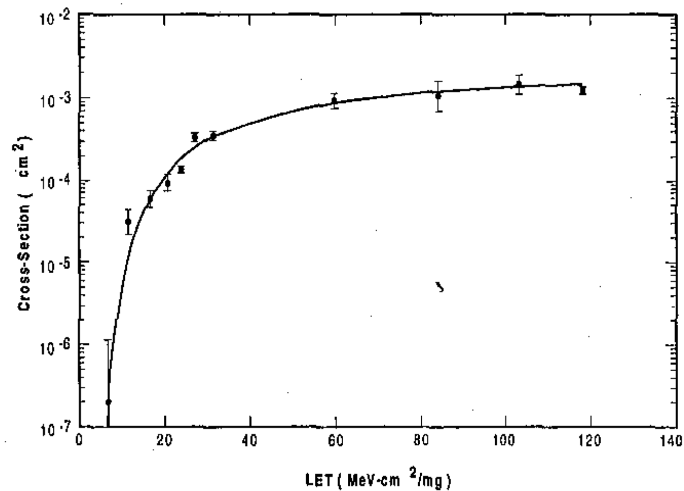


Fig. 1.10. Cross section versus ion LET for the buffer errors in a NAND memory irradiated in static mode (powered idle device) [Nguyen1999].

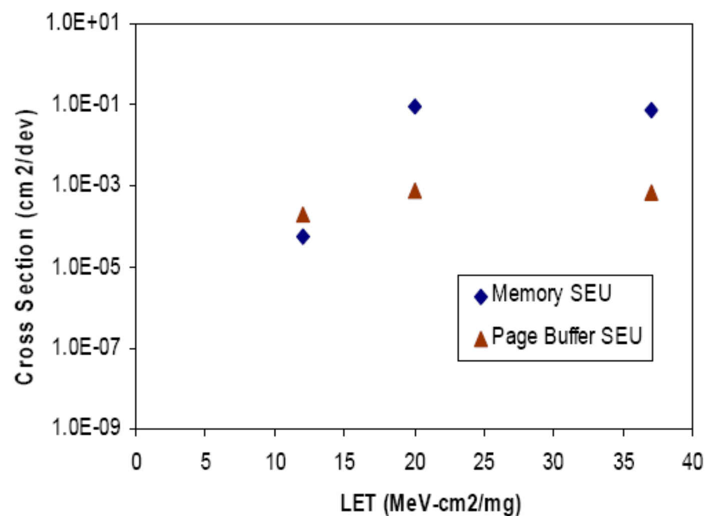


Fig. 1.11. Cross section (per device) versus ion LET for the errors in the buffer and in the memory in a NAND Flash [Langley,Murray2004].

were irradiated unbiased. In fact, at that time, the number of carriers required to store the information in the FG cell was high enough to make it very unlikely that an ion strike could lead to a User Mode error, even though shifts in the cell threshold voltage are mentioned as a possible phenomenon [Schwartz1997].

The conclusion that the logic information stored in floating gate cells could not be affected by a heavy-ion strike proved true for several years [Nguyen1999] [Roth2000] [Krawzsenek2000]. Fig. 1.10 shows, for instance, the error cross section for a NAND memory irradiated in dynamic mode (periodically reading the device under heavy-ion beam). The phenomenon is attributed to upsets in the 528-byte buffer [Nguyen1999].

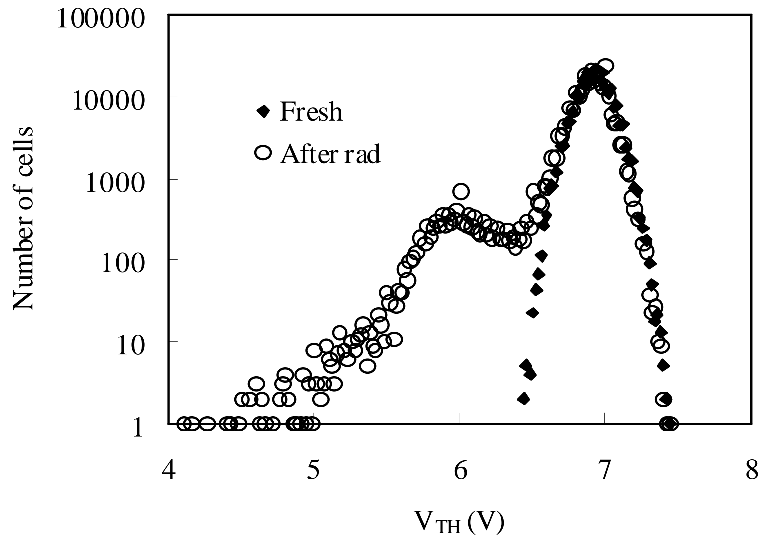


Fig. 1.12. Threshold voltage distribution of FG cells in a NOR memory array before and after irradiation with 2x10^7 Iodine ions/cm^2 [Cellere2001].

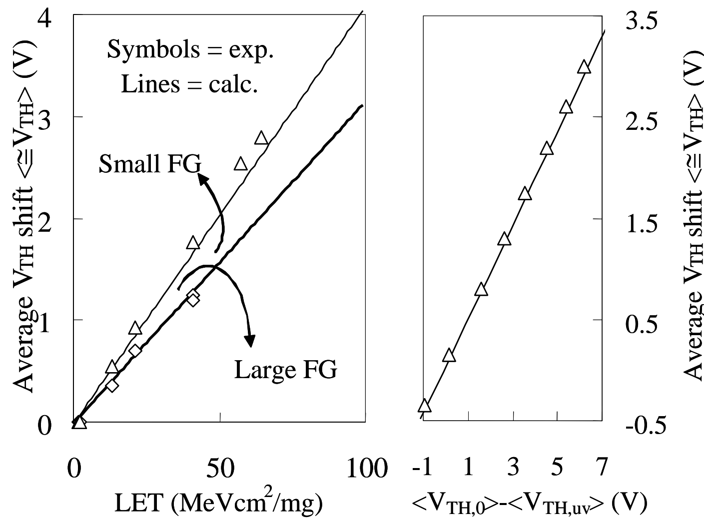


Fig. 1.13. Dependence of the threshold voltage shift on the impinging particle LET (left) and on the electric field across the tunnel oxide (right) [Cellere2004b].

Then, in the first half of this decade, several researchers started to observe the occurrence of errors in the Floating Gate cells as well [Nguyen,Scheick2003] [Koga2004] [Langley,Murray2004]. An example is reported in Fig. 1.11: the cross sections for heavy-ion induced errors in the page buffer and in the memory array are compared [Langley,Murray2004].

The physical origin of these kinds of errors has been widely investigated since the early 2000's and different mechanisms have been proposed in the literature to explain errors in the FG: charge loss due to a conductive path across the tunnel oxide [Cellere2001]

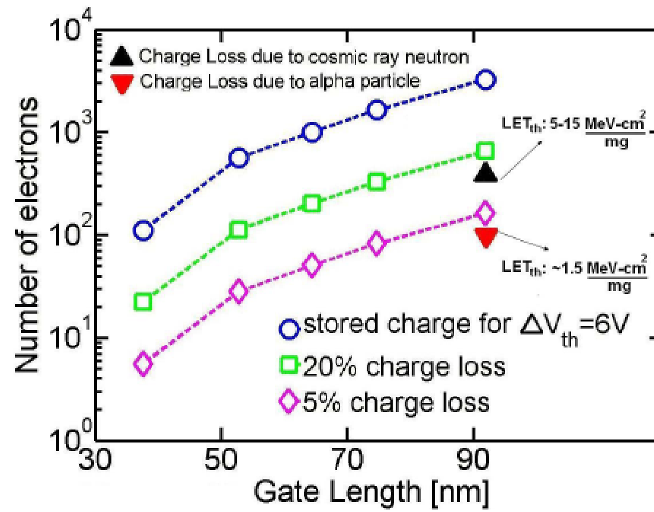
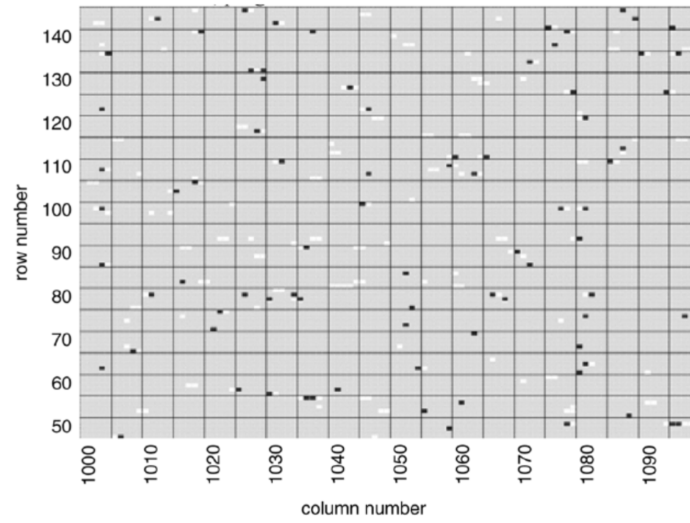


Fig. 1.14. Number of electrons in a NAND Flash (blue circles) and charge loss tolerance (assumed to be 20% for SLC and 5% for MLC devices) as a function of the feature size of the cell. The predicted values for charge loss induced by neutrons and alpha particles are also displayed with solid symbols [Butt,Alam2008].

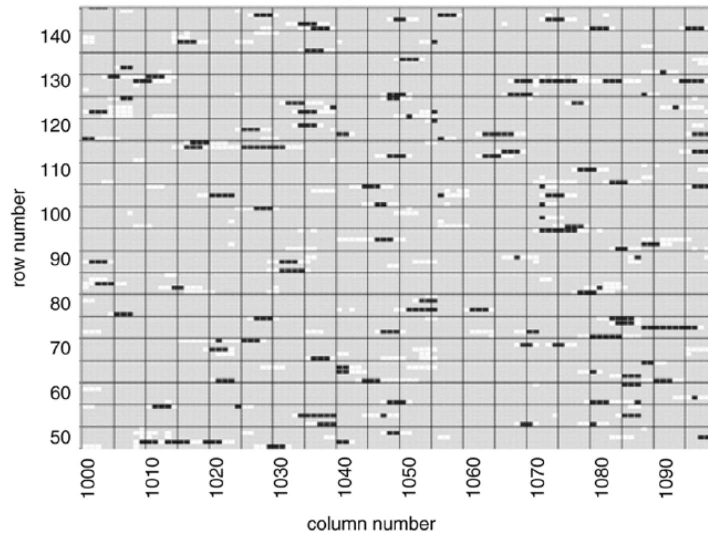
[Cellere2006a], charge trapping in the tunnel oxide and microdose effects [Guertin2006] [Schmidt2007], but also the coexistence of the these phenomena [Oldham2006], and finally, a transient current flux over the oxide barriers [Butt,Alam2008].

In the works by Cellere *et al.*, special test chips were used in order to investigate the effects in the cells, and special measurement structures to study the threshold voltage of the hit cells, without the interference of the peripheral circuitry [Cellere2001]. It turned out that every single ion causes a relatively large but very localized effect, differently from what was seen in the previous section on TID, which uniformly deposits energy and causes a rigid shift in the V_{th} distributions, as illustrated in Fig. 1.2. In fact, in the case of heavy ions, a secondary peak appears in the threshold voltage distributions after exposure, as we can see in Fig. 1.12, corresponding to those FG cells that have been hit by the ions. The distance between the main and the secondary peak is the average threshold voltage shift experienced by hit cells, $<\Delta V_{th}>$.

If we plot the average V_{th} shift as a function of the impinging ion LET and of the tunnel oxide electric field before irradiation [Cellere2004b], we find the results illustrated in Fig. 1.13. As seen in the figures, both relationships are linear (at least for ions having a relatively low energy, such as those used in [Cellere2004b]). Such linear relationships suggest that a model based on charge generation, recombination, and transport, such as that explaining TID effects, is not applicable in this case. In fact, all these phenomena have a strongly non-linear dependence on the electric field that would not be able to explain Fig. 1.13.



(a)



(b)

Fig. 1.15. Physical map of FG cells experiencing a V_{th} shift after Xenon irradiation in a NAND device normal to the beam (a) and tilted 75° (b) [Cellere2007a]

One of the models that were proposed in the literature to clarify these results is based on the idea that the dense electron/hole plasma generated in the tunnel oxide by the incoming ion acts like a resistance, thus promptly discharging the FG [Cellere2006b]. The value of this resistance is linked to the ion LET (for instance, heavier ions result in a denser track, hence in lower resistance and larger discharge) and the duration of the path is linked to the presence of electrons in the FG. In fact, $<\Delta V_{TH}>$ linearly depends on the number of generated electrons/holes (not on the surviving recombination) and this means that charge loss happens before recombination. As for the time scale of the phenomenon, according to [Cellere2006b], the FG discharge is believed to happen in about 10 fs.

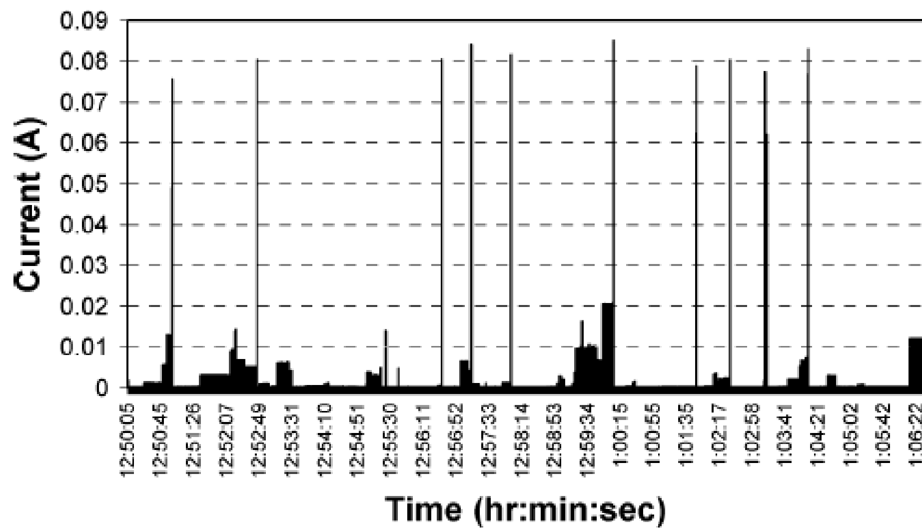


Fig. 1.16.Temporal evolution of the supply current in a NAND Flash irradiated with Tantalum in standby mode [Irom,Nguyen2007].

Another interesting thing to note in Fig. 1.13 is that with technology shrinking the amount of ΔV_{th} increases. This is why in the second half of this decade we have witnessed a progressively higher importance of errors in the FG cells. In fact, with the scaling of technology, the sensitivity of the FGs is expected to increase, due to the smaller number of electrons/holes stored in the programmed/erased status and the introduction of MLC devices, which further complicate the issue. Fig. 1.14 shows the number of carriers required to store information in the FG as a function of the cell technology node (blue circles), together with the charge loss tolerance (assumed to be 20% in Single Level Cell and 5% in Multi-Level Cell devices). Note that the value of charge loss tolerance chosen for MLC memories is lower with respect to SLC due to the lower margin between the program levels. A remarkable feature in the graph in Fig. 1.14 is the rapid decrease of the storage charge as the gate length shrinks, meaning an enhanced sensitivity to heavy-ion strikes for more advanced samples.

Finally, in any real environment, be it space, high energy physics, or simply the atmosphere, particles obviously do not cross the devices normally to the silicon surface. Interestingly, at grazing angles an ion hit can lead to the formation of a “tail” of FG cells with corrupted information [Cellere2007a]. In particular, a single particle strike can affect the threshold voltage of more than 20 consecutive FG transistors. Fig. 1.15 depicts the physical map of FG cells experiencing V_{th} shifts in a NAND device irradiated at different angles with respect to the beam (normal incidence and 75°). It is easy to imagine that this issue will be exacerbated as technology scaling brings about more and more dense devices, due to charge collection at multiple nodes, causing a serious threat for the capability of ECC algorithms.

Putting together all the observed contributions, the picture of possible Single Event Effects in a modern Flash memory forms a very intricate scenario, as emerges from several recent reports [Guertin2006] [Oldham2006] [Nguyen2006] [Irom,Nguyen2007] [Schmidt2007] [Oldham2007] [Schmidt2008]. In fact, prompt effects, annealing effects, control circuitry phenomena, more or less destructive, including transient errors, current spikes even in standby mode, and functional interruptions, all act together. An example of a destructive phenomenon that was recently observed in some advanced NAND Flash devices is illustrated in Fig. 1.16 [Irom,Nguyen2007]. As seen in the graph, a sample irradiated with heavy ions in standby operating mode experiences several jumps in the supply current (up to 85 mA) that largely exceed the nominal operating current (which is about 3 mA in these devices). These large current spikes usually recover without intervention (so they certainly cannot be identified with Single Event Latchup) and they may be destructive or not. Interestingly, only devices manufactured by given vendors displayed this behavior. The physical origin of the phenomenon has not been understood in detail yet, but there some elements suggesting that the damage likely originates in the charge pump circuitry. In addition, [Oldham2009] shows that these current spikes are not present if the memories are irradiated with lower ion fluxes (< 10^3 ions/cm^2/s rather than 10^4 ions/cm^2/s) and this is an indication that the phenomenon may be caused by multiple ions hitting sensitive regions simultaneously.

As a final note, even though during the last decade the radiation effect community has come a long way and several effects were identified and explained in irradiated Flash memories, several issues are still open. Just to mention one of them, despite the so-called 'static errors' (originating in the FG cells) and 'dynamic errors' (originating in the peripheral circuitry and usually attributed to the page buffer) have been described in a number of reports [Nguyen,Scheick2003] [Langley,Murray2004] [Oldham2006] (see Fig. 1.11), no systematic studies exist on the FG array and page buffer contributions, in relation to factors like the pattern stored in the memory, the operation mode, the LET of impinging ions, etc. As a result, it is not clear how to predict the device behavior when exposed to heavy ions taking into account, for instance, the operating conditions during irradiation.

1.4 Annealing of radiation-induced errors

The damage introduced by radiation is not stable over time. In fact, it can evolve during and after exposure. This process takes place, at room temperature, due to the neutralization and compensation of charge that has been trapped in the oxide layers following irradiation [Schwank1984] [Lelis1988] [Lelis1989] [Oldham,McLean2003]; at high temperature, other phenomena like the annealing of interface traps take place as well [Schwank1984].

Fig. 1.17 shows an example of post-radiation annealing: the threshold voltage of an NMOSFET is plotted as a function of time after irradiation [Schwank1984]. As seen in the

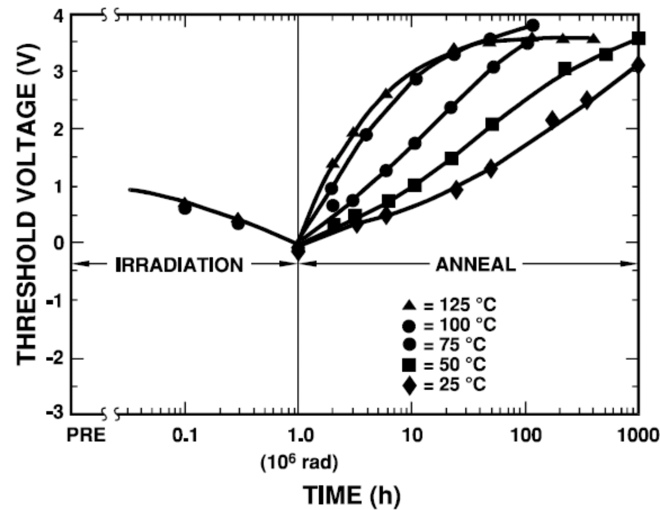


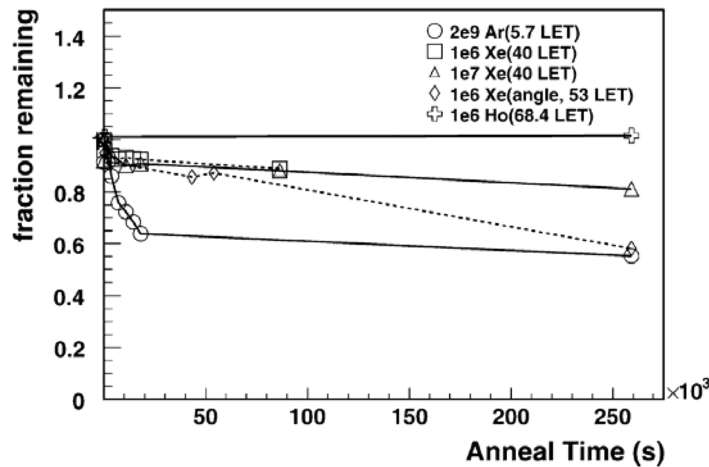
Fig. 1.17. Temporal evolution of the threshold voltage in an n-MOSFET after irradiation at different temperatures [Schwank1984].

graph, immediately after exposure, the V_{th} of the device is lower than prior to irradiation and the shift can be large enough to cause functional failure of the component. Then, in the hours after exposure, the threshold voltage increases, due to the tunneling of electrons into the oxide. Annealing phenomena are usually accelerated at high temperature as seen, for instance, in Fig. 1.17.

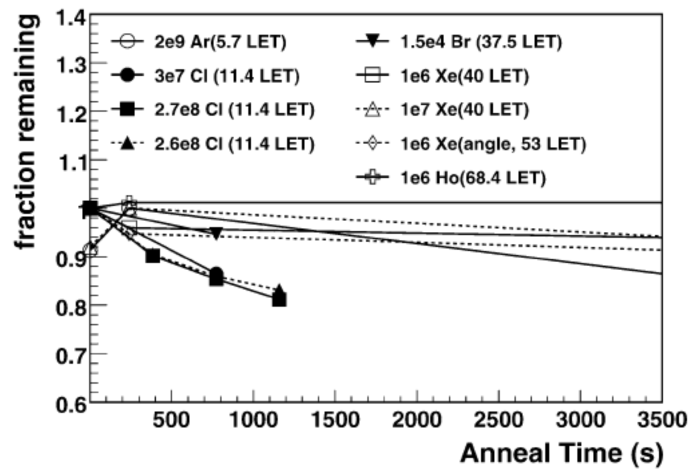
Depending on several factors, among which the type of irradiated device, the radiation source used, and the features of the observed effects, annealing can either improve or worsen the damage caused by the exposure. For this reason, it is always important not to neglect the post-exposure behavior during both TID and SEE radiation studies. For instance, annealing effects should be taken into account when the result of an accelerated test, performed at high dose rate, needs to be extrapolated to a low dose rate environment, where the amount of annealed damage may be important [Fleetwood,Eisen2003]. Annealing phenomena may also be considerable after heavy-ion irradiation, for instance for stuck bits induced by exposure in an SRAM device [Dufour1992].

With regards to Flash memories, given the relatively thick oxides (tunnel oxide thickness is about 7-10 nm) that are present in Floating Gate cells, one can look at the possibility that FG errors evolve after irradiation.

Few works exist in the literature describing annealing effects in Flash memories. Recently, Guertin *et al.* reported the decrease in the number of Floating Gate errors up to 3 days after heavy-ion exposure [Guertin2006]. Fig. 1.18 describes both the long-term and short-term temporal evolution of the fraction of remaining raw bit errors in NAND samples irradiated with different heavy ions. This behavior indicates that the result of irradiation is not only connected with loss of charge from the FG [Cellere2001]; according to Guertin and collaborators, some charge must have been trapped (and display some kind of evolution after



(a)

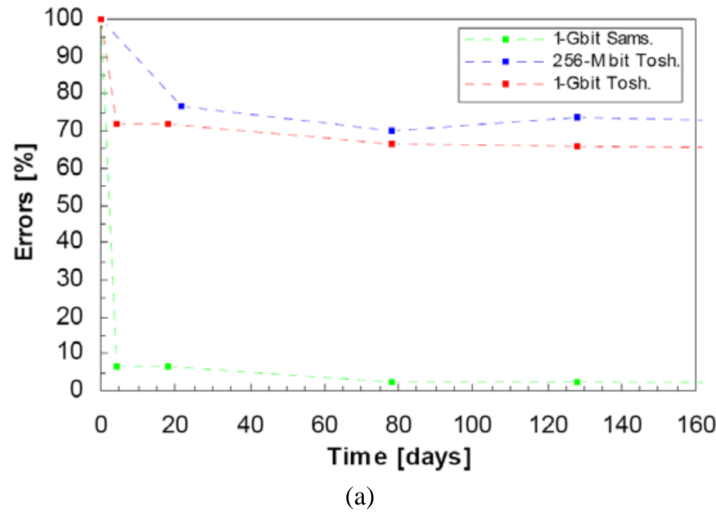


(b)

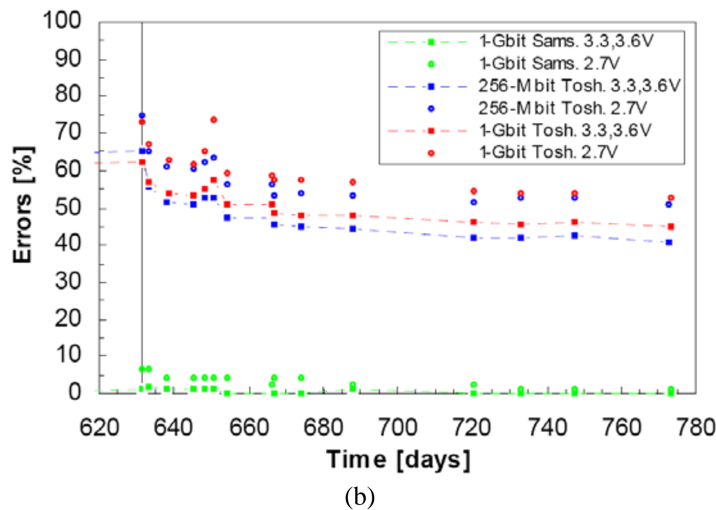
Fig. 1.18. Long-term (a) and short-term (b) annealing of the number of raw bit errors in a NAND memory irradiated with different heavy ions, in particular the number of remaining errors is plotted as a function of time [Guertin2006].

exposure) in one or more of the oxides surrounding the FG. In particular, the authors attribute the effect to either recombination or migration (especially in the ONO structure towards the top of the ONO-FG-TO sandwich) of trapped holes.

One year later, Schmidt and collaborators described a decrease in the number of errors as well, which can be strongly enhanced after high-temperature annealing [Schmidt2007]. Fig. 1.19 shows the percentage of raw bit errors as a function of time after irradiation, for room-temperature annealing (a) and 100°C annealing (b). As seen in the graphs, the decrease in the errors is significant in the first few days after exposure at room temperature, while it is negligible in the subsequent days. On the contrary, a much more evident decrease in the FG errors is present after high-temperature annealing, even several hundred days after irradiation. Schmidt *et al.* propose the idea that due to microdose effects following



(a)



(b)

Fig. 1.19. Room temperature annealing (a) and high-temperature (100°C) annealing (b) for the percentage of raw bit errors for NAND devices produced by different manufacturers irradiated with heavy ions [Schmidt2007].

irradiation, positive charge gets trapped in the tunnel oxide and balances the charge stored in the FG, lowering the threshold voltage of the cell. Then, according to [Schmidt2007], trapped holes may escape after exposure, hence the original value of the cell threshold voltage is restored. In this study there are also some data taken with ions having different LET values. The authors attribute the different annealing percentages to the different number of 'persistent errors', which in turn depends on both the ion LET and on the studied device.

On the other hand, most of the works on Total Ionizing Dose effects in floating gate cells do not analyze post-radiation annealing. In fact, existing reports such as [Cellere2004a] [Cellere2005a] [Cellere2007b] usually analyze the threshold voltage shift following exposure after the short-term annealing process was reasonably completed (in the above mentioned works, devices were measured several days after irradiation). To our knowledge,

the only work in the literature describing possible annealing in FG errors is [Oldham2006]. In this study, the authors reported that after TID (but also heavy-ion) exposure, a rapid annealing process occurs due to the reduced thickness of the tunnel oxide, which allows the positive charge trapped in the oxide (which compensates the negative charge in the FG of programmed cells) to disappear through the tunnel effect.

The results shown in this section demonstrate that, despite the experimental evidence that annealing effects exist in Flash memories, possibly leading the FG errors to disappear after heavy-ion and TID exposure, a systematic analysis of the memory behavior after heavy-ion exposure is not present in literature. In addition, to our knowledge, no reports exist showing quantitative results on the evolution of either cell V_{th} or the number of FG errors after TID exposure.

1.5 Soft errors induced by atmospheric neutrons

Space is known as a harsh radiation environment, as discussed in the previous sections, but also the earth atmosphere is not free from radiation, due to showers of particles mainly generated by protons of galactic origin [Ziegler2004]. In fact, galactic cosmic rays, as they penetrate into the atmosphere, interact with atmospheric layers, generating secondary cascades of different types of particles.

Even though muons are the most abundant particles at sea level, neutrons are the most important ones from the standpoint of electronic reliability, because they are able to trigger nuclear reactions inside the chips, giving rise to charged secondary by-products

Flash Memory Arrays [Size/Technology]	Threshold LET [MeV-cm^2/mg]	Saturation Cross section [cm^2/bit]	Reference
4 Gb/90nm	3.4	$6x10^{-11}$	[Irom,Nguyen2007]
1 Gbit/No data	3	$2x10^{-11}$	[Irom2007]
2 Gb/90nm	12	$5x10^{-13}$	[Oldham2006]
1 Gb/90nm	No data	$6x10^{-11}$	[Bagatin2007]
1Gb/No data	5	$1x10^{-10}$	[Langley,Murray2004]
4Gb/63nm	3.5	$5x10^{-11}$	[Oldham2007]

Table 1.I. Summary of heavy-ion SEU tests in high-density commercial NAND Flash taken from different sources in literature [Irom,Nguyen2007] [Irom2007] [Oldham2006] [Oldham2007] [Bagatin2007] [Langley,Murray2004].

[Braley2002], something which muons cannot do. In turn, reaction byproducts may be ionizing particles, which deposit charge and disturb the operation of electronic chips (e.g., they may create a bit flip). The probability of interaction between neutrons and matter is very small and not all the ionizing byproducts will cross the device sensitive area; however, a huge amount of devices are unavoidably exposed to the average flux of about 14 neutrons/cm^2 hr [Gordon2004] at sea-level. Furthermore, the neutron flux increases with altitude, reaching a peak very close to the cruise altitude of airplanes, posing an even more serious threat to avionics.

The scaling of technology is bringing about an increased sensitivity to Single Event Upsets in CMOS circuits. For instance, more than 20 years ago, a SRAM cell could experience a bit flip only if it was exposed to ions with very high LET [Nichols1985]. Then, as years passed, SEUs were observed in SRAMs also with lighter ions and uncharged particles like neutrons, due to the progressive decrease of the critical charge (i.e., the minimum charge deposited in the sensitive area that is able to trigger an upset).

As a consequence, the concern of the radiation effect community about soft errors is no more limited to specialized and niche applications, such as those in the satellite industry or front-end electronics for high energy physics, but it has been extended to safety critical medical equipment as well, such as pacemakers or defibrillators [Wilkinson2005] [Wilkinson,Hareland2005], and finally to computing server facilities [Sanda2008].

The majority of studies on neutron-induced soft errors in CMOS memories have been conducted on SRAMs and DRAMs [Baumann2005]. On the other hand, the vulnerability of Flash memories to soft errors after neutron exposure has been dismissed as negligible by some authors [Fogle2004], but suggested by others [Butt2008] in more recent times.

In 2007 Irom *et al.* reported the results of the irradiation of Flash memories with 14-MeV monoenergetic neutrons: very few neutron-induced errors (or even none) were detected in 1-Gbit Single Level Cell NAND and 64-Mbit NOR memories [Irom2007].

However, if we consider more advanced and scaled Flash devices, it is reasonable that some raw bit errors appear during neutron irradiation, based on the heavy-ion sensitivity of these devices [Cellere,Paccagnella2004] [Oldham2006] [Irom,Nguyen2007]. In fact, in recent reports FG errors have been observed in state-of-the-art Flash memories with smaller and smaller values of threshold LET, as described in Table 1.I, whose values are taken from [Irom,Nguyen2007], [Irom2007], [Oldham2006], [Oldham2007], [Bagatin2007], [Langley,Murray2004]. The values of the threshold LET for Floating Gate errors indicate that neutron byproducts can likely produce raw bit errors in Flash memories belonging to recent technology nodes.

1.6 Temperature dependence of soft error rate

In the previous sections, we saw how Total Ionizing Dose effects and Single Event Effects can disturb the functionality of a complex device such as a Flash memory. However, the benchmark that is traditionally used to define the radiation sensitivity of a CMOS technology node is the SRAM cell. This kind of memory is present in virtually all applications that relies on volatile storage, for instance in the configuration memory of FPGAs, or, to stay close to the previous sections, in the page buffer of a Flash. The SRAM cell is nowadays one of the most radiation-sensitive types of solid-state storage and, being relatively easy to test, is one of the reference points for soft error studies [Baumann2005].

An impressive amount of work has been carried out in the field of Single Event Upsets in SRAMs: experimental, simulation, and modeling efforts have led to a deep understanding of the phenomenon. Just to mention a few examples, funneling effects have been discovered and modeled [Hsieh1981]; the role of the struck junction load on the particle-induced transient has been elucidated [Dodd,Sexton1995]; neutron nuclear reactions leading to charged byproducts have been analyzed in the context of terrestrial Soft Error Rate [Palau2001]. Yet, despite the huge amount of work, some areas have received relatively little attention from the research community.

It is well known that electronic chips in many situations must operate at temperatures significantly higher than room temperature, especially for high-performance, space, or automotive applications. Contrary to Single Event Latchup (SEL) tests that are performed at the highest operating temperature [Kolasinski1986] [Hutson2007] (as recommended by the JEDEC standard), SEU measurements are usually carried out at room temperature [Grandlund2006] and very little is known about the SEU rate dependence on temperature. Only a few works in the literature analyzed (or even mentioned) the effects of temperature

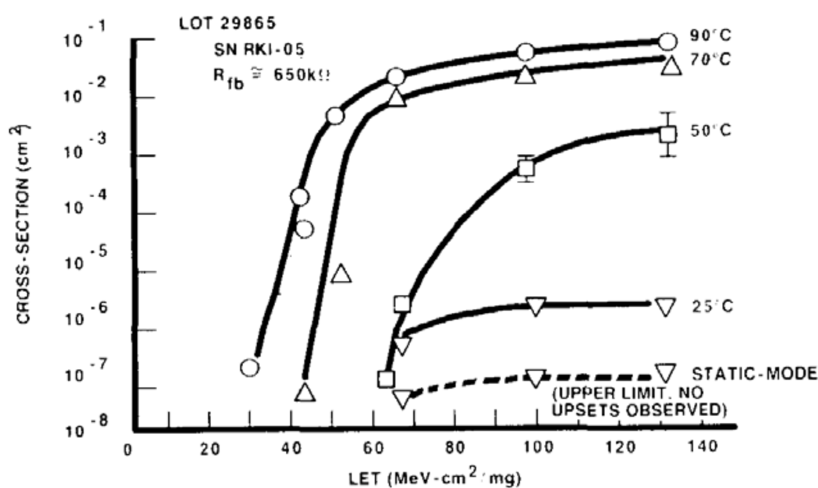


Fig. 1.20. Temperature dependence of the heavy-ion cross section in a radiation-hardened 256K SRAM at 4.5 V with feedback resistance [Sexton1989].

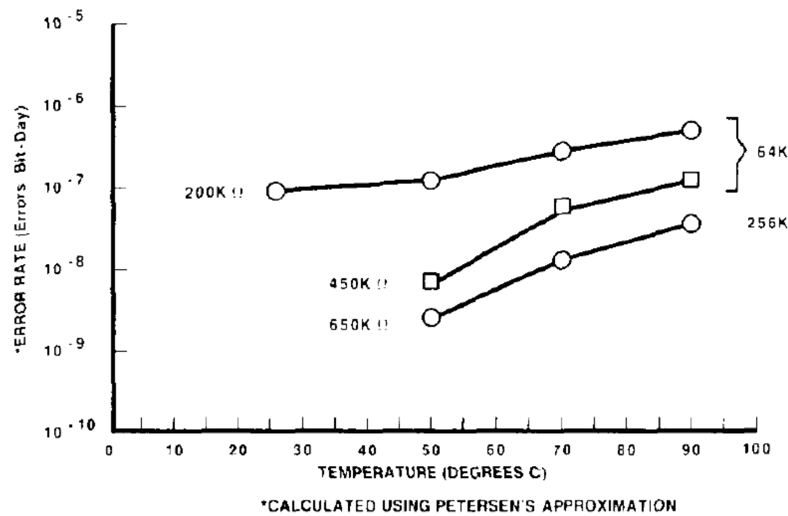


Fig. 1.21. Temperature dependence of the error rate in rad-hard SRAMs having different values of feedback resistances [Sexton1989].

on the Soft Error Rate (SER), among which [Heijmen2006] [Sexton1989] [Truyen2007].

Some of them [Heijmen2006] conclude that operating temperature only plays a marginal role (less than 3% over the range T = - 40 to 125°C) in determining the critical charge in SRAMs.

Much older are the experimental data reported in 1989 by Sexton *et al.*, who observed an increased SEU sensitivity at high temperature in hardened memories, as illustrated in Fig. 1.20, where the heavy-ion cross section of a rad-hard SRAM is plotted as a function of temperature [Sexton1989]. The authors attributed the temperature dependence to variations in the conductivity of the feedback and load resistors: this is clear in Fig. 1.21, where the SER is shown as a function of temperature for SRAMs having different values of feedback resistances and displaying different responses to radiation.

Truyen *et al.* recently performed a number of TCAD simulations of heavy-ion strikes in 180-nm 6-T SRAM cells as a function of temperature [Truyen2007]. In this contribution, based on the simulation results, temperature is shown to have a significant impact on the characteristics of heavy-ions-induced current transient. Fig. 1.22 depicts the simulated drain current induced by a heavy ion with LET = 2 MeV/cm^2/mg impinging at normal incidence on the drain of the off-NMOSFET, at different temperatures. As observed in the figure, the magnitude of the current peak decreases with increasing temperature, while the transient duration increases at high temperatures. Truyen and coworkers also performed an analysis of the electrical characteristics of the memory cell as a function of temperature and the main result is reported in Fig. 1.23: the upset voltage (i.e., the voltage perturbation that is necessary to trigger an bit flip) decreases with increasing temperature. As a result, putting together the results shown in Fig. 1.22 and in Fig. 1.23, it is clear that the influence of temperature on the SEU sensitivity is given by the combination of:

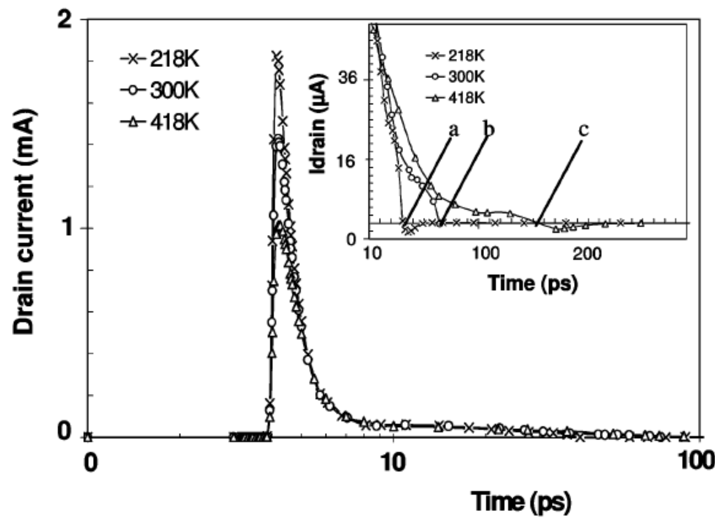


Fig. 1.22. Temperature dependence of the time evolution of the drain current transient, for a track located in the off-NMOS drain generated by a heavy-ion with LET value equal to 2 MeV/cm^2/mg [Truyen2007].

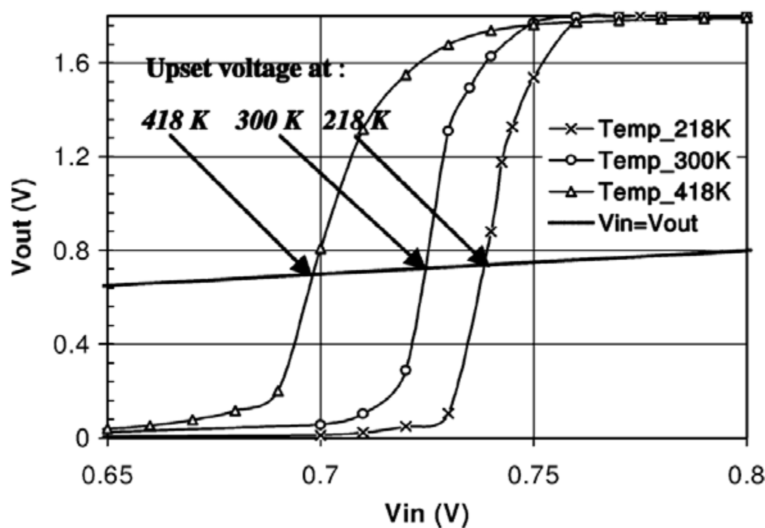


Fig. 1.23. Temperature dependence of the DC transfer characteristics obtained with device simulation of the SRAM cell [Truyen2007].

(i) the drain current peak dependence on temperature

(ii) the upset voltage dependence on temperature.

As a result, the cell SEU sensitivity displays a parabolic dependence on temperature due to the competition between factors (i) and (ii), as depicted in Fig. 1.24, where the threshold LET is plotted versus temperature. The authors conclude that, although the temperature dependence of the transient current is strong (the drain current peak varies up to 60% in the range 218-418 K), the SEU susceptibility only weakly depends on temperature, with a small variation (see Fig. 1.24).

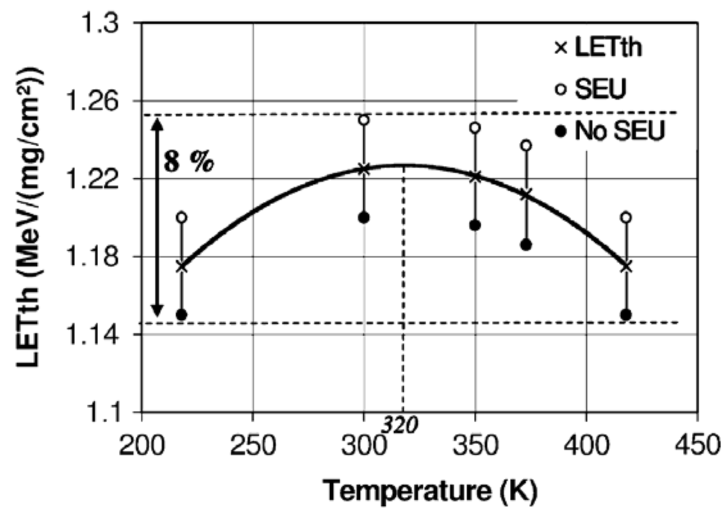


Fig. 1.24. Temperature dependence of the DC transfer characteristics obtained with device simulation of the SRAM cell, for a heavy ion track located in the off-NMOS drain [Truyen2007].

Finally, a few reports describe temperature effects in devices other than SRAMs. For instance, experimental work has been performed on pn diodes using a heavy-ion microbeam, demonstrating that the shape of the particle-induced current pulse changes with temperature [Guo2004] due to variations mobility and lifetime of the carriers. Recently, Laird *et al.* analyzed the temperature dependence of transients in inverters, through laser testing [Laird2008].

To the best of our knowledge, few experimental SER data as a function of temperature are available in the literature for SRAMs operating in the terrestrial radiation environment. However, the topic is worth to be explored, due to the huge number of electronic applications that must operate at high temperatures, not only at sea-level but also in hostile environments such as space.

Chapter 2

TID Effects in NAND Building Blocks

Commercial Flash memories are extensively used in a variety of applications in the terrestrial environment. In addition, they are arousing increasing interest for the possible employment in space and satellite electronics, but also in high-energy physics and nuclear experiments, where the presence of protons, x- and γ-rays can be massive.

Besides the extremely harsh environments like space and nuclear power plants, Total Ionizing Dose (TID) effects should be evaluated, even though at much lower levels, on earth, for instance in airport or food checks, or during PCB inspections in the board assembly processes.

Unfortunately, Flash memories are pretty sensitive to TID effects and the study of radiation issues may be complicated by the lack of (or limited) manufacturing information on the tested devices. Furthermore, technology scaling is not bringing so much benefit to TID susceptibility in Flash devices as for the world of low-voltage CMOS circuits.

The purpose of this chapter is to systematically study the radiation sensitivity of a NAND Flash in terms of Total Ionizing Dose. The role of each memory functional block (floating gate array, charge pumps, row decoder) in determining the whole device susceptibility will be experimentally assessed and discussed with respect to the different error signatures and failure modes.

2.1 Devices

For this work we used commercial 1-Gbit NAND Flash memories manufactured by STMicroelectronics/Numonyx (part number NAND01G-B2B) in a 90-nm CMOS process, with two different supply voltages, 1.8 V and 3 V. The results obtained for the parts with the two supply voltages were nearly identical since the only difference between the two device types is the presence of an internal voltage regulator, whose performance was not (or negligibly) influenced by irradiation in our tests.

Before introducing radiation-induced errors, the architecture of NAND Flash memories will be briefly described. The following description is valid in general, although the reported numbers refer to the specific devices we studied in this work.

Fig. 2.1 shows a schematic organization of the functional blocks in the device that are involved in read operations. The floating gate (FG) storage array is made of 1024 blocks. A single block contains 64 pages, each taking half a word line. Bit lines span across multiple blocks terminating on the control circuitry. A string made of 32 floating gate transistors is enclosed between two devices connected to the Drain Selection Line (DSL) and Source Selection Line (SSL). DSL and SSL transistors are used to select a string and read a single device in the string. Before being input/output to the pins, the Flash cell analog level is translated into 0/1 digital data by using the Page Buffer (PB) read circuit, then the data are temporarily stored into the PB, made of 16,896 latches (corresponding to the 2,112 bytes in each page). For instance, during a read, the content of a whole page is transferred in parallel from the FG to the page buffer, from which it is serially output (8-bit at a time) to the device pins, at each positive transition of the read signal.

Fig. 2.2 shows a complete sketch of the device functional blocks. A Row Decoder (RD) addresses the requested block and page in the memory array. An embedded microcontroller controls the sequence of operations that are necessary to perform read, program, and erase, signaling possible errors through the Status Register (SR, which is a low active signal). In addition, the Ready/Busy (R/B) signal indicates if a read/program/erase operation is in progress. It is worth to highlight that the code for this microcontroller is hard wired so that firmware corruption due to impinging radiation is very unlikely.

Finally, charge pump circuitry consists of large capacitors and diodes that are used to internally generate the high voltages (up to 15 V) needed for the program and erase operations, and, in modern devices, also for read operations. In particular, there are three different charge pumps:

i) The *read pump* is used to generate the voltages needed to read the array and to verify the correctness of the program/erase operations. Note that operating voltages of the memory core do not scale as expected for logic or for static memory, because the scaling of the tunnel oxide in non-volatile memories is very slow due to data retention issues.

ii) The *program pump* is used during program and erase operations. This circuitry generates the high voltages needed to inject charges through the tunnel oxide by

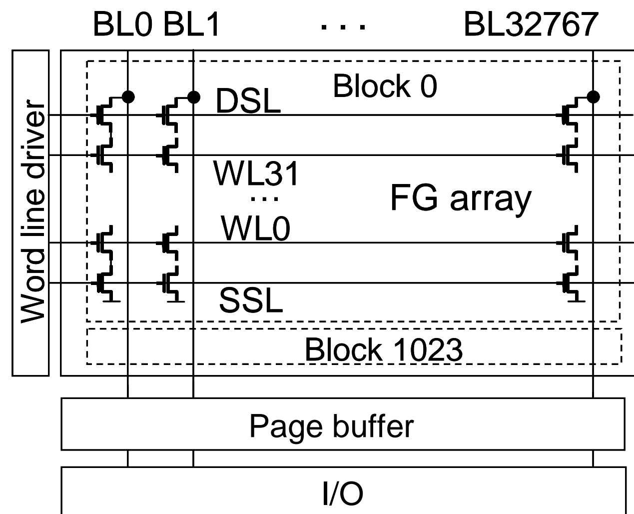


Fig. 2.1. NAND Flash memory sketch showing the main functional blocks that are involved in read operations: Floating Gate memory array, Page Buffer, and I/O circuitry.

means of Fowler-Nordheim tunneling. Voltage is applied to different terminals of the FG transistor in order to inject/remove excess carriers from the FG.

iii) The *pass pump* is used during program and erase operations to prevent the injection of charge in unwanted cells belonging to the same word line as those being programmed/erased.

2.2 Irradiation and experimental

The devices were irradiated with a 10-keV x-ray source at the INFN Legnaro National Laboratories, Padova (Italy), with a dose rate of 100 rad(Si)/s. Dose rate uniformity was within 5% over the device area. Irradiations were performed in 10 s or 50 s steps on idle samples under bias. After each step, corresponding to 1 krad(Si) or to 5 krad(Si), the devices were measured performing either:

i) a read operation on one or more memory blocks that were previously programmed (to all '0') or erased out of the beam (in the following referred to with *Read Cycle*)

ii) or a sequence of Erase/Read/Program/Read operations on selected blocks (*ERPR Cycle*).

During these tests the number of errors (with their physical location), the Status Register, and the charge pump output waveform (accessed through reserved test mode routines) were monitored. To classify the various types of observed errors and understand their origin, we selectively protected part of the device with movable copper shields during irradiation. Modular shields were combined and aligned with a microscope in order to protect the

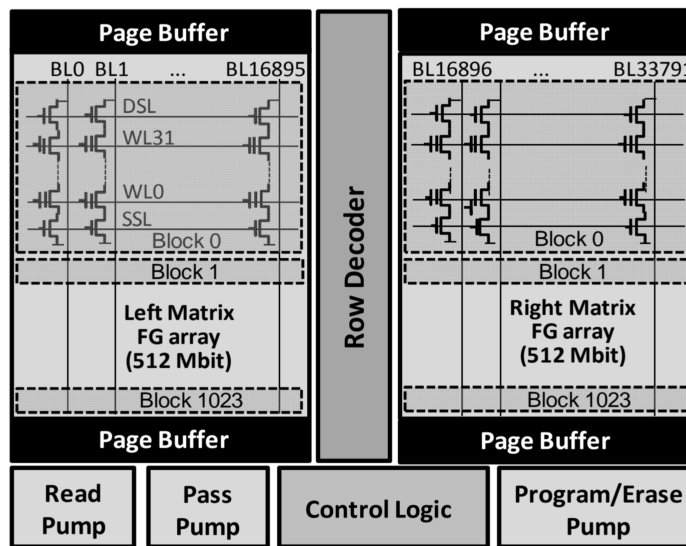


Fig. 2.2. Functional blocks in a modern NAND Flash memory.

different functional device blocks. The thickness of these shields has been calculated in order to virtually reduce to zero the dose to covered device parts. We exposed the shields on top of a dosimeter film, confirming that the dose underneath the chosen copper layer was negligible.

Note that the TID response of complex devices may depend on the energy of the incoming radiation, due to changes in charge yield and to dose enhancements phenomena (due to the presence of high-Z materials). For this reason, ^{60}Co γ-rays are usually the standard benchmark. However, x-rays is a much more effective source for the sort of study we are carrying on than ^{60}Co because it allows selectively shielding of the device, that would be impossible to perform with γ-rays.

2.3 Radiation test results and discussion

Several irradiation runs have been performed to assess the failure dose and the peculiar degradation characteristics of the different functional blocks of the NAND Flash devices. In the following sections, we will present the sensitivity of the FG array, the charge pumps, and the row decoder, going from the most to the least sensitive.

2.3.1 Floating Gate array

If we irradiate the devices shielding all the peripheral circuitry, leaving only the FG memory array exposed to x-rays, and performing a Read operation (i) after each dose step, we observe read errors starting from 55 krad(Si) and gradually increasing as a function of the received dose. Fig. 2.3 shows the progressive buildup of raw bit errors during x-ray exposure

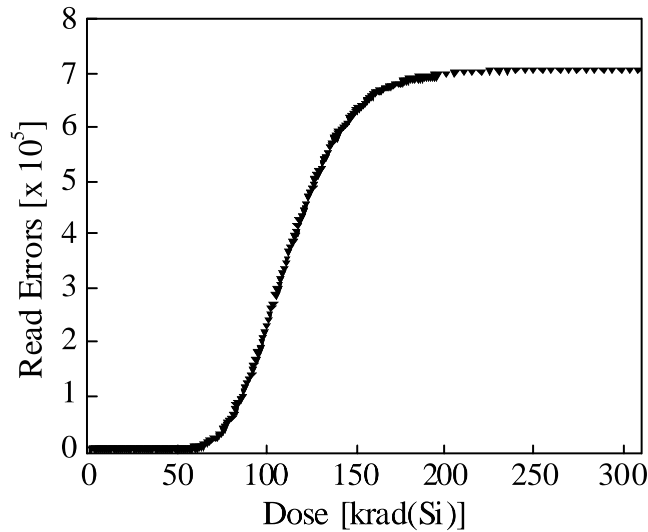


Fig. 2.3. Bit error evolution as a function of the received dose during x-ray irradiation, shielding all the peripheral circuitry for a programmed block ('0'). The number of bit errors (i.e., bit that are read as erased) saturates to the total number of bits exposed to radiation.

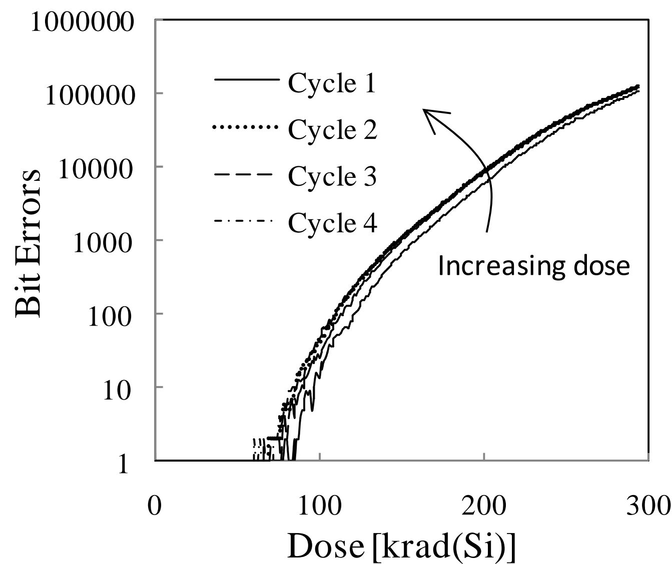


Fig.2.4. Number of errors in the programmed cells ('0') as a function of total dose exposing to x-rays only the FG array. The devices were erased and programmed at '0' at the beginning of each irradiation cycle.

for a block that has been programmed to "all 0" prior to irradiation. The physical locations of the errors are randomly distributed in the array, as can be verified through the scrambling information provided by the manufacturer. This implies that no proximity effect is present, i.e., the error probability of a cell does not increase if a neighbor FG cell fails. As seen in Fig. 2.3, the number of errors monotonically increases and saturates around 200 krad(Si) to the total number of cells exposed to radiation. Note that this number is smaller than the

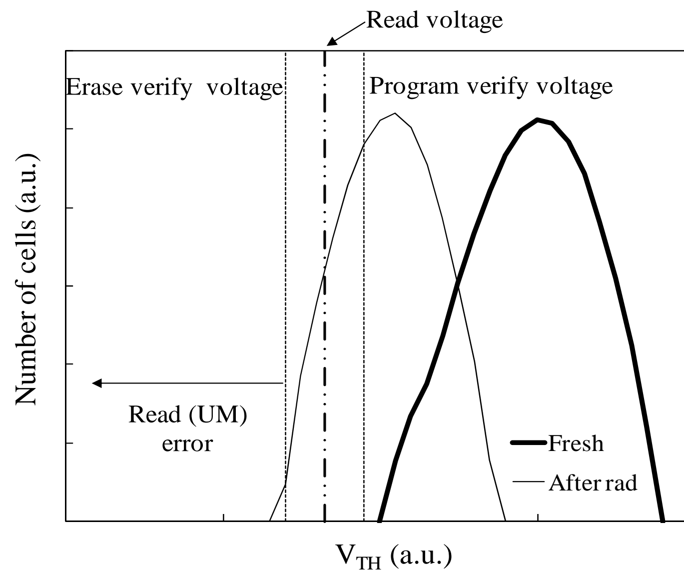


Fig. 2.5. Sketch of the mechanism leading to read errors in the FG array. The distribution of programmed cells shifts towards lower V_{th} voltages after TID exposure. Depending on the position of the shifted distribution, some FG cells will be erroneously read as erased.

number of bits in a block because some cells are unavoidably covered by the copper shields. In other words, after ~ 200 krad(Si) all exposed FGs are read as erased ('1'). At the end of the exposure, we checked the charge pumps with both user-mode (functionality of program, erase, and read operations) and test-mode routines (pump output voltage) and found that the pumps work properly, confirming that shielding was effective.

These raw bit errors happen only when the threshold voltage (V_{th}) of a programmed FG changes enough to cross the user mode read level (0 V for this SLC NAND devices) and to enter the erased FG cells distribution. In detail, the V_{th} distribution moves during irradiation because of the progressive discharge of the FGs and positive charge trapping in the oxides that surround the FG [Cellere2004a] [Cellere2005a] [Cellere2007b]. An experimental evidence showing that the oxides surrounding the FG feature charge trapping due to irradiation is displayed in Fig. 2.4. The graph illustrates the number of raw bit errors found in subsequent irradiation cycles (again, shielding all the peripheral circuitry): at the end of each cycle, the array was erased and programmed again. In this way, we found that the progressive accumulation of dose results in decreasing dose for discharging the same number of FG cells, likely indicating positive charge trapping in the cell oxides (tunnel oxide, STI, ONO).

A qualitative explanation of the threshold voltage shift leading to a raw bit error is reported in Fig. 2.5. When the V_{th} of a given cell goes below the so-called program verify voltage (shown in the figure with a vertical dashed line), there is no guarantee that the cell will be read as programmed. However, the cell will be certainly read as erased when its V_{th} becomes lower than the erase verify voltage, which defines the erased state. The read voltage lays between the erase verify and program verify levels, and in our case can be considered as

the “failure” voltage. The actual value of these voltages is confidential and depends on the selected technology, but the physical mechanisms are the same for all FG technologies.

This description allows us to understand some details of the experimental results. First of all, let us remark that variations in V_{th} occur before 55 krad(Si) [Cellere2004a], but these variations are simply not detectable in user mode (Fig. 2.3 shows the number of raw bit errors). The cells more prone to fail are those programmed at the lowest values of V_{th} (that is, those at the left end of the programmed distribution, see Fig. 2.5).

In addition, errors are detected only in the programmed cells, that is, for ‘0’ (i.e., FGs are filled with electrons, V_{th} is “high”). On the contrary, up to 1 Mrad(Si) we found no errors in the erased blocks (‘1’, FGs are filled with holes, V_{th} is “low”). This may seem in partial contrast with the results of previous work [Cellere2004a], where shifts in both programmed (‘0’) and erased (‘1’) cells were detected, and in agreement with other reports such as [Oldham2006], where only bit flip in the 0 → 1 direction are reported. However, the discrepancy is only seeming and can be reconciled knowing that the intrinsic V_{th} is negative[1] (possibly corrected by the radiation-induced trapped charge), i.e., an empty floating gate is read as erased (‘1’), instead of positive as was for example in [Cellere2004a], where NOR memories were considered. As a consequence, the erased cells deprived of holes by irradiation are still read as erased. Concerning this aspect, it is important to highlight the fact that while virtually all commercial FG NAND technologies share the same architecture and principles, the actual value of the intrinsic V_{th} depends on the specific implementation of the technology. So, errors in the ‘1’ to ‘0’ direction in devices from a different manufacturer (or even in a different technology) can not be excluded. Further, in large arrays (4 Gbits or more) it is impossible to control the intrinsic V_{th} down to the third significant digit, so that this parameter will be characterized by a distribution, rather than by a fixed value. Of course, it is in manufacturers’ interest to keep this distribution as compact as possible in order to guarantee high yield and reliability. However, when dealing with a large array and not with the portion of a single block, it is likely that some of the FGs may have an intrinsic V_{th} slightly larger than 0 V instead than slightly lower. These FGs feature a peculiar behavior with respect to the remaining of the array. In NAND devices an external ECC is always needed, so we expect the overall device reliability to be dominated by the behavior of the majority of the FGs, not by that of extreme cases.

2.3.2 Charge Pumps

If during *Read Cycles* we expose to x rays also the charge pump circuitry, in addition to the FG array, we observe the same behavior as the one described before (cf. Fig. 2.3) up to ~ 100 krad(Si), and a different one from 100 krad(Si) onwards. In fact, after 100 krad(Si), programmed cells start to be correctly read as programmed (Fig. 2.6), while erased cells start to be read as programmed (Fig. 2.7). As depicted in Figs. 2.6-2.7, after 120 krad(Si), we

[1] Please note that the shift of the intrinsic V_{TH} due to charge trapping in the tunnel oxide and in the interpoly dielectric has to be taken into account.

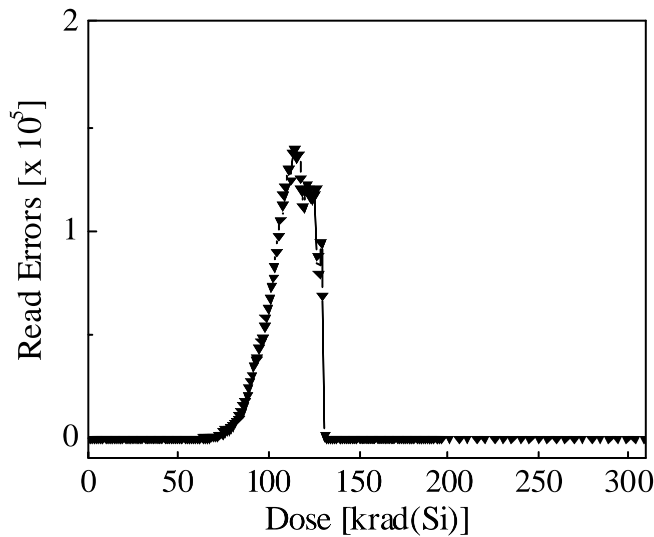


Fig. 2.6. Raw bit errors as a function of the received dose during x-ray irradiation, exposing only the FG array and the charge pumps for a programmed block ('0').

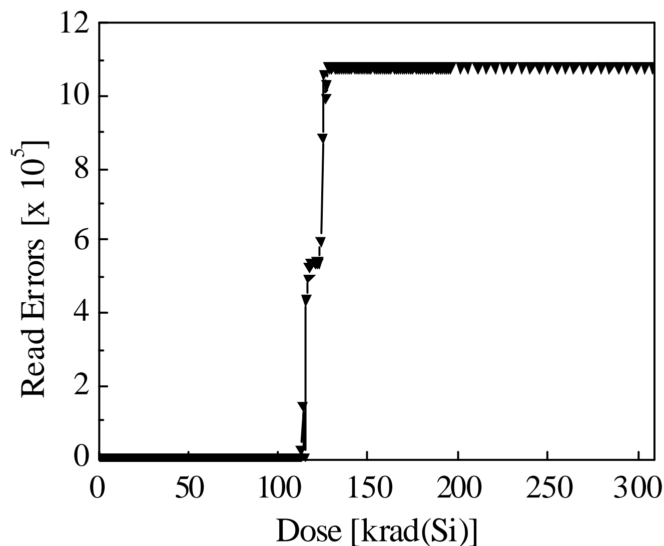


Fig. 2.7. Bit error evolution as a function of the received dose during x-ray irradiation, exposing only the FG array and the charge pumps (same conditions as Fig. 2.14) for an erased block ('1'). The number of bit errors saturates to the total number of bits in a block (1,081,344).

read all the FGs as programmed, regardless of their actual program condition.

This effect can be attributed to a reduction in the voltage available from the read charge pump. In fact, in the NAND architecture, a FG cell is read by applying 0 V to its gate, and biasing all the other cells belonging to the same series of 32 FGs to a voltage (V_{READ}) high enough to guarantee that both erased and programmed cells are turned on. As previously described (cf. Section 2.1.1), this voltage is generated through a dedicated charge pump (read pump). If the voltage provided by this element is lower than designed (i.e., it is not sufficient to turn on even a single transistor in one string, including SSL and DSL

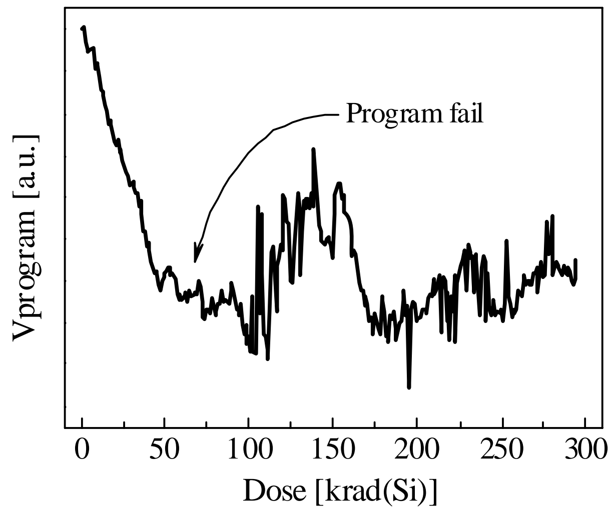


Fig. 2.8. Average voltage generated by the program charge pump as a function of x-ray dose. The voltage is normalized to the one of the fresh device (0 krad). Program fail indicates the failure of the Status Register after a program operation.

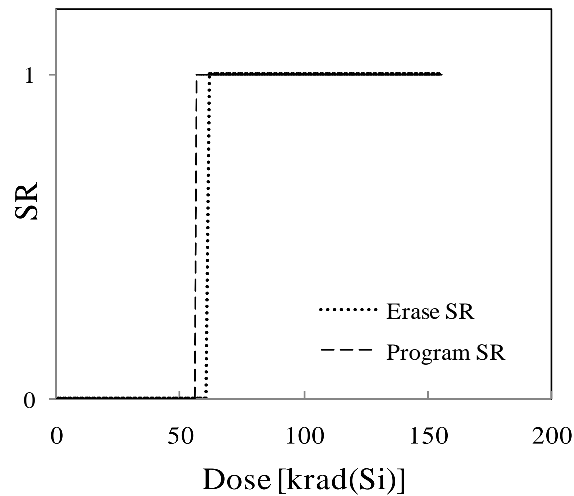


Fig. 2.9. Logic value of the device Status Register signalling the correctness (SR = 0) of the program and erase operations during ERPR Cycles under x-ray exposure, as a function of the received dose.

selectors), all the cells in the string will be read as programmed (no current will flow), regardless of their actual status. This is the likely cause of the sudden drop in the apparent number of errors after 100 krad(Si) in Fig. 2.6 ('0'), and of the abrupt increase in the number of errors in Fig. 2.7 ('1'). In more detail, all FG cells in Fig. 2.6 are programmed at '0', so in this case we do not know which is the transistor which is not turned on (that is, one of the FG MOSFETs in the string, or one selection transistor, either SSL or DSL).

However, in Fig. 2.7, FGs are erased ('1') and, as already discussed, FGs programmed in this status never achieve a V_{th} larger than 0 V. Hence, even if the charge pump were generating 0 V, all FGs in the string would be on. This demonstrates that the charge pump

voltage drops below the level needed to turn on one of the two selection transistors (SSL or DSL), explaining the behavior in Fig. 2.7. Also note that in both Fig. 2.6 and 2.7 we can distinguish a two-step behavior: at first, half of the FGs are read as ‘0’, then the same happens to the second half. This puts in evidence a different sensitivity of the two half planes of the memory array.

Experimental evidence of charge pump degradation is shown in Fig. 2.8. This figure illustrates the output voltage of the program charge pump during *ERPR Cycles*. This test mode allows us to measure the voltage waveform output by the program pump (V_{PROG}) when programming a page in the memory array (injecting electrons in the FG). This way, we can measure the degradation of the program pump output voltage at different dose steps. The average voltage generated by the pump linearly decreases up to 50 krad(Si). Despite this, the device appears able to correctly program and erase until 60 krad(Si), when the device Status Register signals failures in the program operation.

The failure of the SR is indicated in Fig. 2.8 with an arrow and more clearly illustrated as a function of the received dose in Fig. 2.9, which displays the logic values of the Status Register detected after erase and program operations, during *ERPR Cycles* under x-ray exposure.

The voltage generated by the charge pump circuitry can be degraded because of V_{th} shifts in the pass transistors and leakage increase due to charge trapping in the Shallow Trench Isolations (as shown in [Faccio2005] after TID exposure and in [Gerardin2006] after heavy-ion irradiation).

Fig. 2.8 refers to the program pump but similar considerations apply to the read pump as well, even though the failure dose is higher in the second case [100 krad(SiO_2) vs. 60 krad(SiO_2)]; this is due to the lower voltage generated by the read pump with respect to the program one [Nguyen1999]. The higher hardness of the read pump is likely due to the fact that variations in the E/P pump voltage are more critical than in the read pump. Indeed, the E/P pump voltage is used to trigger injection mechanisms that exponentially depend on voltage, while the read pump is used to turn on FG cells, for which the bias dependence is weaker.

Finally, it is important to note that the charge pump was never activated during x-ray exposure, so an even worse degradation can be expected performing program operations during irradiation [Nguyen1999].

2.3.3 Row Decoder

The final experiment presented here is done by shielding the charge pump circuitry and leaving the FG array and the row decoder exposed to radiation. For doses up to about 130 krad(Si), the memory behavior during *Read Cycle* is similar to that presented in Section 2.3.1) (only FG cells exposed to x rays), but a peculiar behavior emerges at higher doses due to the degradation of the row decoder.

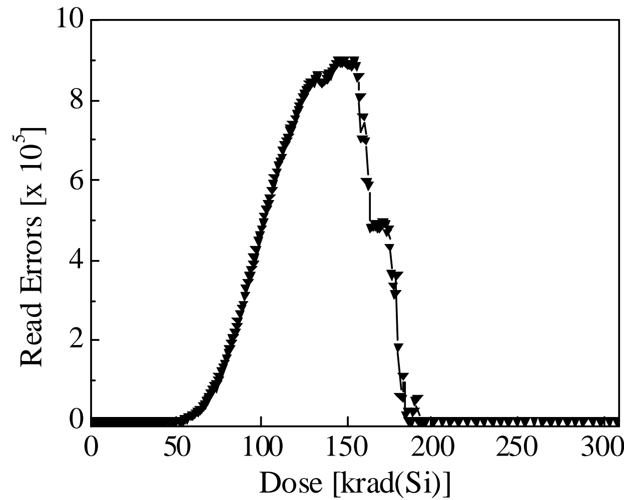


Fig. 2.10. Raw bit error evolution as a function of the received dose, during x-ray exposure of FG array and Row Decoder for a programmed block ('0').

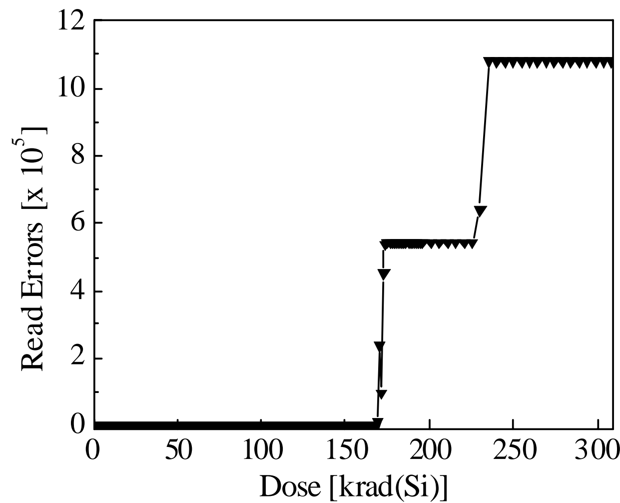


Fig. 2.11. Raw bit error evolution as a function of the received dose, during x-ray exposure of FG array and Row Decoder for an erased block ("1"). The number of bit errors saturates to the total number of bits in a block.

Fig. 2.10 displays the evolution of the number of raw bit errors in the programmed cells. In the first part of the curve, up to 130-150 krad(Si), the behavior is very similar to that of Fig. 2.3, and we observe the same increasing trend, with errors randomly distributed across the FG array. Afterwards, from 150 to 200 krad(Si), a sudden step-like decrease occurs and, from 200 krad(Si) on, we detected no more errors. Errors disappear first in one half of the array and then in the other half. In addition, after 150 krad(Si), we detect errors also in the erased cells (all '1') (Fig. 2.11). Similar to the trend observed in Fig. 2.7, the increase is not gradual, but is step-like, and, again, from the physical maps we learn that the errors appear first in one half of the array [around 175 krad(Si)] and then in the other half

[around 225 krad(Si)]. In other words, we read all the cells as programmed, regardless of their program condition before irradiation.

This effect is very similar to that caused by the charge pump degradation, even though it happens at higher doses. Given the exposure conditions (only array and row decoders are exposed) and the behavior described so far, this effect has to be attributed to radiation damage to the addressing circuitry. Different parts of the Row Decoder may be responsible for these errors. The fact that all the cells are read as programmed indicates that some transistors that should be turned *on* are actually *off*, or that leakage too rapidly discharges some nodes that were pulled high, thus impeding current to flow through the string of 32 FGs. In particular, one or more of the following conditions may occur:

- SSL and/or DSL are not operational (as seen in Figs. 2.1-2.2, the FG chain remains open if the SSL and/or DSL are not turned on);
- the gate of the cell to be read is not grounded due to failure in one or more pass transistors;
- a voltage lower than V_{READ} is applied to the transistors in series to the cell to be read.

The observed failure in one half-plane and then in the other is highly indicative of damage in the local row decoders controlling each of the two half planes. Increase in leakage current or change in the V_{th} of transistors even at TID lower than those used here are expected since the single ended program voltages used by NAND memories require very thick (~ 35 nm) oxides, which is prone to charge trapping and interface state formation. Their NOR counterparts feature thinner oxides (intrinsically harder), but also more complex control circuitry.

2.4 Summary

An experimental study of TID effects in NAND Flash memories has been presented. The adoption of these devices in the space and satellite industry is made difficult by the fact that they feature a very complex structure, which is hidden to the final user. In this sense, it is essential to understand which of the different elements is the most vulnerable to ionizing radiation, and its peculiar degradation characteristics. This is useful, for instance, in order to design a rad-tolerant or rad-hard part, but also, to design a radiation hard sub-system which uses commercial FG memories.

The approach we used here was to begin irradiations with all the control circuitry shielded, and then adding to the exposed portion the charge pumps and the decoders. As TID builds-up, read errors first appear due to charge loss and charge trapping in the FG cell, then due to the charge pump output voltage reduction, and finally due to row decoder failure. TID issues in the peripheral circuitry are exacerbated by the use of thick gate oxide, for cost saving reasons.

If we now go back to the question posed at the beginning of this section (how to design a rad-hard memory or memory subsystem), these results can give some preliminary but important indications. In fact, FG cell array is the first block to fail during irradiation. All phenomena leading to charge loss from programmed FG and charge trapping in the cell oxides are linked to the basic physics of the FG MOSFET [Cellere2004a] [Cellere2005a]. Hence there is nothing one can do if not scrubbing the memory, detecting possible errors, and rewriting the exact values in the array. NAND memories help somewhat from this point of view since they need ECC even for normal uses. However, the usefulness of ECC is limited since it only works for isolated errors, and it is clear from the experimental data that the number of errors steeply increases after the first ones begin to show up (see for instance Fig. 2.3).

The dose after which we detected FG errors is relatively high [55 krad(Si)], and dose enhancement effects have been reported in FG MOSFETs during x-ray irradiation [Cellere2007b], so that the cited 55 krad(Si) is likely a conservative estimation that may exceed the sensitivity under ^{60}Co γ-ray exposure.

Concerning the failures of the control circuitry, there is little one can do at the sub-system level. In fact, modern devices are black boxes where no internal signal is accessible without the use of reserved test-mode routines. For instance, up to a few years ago it was possible to externally provide the program/erase voltage. However, these operating modes are no more available if not with peculiar limitations (i.e., high speed factory program). Hence, the only way to cope with control circuitry-related issues appears to be working on the device design and technology which is probably too expensive for any niche application.

Chapter 3

Heavy-ion Induced SEE in NAND Memories

As we saw in Chapter 1, Flash memories are quite sensitive to heavy-ion strikes, that are a constant presence in the space environment. Furthermore, being complex devices, some aspects of their response to radiation are not straightforward to understand. Depending on the operating condition and other factors, as we will see in detail in this section, the sensitivity of the floating gate array, or that of the peripheral circuitry can play a key role in determining the device response to heavy ions.

The purpose of this chapter is to study the sensitivity to Single Event Effects of a NAND Flash memory. The importance of the floating gate array, page buffer, and microcontroller in determining the overall device heavy-ion sensitivity will be discussed and an 'effective cross section' will be presented.

3.1 Devices

For this study we used commercial 1-Gbit NAND Flash memories manufactured by STMicroelectronics/Numonyx (part number NAND01G-B2B) in a 90-nm CMOS process, with two different supply voltages, 1.8 and 3 V. The parts with the two supply voltages were nearly identical since the only difference between the two device types is the presence of an internal voltage regulator, whose performance was not (or negligibly) influenced by irradiation in our tests.

The devices are the same that we used in Chapter 2 for TID experiments and for a detailed description of the samples, the reader is referred to Section 2.1.

3.2 Irradiation and experimental

The irradiations have been performed with heavy ions at the SIRAD beam line of the TANDEM accelerator at the Laboratori Nazionali di Legnaro, INFN, Padova (Italy) [Wyss2001] and at the RADEF beam line at Jyväskylä University (Finland) [Virtanen2007]. We also irradiated the memories with 5.4-MeV alpha particles emitted by a portable ^{241}Am source which is available at the Department of Information Engineering at the University of Padova.

Table 3.I reports the ion species with the corresponding LET, energy, range, and facility. The LET coefficient measures the amount of energy deposited per unit length in a given material, which, in turn, determines the number of electron/hole pairs created per unit length. On the other hand, the range measures the distance travelled by the particle in the target material. Note that, due to the limited range of heavy ions in silicon (few tens of μm), the memory die has to be fully exposed to radiation and this was possible thanks to the de-lidded package provided by Numonyx.

All irradiations were performed at normal incidence and at room temperature. The test set-up we used for this work was developed in collaboration with STMicroelectronics. The test board allowed us to use both User Mode routines (i.e., those routines that are available to the end user) and Test Mode routines (such as the monitor of the charge pump output voltage). We performed our experiments under three different operating conditions, corresponding to different operating scenarios that are encountered by devices during space missions:

1. Irradiation of unbiased devices previously programmed out of the beam (static test).
2. Continuous read operations under irradiation (dynamic reads) on devices previously programmed out of the beam.
3. Program/Read/Erase/Read cycles under irradiation (dynamic program/erase).

It is worth to remark that all the read operations were performed without applying Error Correction Codes (which are strictly required for NAND Flash memories).

Ion species	Energy [MeV]	Surface LET in SiO_2 [$MeVcm^2/mg$]	Range in Si [μm]	Facility
He	5.4	0.64	27.3	^{241}Am source
Ne	186	3.75	150	RADEF
Si	157	8.59	61.5	SIRAD
Ar	372	10.72	118	RADEF
Fe	523	19.49	100	RADEF
Ni	210	28.14	33	SIRAD
Kr	768	32.12	96	RADEF
Br	250.3	40.88	32	SIRAD
Xe	1217	56.35	97	RADEF
Ag	266.2	57.34	28	SIRAD

Table 3.I. Description of the heavy ions used for irradiations

3.3 Experimental results and discussion

In this section we will evaluate and discuss the features of page buffer and floating gate errors, the functional interruptions, and finally we will introduce an 'effective cross section' which accounts for the contribution of the main building blocks as a function of the operating conditions.

3.3.1 Page Buffer and Floating Gate errors

The first test we carried out consisted in periodically reading the content of one or more programmed (i.e., filled with zeros) memory blocks exposed to a constant flux of particles (scenario 2., dynamic read). In the "0" state (programmed), excess electrons are stored in the floating gate, thus increasing the FG transistor threshold voltage, V_{th}. We chose this program pattern since this state is usually the more radiation-sensitive, because of the larger electric field in the tunnel oxide [Cellere2001]. A linear build-up of errors is initially observed, which may be followed by sudden bursts of errors (Single Event Functional Interruption, SEFI), and usually ends up with a non operating device, until a reset or a power-cycle is performed. As shown in Fig. 3.1, before the mentioned SEFI, the number of raw bit errors (i.e., without ECC) linearly depends on the ion fluence. The new errors which are observed after each read operation belong to two categories: some of them appear only once (i.e., they disappear at the following read operation), while others are present from a

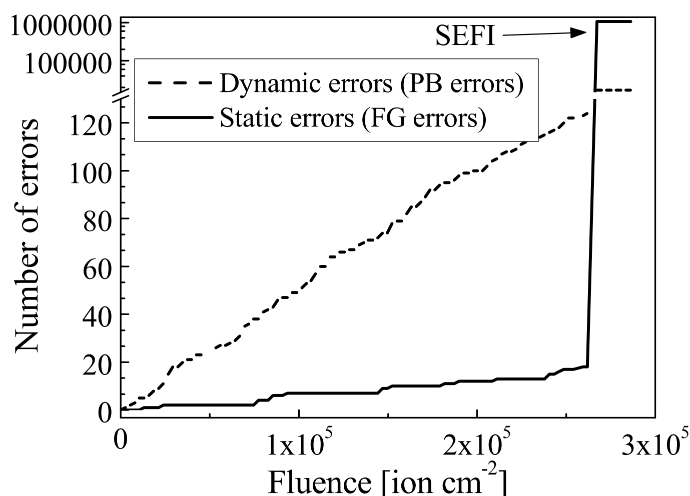


Fig. 3.1 Temporal evolution of dynamic (PB) and static (FG) errors during repeated reads of a memory block under Bromine beam (flux 150 ions/cm^2/s), as a function of the ion fluence. After $2.5 \cdot 10^5$ ions cm^{-2}, a SEFI occurs and a sudden burst of errors is observed.

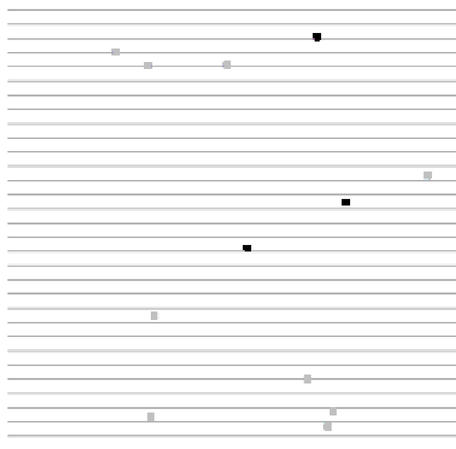


Fig. 3.2. Physical distribution of the bit-flips inside a block relative to Fig. 3 (at very low fluences). Gray dots are PB errors, black ones FG errors. The block word lines are split into several parts (separated by grey lines) and the dots representing errors are enlarged for ease of visualization.

given read cycle on, and remain even after a reset or a power cycle, but they disappear when the device is reprogrammed. Fig. 3.1 shows the temporal evolution of the errors during Bromine ion irradiation (with a flux of about 150 ions/cm^2/s), as a function of the particle fluence.

This behavior is in agreement with previous reports [Nguyen2003] [Oldham2006], which showed the existence of "dynamic errors" that disappear from one read to another[1],

[1] Note that definitions commonly used in literature can be misleading. In particular, while it is true that dynamic errors can appear only during dynamic read test (with unbiased devices errors can happen in the FG array only),

and "static errors" that can be corrected only by reprogramming the device. Whereas in literature dynamic errors were attributed to the peripheral circuitry, static errors were ascribed to upsets in FG cells; hence, in the following, we will call them FG errors. Thanks to confidential information provided by the manufacturer on the device architecture, we can map the observed errors to the corresponding physical locations in the memory cell array. As seen in Fig. 3.2, all these errors were randomly distributed across the block array (in the figure black points represent static errors, while grey ones refer to dynamic errors).

To fully understand the origin of the dynamic errors, we now need to review the read protocol of a NAND Flash memory and analyze the operations that occur during read. When the "read" command is issued to the embedded microcontroller, the row decoder addresses the requested page in the FG array. The page is then temporarily transferred to the Page Buffer (2112-byte static latch bank). From there, data are serially output, byte by byte, to the device pins every time the Read Enable (RE) signal is pulsed.

As the previous discussion suggests, dynamic errors can be traced back to upsets in the PB latches; in fact, reading once again the page is enough to retrieve the correct information, implying that the information actually stored in the FG has not been corrupted. To verify this conjecture, we introduced a delay (t_{delay}) between the "read" confirmation command and the transfer of the data from the memory to the output pins as shown in Fig. 3.3. Doing so, we can "freeze" the data in the PB latch for an arbitrarily long time. It turns out that the dynamic error rate grows linearly with increasing t_{delay} (Fig. 3.3), whereas the number of FG errors remains unchanged (not shown). In other words, the longer the data stay in the PB, the larger the dynamic errors rate. One can also compute the cross section of the PB (σ_{PB}), dividing the number of dynamic errors by the time the data stay in the PB. The result is depicted in Fig. 3.4: the cross section computed in this way is independent of the delay. This confirms our hypothesis on the origin of dynamic errors; we will therefore refer to them as PB errors.

Similar results can be obtained by changing the read time, for instance through the insertion of a delay before each Read Enable pulse ($t_{delay,RE}$), when outputting the data from the PB to the pins. In this case though, the time each byte spends in the PB is not constant, since the first byte is almost immediately output, while the last byte to be transferred stays in the PB for a time corresponding to $t_{delay,RE}$ times the number of bytes in the PB (2112); on average, each byte spends in the PB a time $t = t_{delay,RE} \cdot 2112 / 2$. Note that changing the time data spend in the PB is equivalent to changing the speed of the interface between the memory and the control system. Also, no matter how the read delay is introduced, it is necessary to account for the intrinsic read time (in Fig. 3.3, the interpolation line crosses the Y-axis at a larger-than-zero value). As we shall see later, the read time plays an important role in the determination of the device cross section (Section 3.3.5).

not all errors that appear during dynamic tests can be called dynamic according to our definition (errors happening in the FG cells are static).

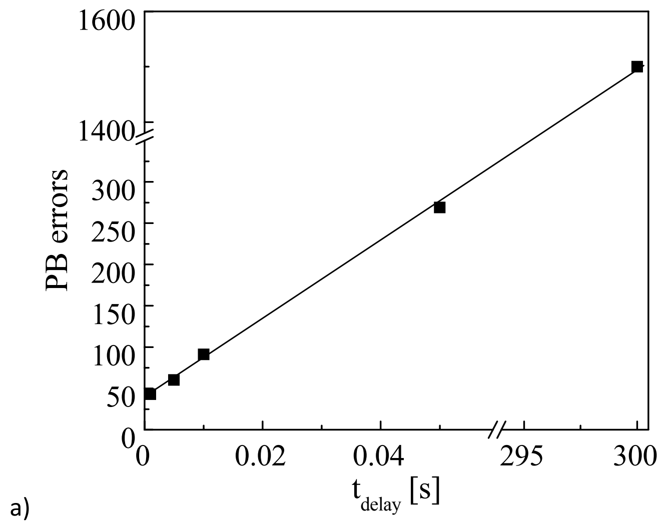


Fig. 3.3. The number of PB errors versus t_{delay} displays a linear dependence, showing that the longer the data stay in the PB, the larger the probability of PB errors.

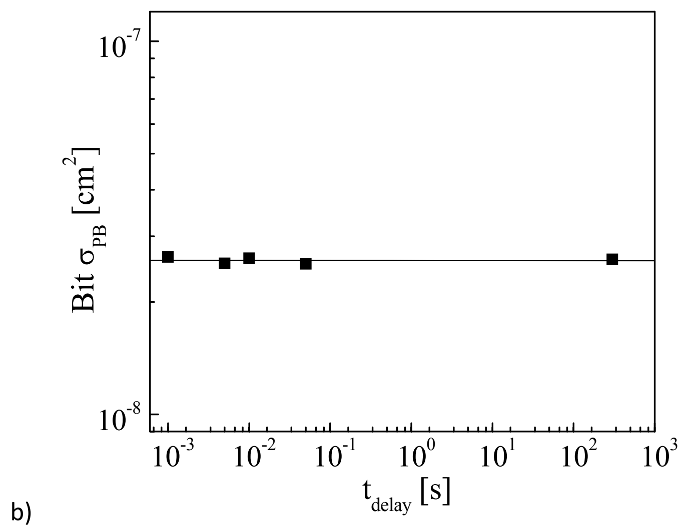


Fig. 3.4. PB bit cross section (σ_{PB}) is, as expected, independent of the delay after the read command. Both figures refer to irradiation with Silicon.

Another interesting characteristic of PB errors is their dependence on the program pattern (see Fig. 3.5). In fact, although the latches used for the page buffer are similar to 6-T SRAM cells, they exhibit some peculiar features. First of all, the design is not symmetrical for the two sides of the latch. This results in different load capacitances associated with the storage nodes of the latch, leading to different values of the critical charge required to upset the latch in the '0' and in the '1' state. In fact, as shown in Fig. 3.5, the page buffer cross section (σ_{PB}) is dependent on the stored pattern ($\sigma_{PB,1}$ is ~ 40% larger than $\sigma_{PB,0}$), no matter the ion species we used for the irradiation. Besides, to reduce the manufacturing cost, PB and

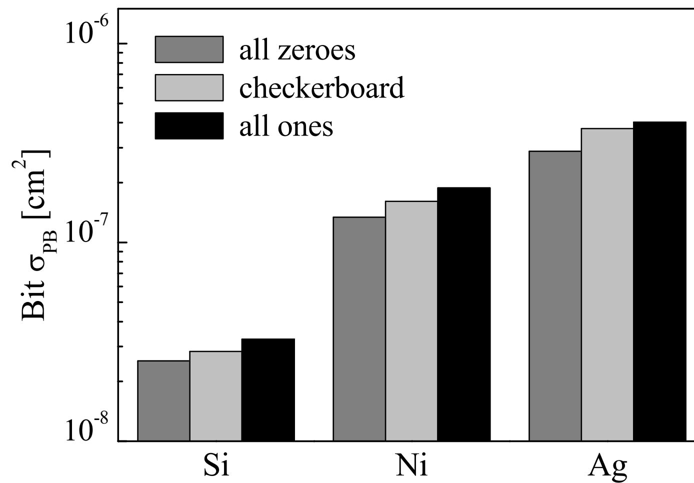


Fig. 3.5. Bit σ_{PB} dependence on the pattern stored in the memory, for irradiations with Silicon, Nickel, and Silver. For all the three ion species, the cross section per bit is higher for the cells in the '1' rather than '0' state.

all control circuitry transistors use the tunnel oxide as gate dielectric (this avoids the integration of a further thin oxide just for the logic) and have relatively large channel width and length.

As we saw up to now, the page buffer is sensitive to radiation only in the (usually short) time window between the transfer of the page content to it and until the data are serially output to the I/O pins. On the contrary, data in programmed FG cells can be corrupted at any time during the radiation exposure, no matter which operation is being performed by the device. That is why during our irradiations, we recorded FG errors both during dynamic and after static tests. As expected, these errors are randomly distributed in the memory array (see again Fig. 3.2).

Once a FG is hit by a single ion, it experiences a threshold voltage (V_{th}) shift, [Cellere2001] [Guertin2006] [Oldham2006] that, if large enough, can result in a user mode error. In this case, the information is permanently lost (even after resetting or power cycling the memory) and it can be recovered only with a new program operation on the memory cell. The mechanism lying under the discharge of the FG cell has been deeply investigated in literature [Cellere2001] [Cellere2006b] [Butt2008]. The bits affected by FG errors can be rewritten, even though there may be some issues with their long-term retention due to radiation induced leakage current [Cellere2005b]. Besides charge loss phenomena, also charge trapping may occur in the oxides that surround the FG [Guertin2006] [Oldham2006] [Schmidt2007], as we will see more extensively in Chapter 4. Some of the heavy-ion induced Floating Gate errors display peculiar features that will be investigated in the following sections.

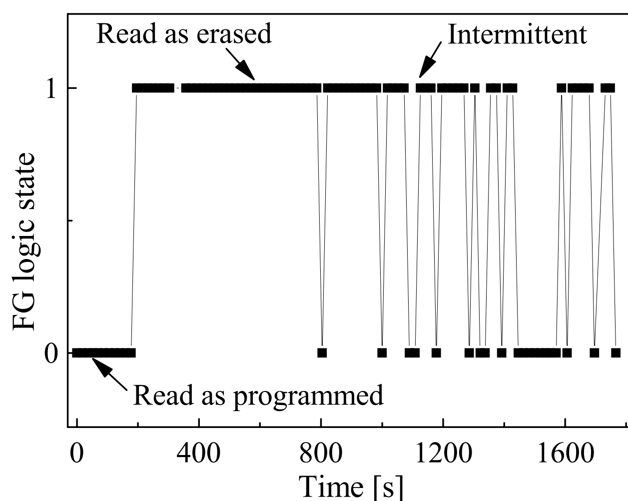


Fig. 3.6. Intermittent FG error in subsequent readings during irradiation with Bromine in a FG cell that was programmed prior to exposure. Depending on the random noise, the same cell is sometimes read as programmed and sometimes as erased.

3.3.2 Floating Gate 'intermittent' errors

Some of the FG errors (both in and out of beam) are not stable, i.e., they appear and disappear in successive read operations. Given the low flux we used (about 150 ions/cm^2/s), it is absolutely unlikely that a single cell experienced multiple hits (not even two). At any rate, a second hit would have resulted in a further discharge of the FG, and there is no reason why more electrons should be stored in the FG after a second or third strike. On the other hand, this switching behavior of the errors likely originates from a single FG cell being hit by a single ion, which caused the cell threshold voltage to about half-way between the programmed and the erased status.

As a result, depending on random noise in the readout circuitry, this bit would be read sometimes as programmed ('0'), some other times as erased ('1'). Fig. 3.6 shows, for instance, one of these "intermittent" bits (programmed out of the ion beam) detected during Bromine irradiation.

3.3.3 Floating Gate annealing errors

Other FG errors may also completely disappear after irradiation. Chapter 4 will be entirely devoted to the analysis of the FG error annealing after both heavy-ion and TID exposure, but is worth mentioning the effect here as well, to make a complete picture of the features of FG errors that will be useful in the following sections.

Fig. 3.7 displays the room temperature annealing of FG errors in a NAND memory, which was entirely programmed out of the beam, and then irradiated without bias with $3.6 \cdot 10^6$ Ni ions/cm^2. If we neglect a few readings where bursts of errors were detected

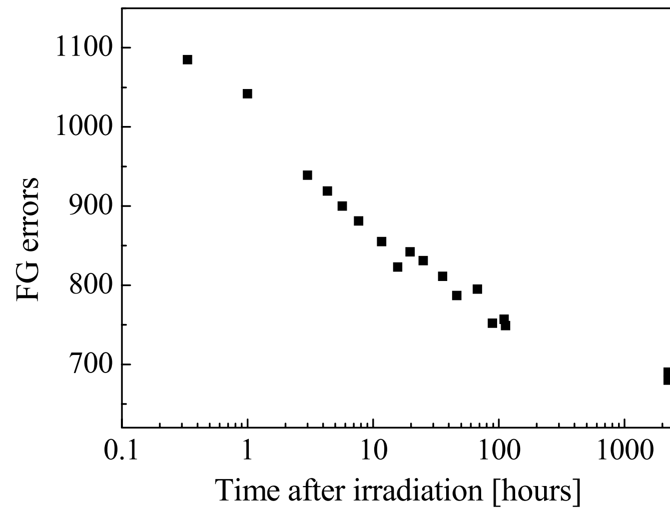


Fig. 3.7. Temporal evolution of FG errors annealing (lin-log scale) at room temperature after irradiation with Nickel with no shields (both the array and the peripheral circuitry are irradiated).

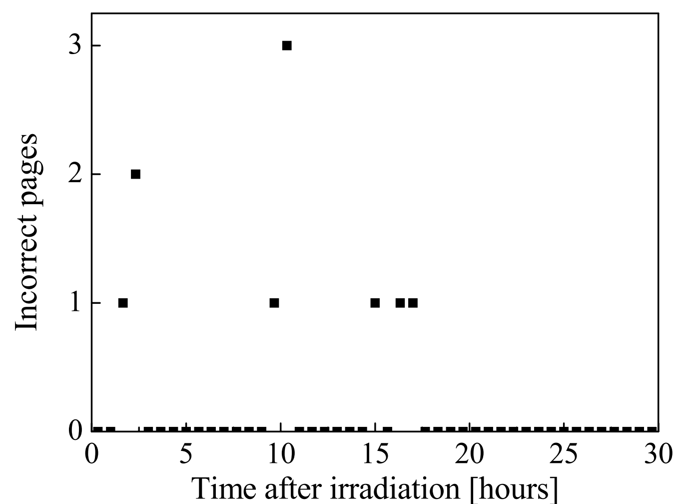


Fig. 3.8. Number of incorrectly read pages in the first hours after irradiation for the same device as Fig. 3.7 irradiated with Nickel.

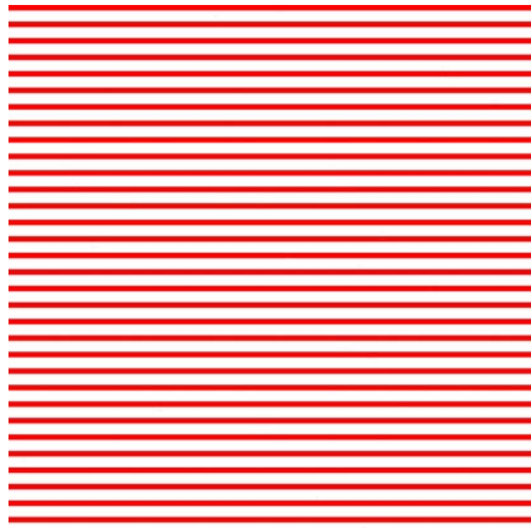
(which are reported in Fig. 3.8), the reduction in the first 100 hours after exposure follows a monotonic decay. In Fig. 3.8, we observe that from the third read operation on, some whole pages (every time a different page) fail in a few reads. In particular, all the 2112 bytes in the pages are read with the same (wrong) value, e.g., ‘04’ instead of ‘00’.

This effect is likely related to radiation damage in the peripheral circuitry, since devices irradiated with shielded peripheral circuitry do not exhibit this behavior, as we shall see in more details in Chapter 4. In this case, the incorrect reading of whole pages probably derives from microdose effects in the PB or address decoder, which, as we mentioned before,

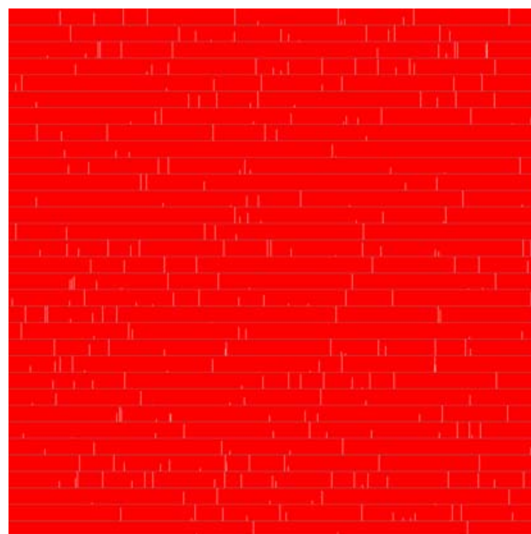
use the relatively thick tunnel oxide as gate dielectric. V_{th} shifts and leakage currents can lead to the wrong read of whole pages.

3.3.4 Single Event Functional Interruptions

In addition to upsets in the PB and FG array, several functional interruptions were detected during both read and Program/Read/Erase/Read cycles under irradiation. Three



(a)



(b)

Fig. 3.9. Physical map of a block after unsuccessful program operations: (a) programming failed on several adjacent word lines (red horizontal lines), (b) only few bit lines were correctly programmed (white vertical lines). In both cases, the status register did not signal any anomaly. The block word lines are split into several parts (separated by grey lines) for ease of visualization.

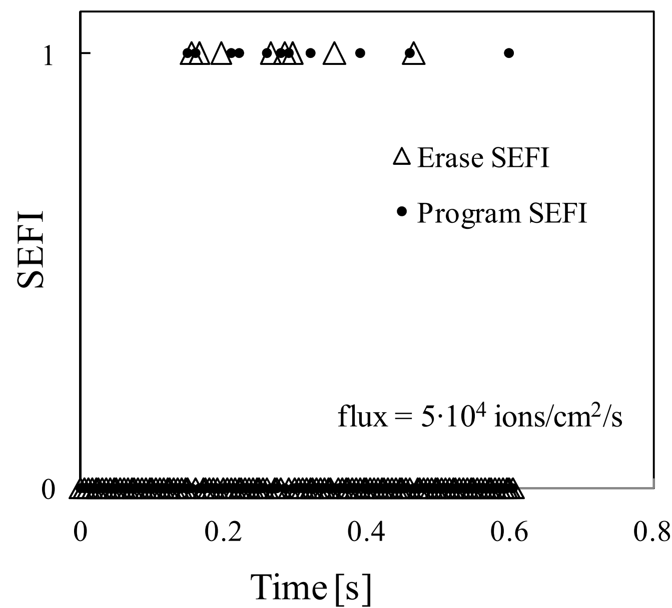


Fig. 3.10. Single Event Functional Interruptions (SEFI = 1) during program and erase operations for a T4 device during irradiation with Br. The device was cycled through a P/R/E/R sequence.

different test sequences were used to investigate the occurrence of functional interruptions:

(i) Continuous cycles of program and erase operations (P/E), monitoring Status Register (SR) and Ready/Busy (R/B) signals: this kind of test allows us to detect possible unsuccessful program and/or erase signaled by the SR and also to monitor the time required to complete a program operation (on the contrary, erase operation has a fixed duration, as explained in more details later on);

(ii) The same cycles as the one described in (i), but with each P/E operation followed by a block read (P/R/E/R): in this way, it is possible to observe the real status or a memory page/block after program and erase operations;

(iii) Finally, simple read cycles on a memory page/block that was previously programmed out of the beam.

In several occasions during test (i), the device SR signaled an anomalous condition and/or an increased program time was detected monitoring the R/B. Programming errors (i.e., errors signaled by the status register after a program operation) were more frequent than erasing ones. This difference may be due to the higher complexity of the program algorithm compared to the erase one. In fact, erasing a block is simply a matter of applying the ‘right’ bias for a fixed amount of time and involves only a limited amount of logic. On the contrary, a more sophisticated algorithm controls program operations. In fact, the correct amount of electrons must be stored in the floating gates so that the programming time (as well as the number of programming pulses) may vary depending on various conditions. After each program operation, the internal microcontroller checks that the programmed cells feature the right threshold voltage. If this is not the case, program is repeated several times until either

SEFIs DURING READ OPERATIONS

	Auto-restored	Reset	Power cycle	Total
Read errors	3	8	5	16
Functional blocks	1	1	3	5

SEFIs DURING P/E OPERATIONS

	Auto-restored	Reset	Power cycle	Total
Read errors	1	3	2	6
Functional blocks	0	0	0	0

Table 3.II. Description of the Single Event Functional Interruptions observed during heavy-ion irradiations.

the bit is correctly set or the maximum number of program operations is reached. In the latter case, the status register signals the presence of an error.

We speculate that when the SEFI is signaled by the SR, the internal microcontroller was unable to program the cells because, for instance, of problems with the charge pumps, which may be unable to provide the correct voltage level under heavy-ion exposure. Charge pumps consist of large capacitors and diodes and are used to internally generate the high voltages needed for program and erase operations (in most modern devices, charge pumps are used during read operations as well). The electron-hole tracks left by heavy ions may temporarily short the electrodes of the capacitors, causing a reduction in the programming voltages. We can rule out any permanent damage to these capacitors (i.e., Single Event Gate Rupture, SEGR), since all the devices worked correctly after irradiation.

The second test we performed (P/R/E/R cycles) showed that program and erase operations can fail on the majority of a block, without the SR signaling any anomaly. In these cases, when the chip is not 'aware' of errors during the program operation, the corruption may have occurred in both the internal registers of page buffer and microcontroller, but also in the SR circuitry. Pointers to locations may fail to be programmed, or flags signaling successful programming may have been altered, giving rise to the error patterns shown in Fig. 3.9. Fig. 3.10 presents an example of the occurrence of functional interruptions (SEFI = 1 in the graph) as a function of time, detected during an irradiation run with Bromine, with the test sequence (ii).

As we saw up to now, with the lighter ions the greatest part of SEFIs occurred during program and erase operations, when the device microcontroller is used more heavily, and the applied voltages are at their maximum. Conversely, with the heavier ions (i.e., Silver and

Bromine), functional interruptions were observed during read operations (iii) as well. In this case, the effect can be attributed to some malfunction in the read pump, which may be temporary unable to provide the correct voltage, or to the microcontroller.

Table 3.II summarizes the features of all the functional interruptions that were observed during heavy-ion exposure. We can distinguish between SEFIs that give rise to read errors only (a whole page or block was read with the wrong value) and SEFIs that slowed down or totally blocked the ability of the device to program and/or to erase. We can also classify SEFIs depending on the way the functionality was restored after the event: in several cases, a power cycle was necessary in order to recover the device from the error condition, in some others a reset command was sufficient, and in others proper functioning was spontaneously restored after a few seconds.

We also often observed a sudden increase in the memory supply current [Irom2007a], which went back to its nominal value after a reset or a power cycle. These current increases may be either due to micro latch-up [Nguyen1999] or to conflicts in the control logic.

3.3.5 Effective Cross Section

Now that we have described and discussed all the features of the errors under heavy-ion irradiation, we may draw some quantitative conclusions on the relative importance of the observed contributions to the overall Single Event Upset cross section. To this end, a full characterization of the FG array and of the PB is presented in Fig. 3.11, where bit cross sections versus LET (no errors were detected with alpha particles) are shown for PB and FG cells (σ_{PB} and σ_{FG}, respectively). These results are in agreement with previous reports, where static cross section per device (corresponding to our $\sigma_{FG,device}$) has been shown to have a larger threshold LET and a smaller saturation value than dynamic cross section (corresponding to our $\sigma_{PB,\ device} + \sigma_{FG,\ device}$) [Oldham2007]. Note that the LET values used in Fig. 3.11 are at the chip surface and have not been adjusted for the energy loss through the overlayers above the transistors, because the LET variation is within 3% and negligible for our purposes.

It is worth to remark that the graph in Fig. 3.11 is expressed in units of cm^{-2} per bit, but in the following we will refer to cross section per device. Based on the previous discussion (setting aside functional interruptions), the highest effective cross section is obtained with a fully programmed memory, which is continuously and entirely accessed performing a read loop. The device cross section (σ_{NAND}) in these conditions is given by the sum of $\sigma_{FG,device}$ plus half of the $\sigma_{PB,0,device}$ (see previous remarks on the impact of read time). Depending on the ion LET, the device cross section, σ_{NAND}, can be dominated by the PB (e.g., with Silicon, $\sigma_{PB,0,device}/2 + \sigma_{FG,device} = 2.1 \cdot 10^{-4} + 1.2 \cdot 10^{-6}\ cm^2$) or by the FG array (e.g., with Silver, $\sigma_{PB,0,device}/2 + \sigma_{FG,device} = 2.4 \cdot 10^{-3} + 5.2 \cdot 10^{-2}\ cm^2$), due to the very different threshold LETs for PB and FG array. On the other hand, let us consider the best case scenario: the memory is fully erased and quickly (and sporadically) read. In this condition, the FG array is not sensitive (being not programmed) and the sensitivity of the PB must be scaled by the read

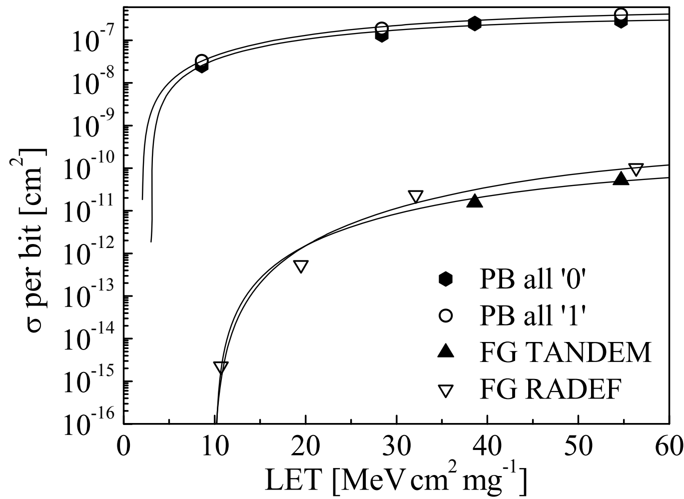


Fig. 3.11. Bit σ_{PB} (TANDEM) and bit σ_{FG} (both TANDEM and RADEF) as a function of the impinging particle LET.

activity ($\sigma_{device} = \sigma_{PB}/2 \cdot t_{read}/t_{irrad}$), where t_{read} is the total time the memory is read while being exposed to heavy ions for a time t_{irrad}.

In more general terms, we can introduce an *effective cross section* ($\sigma_{NAND,eff}$), which takes into account the different contributions and factors we have discussed up to now. We will first define two separate terms, respectively referred to as the PB and FG sensitivity in the following equations:

$$\sigma_{PB} = \left(\sigma_{PB,0} \cdot \frac{N_{FG,0}}{N_{FG}} + \sigma_{PB,1} \cdot \frac{N_{FG,1}}{N_{FG}} \right) \cdot PB_{size} \cdot \frac{t_{read}}{2t_{irrad}} \tag{1}$$

$$\sigma_{FG,SLC} = \sigma_{FG,0} \cdot N_{FG,0} \cdot r_{anneal} \tag{2}$$

where $N_{FG,0}$ and $N_{FG,1}$ are the number of ‘0’ and ‘1’ stored in the FG array, r_{anneal} is the ‘annealing’ coefficient, which is the average reduction in FG errors due to charge neutralization, PB_{size} is the size of the page buffer (the other terms are defined above). A number of simplifying assumptions are made in (1) and (2): FG cells are Single Level Cells (SLC); no multiple bit upsets both for the PB and the FG array [Cellere2007a] and no long-term effects due to Radiation Induced Leakage Current [Cellere2005b] occur. Note that $\sigma_{FG,1}$ does not appear in (2) because its contribution is negligible in comparison to $\sigma_{FG,0}$. In fact, the cell in the neutral state (i.e., with no charge in the FG) is typically read as erased due to its manufacturing parameters (oxide thickness, channel doping, etc.).

In order to determine r_{anneal}, i.e., the percentage of errors which will disappear in actual applications, one needs to know several parameters on the cells threshold voltage and on the shifts induced by heavy ions (both the pre-rad threshold voltage and the amount of

ΔV_{th} are statistical parameters; the second, for instance, depends on the strike location). Since its estimation may prove extremely complex, it is reasonable to assume $r_{anneal} = 1$ to obtain a worst-case estimation of the memory sensitivity.

We can finally obtain the overall device $\sigma_{NAND,eff}$ adding the FG and PB terms, and the SEFI cross section for each operation (read, program, erase) multiplied by the percentage of time in which that operation is performed:

$$\sigma_{NAND,eff} = \sigma_{PB} + \sigma_{FG} + \sum_{OP} \sigma_{SEFI,OP} \cdot \frac{t_{OP}}{t_{irr}} \quad (3)$$

The effective cross section provides a measure of the total sensitive area of the device as a function of the operating conditions, and can be used for estimating the probability of errors, in order to design proper mitigation strategies at the system level.

Technology is going to affect $\sigma_{NAND,eff}$ in a number of different ways. The sensitivity of the FG cells will increase, due to shrinking geometry; as well as the number of FG bits compared to PB bits (unless the memory architecture is modified with larger pages). The SEFI cross section will probably rise, since more advanced memories usually require more complex algorithms to ensure correct operations. Finally, the PB cross section may be only marginally affected by technology scaling, since it relies on the tunnel oxide (which is at its scaling limit) as gate dielectric, at least until high-k dielectrics are introduced.

In the case of Multi-Level Cells (MLC) flash, σ_{PB} remains the same, while (2) must be modified, taking into account the different cross sections for the various program levels (that can be different from one technology to another). In general, for a MLC Flash memory, we can express σ_{FG} as:

$$\sigma_{FG,MLC} = \sum_{state} \sigma_{FG,state} \cdot N_{FG,state} \cdot r_{anneal,state} \quad (4)$$

where $\sigma_{FG,state}$ is the cross section for a FG error in the various program states for a MLC memory, $N_{FG,state}$ is the number of bits programmed with a certain state, and $r_{anneal,state}$ is the annealing coefficient associated with that program state. The most common error is likely given by a cell going from one state to the next one with a lower threshold voltage. Supposing that the program levels are '11', '01', '00', '10', from the lowest to the highest V_{th}., this kind of error involves only one bit and annealing can eliminate it. Yet, a high-LET heavy-ion strike may also cause a shift from the '10' state to the '01' state. In this case two bits are upset, and annealing will probably cure at most only one of them (bringing the cell to the '00' state). In any case, a single coefficient in (4) accounts for the annealing error percentage in our simplified picture.

3.4 Summary

A comprehensive analysis of the different kinds of errors occurring in a NAND Flash memory exposed to heavy ions has been provided. We identified and discussed the features of the errors occurring when the device is operated in different conditions during irradiation. In particular, both the floating gate memory array and the page buffer can contribute to single event upsets. In the latter case, errors can be recovered by simply reading the array once again, while in the former errors cannot be recovered (without reprogramming the cell), if not by using ECC algorithms which are therefore strictly needed to guarantee reliability at system level. Further, SEFIs can happen in the control circuitry leading to the inability to erase or program blocks or pages.

Though SEFIs and control logic errors are still non-negligible, especially with high-LET particles, the most important contribution to the overall heavy-ion sensitivity comes from the floating gate memory array and the page buffer. The importance of the floating gate matrix should not be surprising since the area used by the control circuitry is becoming small as compared to the larger and larger arrays. Our experimental data showed that the FG array has a larger threshold LET and a lower saturation cross section per bit than the page buffer, but, from the practical standpoint, the FG array contains many more bits that the page buffer. Moreover, under certain conditions, errors in FG cells anneal with time, further complicating the issue.

We can conclude that the effective device cross section strongly depends on the operating conditions and on the data pattern. Depending on the ion LET, on the time spent reading the memory, and on the pattern stored in the array, the device sensitivity can be dominated either by the Floating Gate array or by Page Buffer latches. Large variations, up to several orders of magnitudes, can occur as a function of these parameters. Just to give an example, if a memory is kept in standby for the majority of time and read once a year, the reliability of the information stored in the array may be the limiting factor during heavy-ion exposure, whereas the control circuitry, in particular the page buffer, plays a prominent role if the device is read very often.

Chapter 4

Annealing of Floating Gate Errors

When assessing the radiation sensitivity of a complex device such as a Flash memory, an important aspect to take into account is the evolution of the radiation-induced damage as a function of the time elapsed after the exposure. As we will see in this section, Floating Gate errors can decrease after exposure, but, interestingly, under certain conditions they can also increase.

The purpose of this chapter is to analyze how radiation-induced Floating Gate errors can anneal in NAND and NOR Flash memories, after both heavy-ion and total ionizing dose exposure. We will start from the observation of annealing phenomena in the raw bit errors. After that, through Test Mode routines provided by the manufacturer, which allow us to follow the threshold voltage of single floating gate cells, the origin of the effect and the underlying physics will be investigated, also providing some hints on the role of the device operating temperature.

4.1 Annealing after heavy-ion irradiation

In this section, the dependence of the annealing on the impinging particle LET and cell feature size dependence of the evolution of both user mode errors and threshold voltage distributions are studied for the first time.

4.1.1 Devices

For this work we used three kinds of commercial Flash devices, all manufactured by STMicroelectronics/Numonyx:

- 1-Gbit 90-nm Single Level Cell (SLC) NAND (part number NAND01G-B2B)
- 4-Gbit 70-nm Single Level Cell (SLC) NAND (part number NAND04G-B2B)
- 90-nm Multi-Level Cell (MLC), 2-bit-per-cell NOR Flash (part number M58PR256J).

We recall that information is stored in a Floating Gate cell by introducing excess charge in the FG, either electrons or holes, thus changing its V_{th}. FG cells filled with holes are usually referred to as 'erased', while those filled with electrons are referred to as 'programmed'. During the read operation of a FG cell, its V_{th} is compared to a reference voltage (V_{ref}), through a sensing circuit, in order to generate a digital output, which is the only information available in User Mode (UM): based on this comparison, the cell program level is determined. In Single Level Cell devices, each FG transistor stores one bit of information and the sign of the charge stored in the FG is enough to determine the state of the cell; conversely, in 2-bit per cell MLC, every FG can store two bits and, depending on the amount of stored charge, multiple program levels can be chosen.

Figs. 4.1 and 4.2 depict the diagram of the cell V_{th} distributions for the SLC NAND and MLC NOR devices used in this work. Traditionally, the erased level is indicated with '11', while the choice of the codes for the programmed level is arbitrary, keeping into account that close levels differ for only one bit at a time. Neutral cells are those with neither holes nor electrons stored in the FG; in the MLC devices we are considering, the neutral distribution lies between the erased state and the lower V_{TH} program state ('10'). In both figures, the reference voltages dividing the various program states are represented with vertical lines.

4.1.2 Irradiation and experimental

The memories were irradiated at the SIRAD beam line of the TANDEM accelerator at the INFN Laboratori Nazionali di Legnaro (LNL) (Padova, Italy), with ions having different LETs. All the details about the ion species we used are reported in Table 4.I.

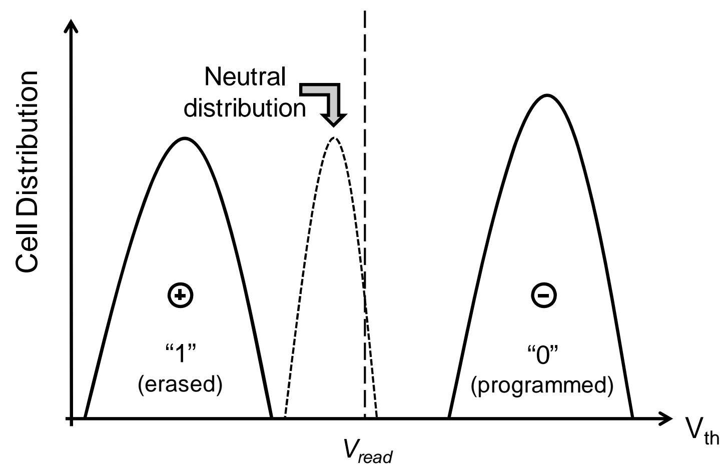


Fig. 4.1. Sketch for the V_{TH} distributions in SLC NAND memories. Erased and programmed levels corresponds to holes and electrons in the FG, respectively, while neutral cells have no charge stored in the FG.

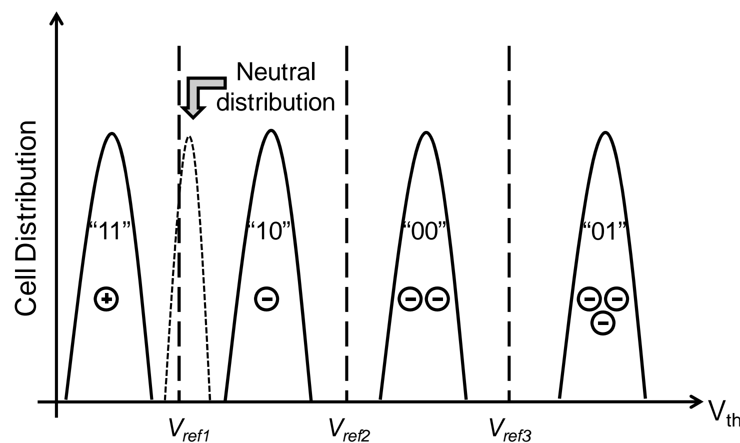


Fig. 4.2. Sketch for the V_{TH} distributions in MLC (2 bits per cell) NOR memories. The erased level stores holes in the FG. For program levels, increasing cell V_{TH} are obtained storing an increasing number of electrons in the FG. Neutral cells have no charge in the FG.

Some NAND blocks and NOR sectors of the devices were programmed prior to irradiation with different patterns (either all zeroes '00' or checkerboard '55', for SLC NAND; all four program levels, for MLC NOR). To exclude the onset of errors other than FG cell errors, we protected the memory peripheral circuitry (charge pumps, row decoder, page buffer, etc.) with 5-mm thick Aluminum shields during heavy-ion exposure.

All irradiations were performed with the device unbiased, at normal incidence, and at room temperature. An ion fluence of approximately 10^5 - 10^6 ions/cm^2 was chosen (and adjusted for every ion depending on its LET) so that a statistically significant number of errors (several hundreds or thousands) could be gathered for each experimental point. Note that all irradiations lasted just few tens of seconds, so, even though it is possible that some

HEAVY-ION SPECIES			
Ion	Energy [MeV]	Surface LET in SiO_2 [$MeVcm^2/mg$]	Range in Si [μm]
Ni	220	27.9	34.8
Br	241	38.1	31.4
Ag	266	53	28.1
I	276	61.8	27.5

Table 4.I. Heavy-ion species used for irradiations (SIRAD facility).

errors annealed during the exposure itself, we will neglect this component in the following analysis.

After irradiation, we kept the devices unbiased at room temperature, and periodically monitored their functionality up to 120 hours after exposure (3000 hours for NOR MLC devices), measuring the number of errors in the irradiated blocks/sectors.

We would like to note that, for both NAND and NOR memories, mandatory Error Correction Codes (ECC) algorithms were disabled during the experiments, allowing us to simplify the analysis and have the maximum visibility on ion-induced errors. It is important to note that ECC is managed in different ways in NAND and NOR devices. In NAND, it is user's responsibility to correctly implement ECC (to this purpose, the manufacturer dedicates some extra bits in every page – the so called 'spare area'). Hence, "ignoring" the ECC simply means not implementing it. Conversely, in NOR devices the reliability of each single bit is guaranteed by the manufacturer by the implementation of error correction inside the device itself. For this reason, a special Test Mode routine in our NOR testing board enables the deactivation of ECC during read operations.

We just briefly mention that, for both NAND and NOR memories, errors must be measured at a constant temperature. In fact, the number of detected errors depends on the device temperature during read operation, as we will discuss in more details in Section 4.2.2.4.

4.1.3 Experimental results and discussion

Immediately after heavy-ion irradiation of SLC NAND blocks and MLC NOR sectors programmed with different patterns (after the *Static Cycles* test described in section 3.2), we detected several single-bit errors on NAND cells programmed at '0' (i.e., with electrons stored in the FG) and on NOR cells programmed at '10', '00', and '01'. On the other hand, no errors were detected in the lowest levels ('1' and '11' for NAND and NOR, respectively, see Figs. 4.1 and 4.2). We remark that error correction, when embedded, was disabled during the experiments.

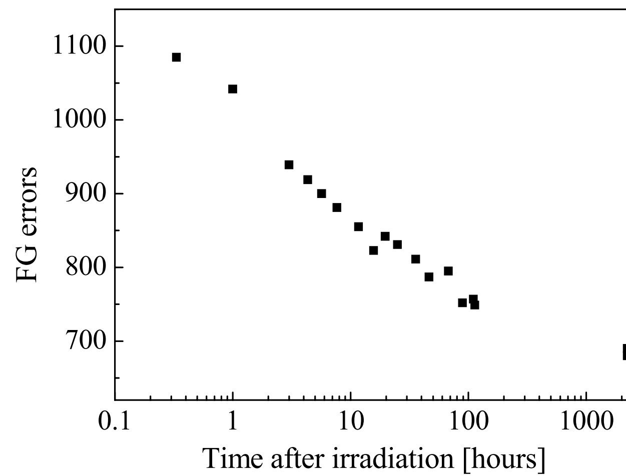


Fig. 4.3. Temporal evolution of FG errors annealing (lin-log scale) at room temperature after irradiation with Nickel for a SLC NAND .

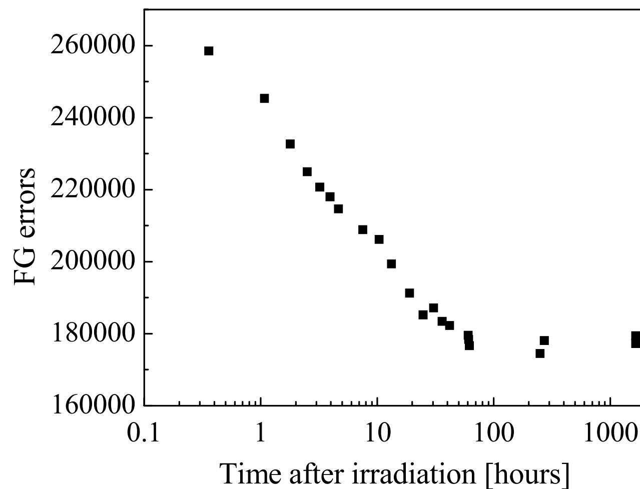


Fig. 4.4. Temporal evolution of FG errors annealing (lin-log scale) at room temperature after irradiation with Silver for a SLC NAND.

As we anticipated in Chapter 3, some of these Floating Gate errors disappear in the hours after heavy-ion exposure. To examine the annealing process in the FG cells while excluding all possible effects in the peripheral circuitry, we performed irradiation with heavy-ion beam, shielding all the control circuitry. In the following, we will discuss the results first on NAND SLC and then on NOR MLC memories.

4.1.3.1 Raw bit error annealing in SLC NAND

Figs. 4.3 and 4.4 show the raw bit error annealing after Nickel and Silver irradiation, respectively, as a function of time after exposure in two 90-nm NAND samples. The monotonic decrease in the number of errors indicates some positive charge detrapping, likely

due to electrons tunneling into the oxide (both from the substrate and the FG) and recombining part of the charge therein trapped. This was previously suggested by Oldham and co-authors in similar devices [Oldham2006].

A detailed analysis of the tunneling process which determines anneling phenomena can be found in [Oldham1986]. Basically, the model assumes that, starting at $t = 10^{-13}$ s, the tunneling front moves into the oxide at 0.2 nm/decade. By "tunneling front", the authors mean that nearly all the holes behind the front are neutralized, and nearly all the holes ahead of the front are not neutralized. The existence of the front is a consequence of the exponential nature of the tunneling probability function. As a consequence, a 2-3-nm oxide (such as the gate oxide of a 90-nm technology) would discharge completely in the order of minutes. On the contrary, for an 8.5-nm oxide, with a front moving in from both interfaces, the fronts would meet in the middle between 10^7 and 10^8 s, which is a few thousand hours. In addition, if the trapped charge distribution was not spatially uniform, but peaked near one of the interfaces, the process would appear to complete sooner, as it will be shown in detail in the next section.

The ONO (Oxide-Nitride-Oxide) dielectric which separates the FG from the CG (Control Gate) is not likely to detrap charge injected therein, as clearly demonstrated by nitride trapping memory technologies. In any case, as nitrogen related centers likely trap both electrons and holes very efficiently, it is possible that the net charge trapping in those layers is relatively small as well. Finally, the lateral isolation (STI) is made of thick oxide, and can trap positive charge as confirmed by total ionizing dose tests [Faccio,Cervelli2005] and also heavy-ion exposure [Gerardin2006].

Anyway, no matter the precise location of the trapped charge, it is difficult to imagine that this alone could generate a user-mode error, without any charge loss from the floating gate. In addition, the fact that not all the FG errors anneal, it is a clear indication that irradiation implies some loss of charge [Cellere2001].

Let us recall that a user mode error in a Flash memory occurs when the threshold voltage of a programmed cell goes below the read voltage (0 V for our SLC devices). It is reasonable to think that part of this shift is given by FG charge loss (in the following we will call this threshold voltage shift $\Delta V_{th,CL}$), and part by charge trapping (referred to as $\Delta V_{th,CT}$). While charge loss leads to a V_{th} shift that is not recoverable, charge trapping causes a recoverable shift, due to charge detrapping and neutralization (causing a shift to the opposite direction, called $\Delta V_{th,CN}$).

As depicted in Fig. 4.5, we can imagine two distinct scenarios, depending on the LET of the impinging ion. In the first case (Fig. 4.5a), let us suppose that $\Delta V_{th,CL}$ alone is large enough to be able to generate a user-mode error: as a result, no anneal of the error will take place, even after charge neutralization. Otherwise, if the contribution of trapped charge is necessary to generate the error (because charge loss alone is not enough to bring the cell V_{th} below the read voltage), as illustrated in Fig. 4.5b, charge neutralization will cause the error to anneal after exposure.

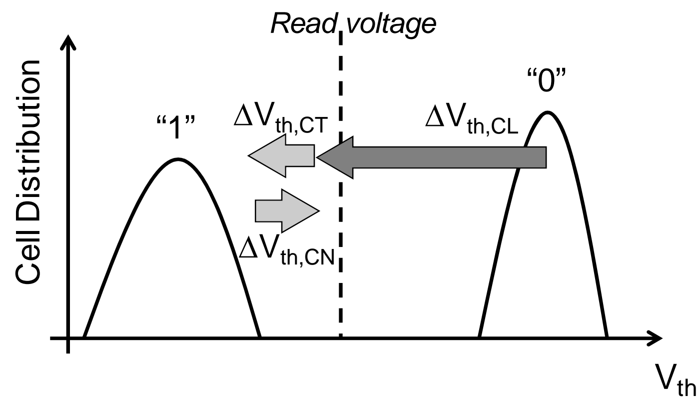


Fig. 4.5 a) Non-annealing user-mode error: if the contribution of charge loss ($\Delta V_{th,CL}$) alone is large enough to cause a user-mode error the error is permanent, regardless of charge neutralization ($\Delta V_{th,CN}$).

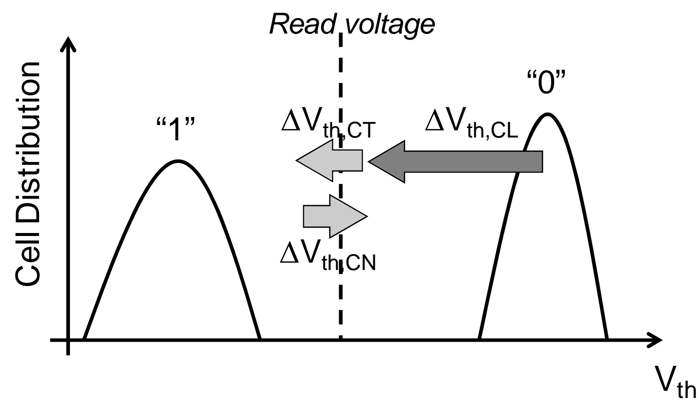


Fig. 4.5b) Annealing user-mode error: if charge loss alone is not enough to generate a user-mode error (but charge loss plus charge trapping, $\Delta V_{th,CT}$, are), charge neutralization causes the error to anneal.

As a consequence, the characteristics of the observed annealing is a function of the LET of the impinging ion, as experimentally confirmed by Figs. 4.3 and 4.4, where particles with different LET values cause different annealing curves. In the following Section, we will deeply analyze this aspect, discussing how, depending on the impinging particle and on the cell feature size, the effect on the evolution of the threshold voltage distributions may be significantly different.

4.1.3.2 Ion LET and cell feature size dependence

Figs. 4.6-4.8 show the post-radiation temporal evolution (in lin-log scale) of floating gate errors in three 70-nm SLC NAND samples irradiated with different ions (Nickel, Bromine, and Iodine). In order to compare the behavior with the three ions, the number of

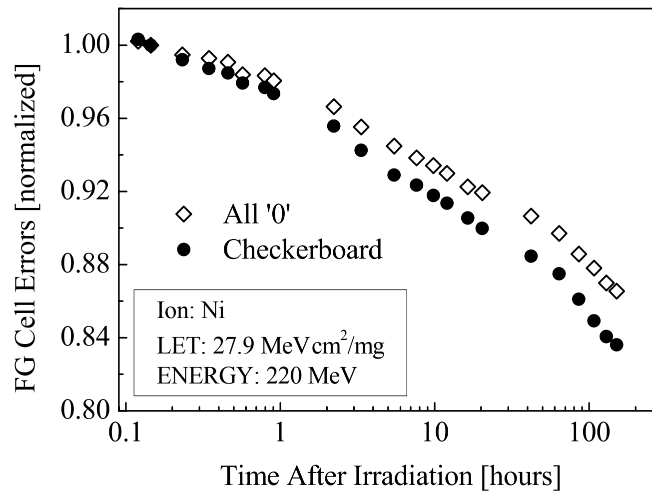


Fig. 4.6. Room temperature annealing (lin-log scale) of FG cell errors in a 70-nm NAND Flash after Nickel irradiation. x axis refers to the time elapsed from the end of the irradiation. In addition, the number of errors has been normalized by its value a few minutes after the exposure.

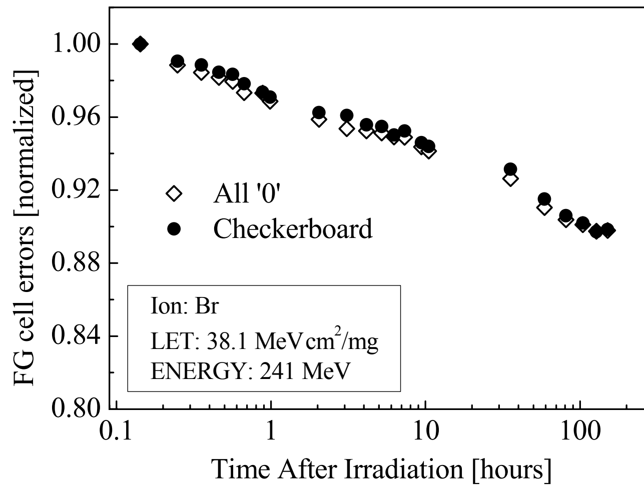


Fig. 4.7. Room temperature annealing (lin-log scale) of FG cell errors in a 70-nm NAND Flash after Bromine irradiation.

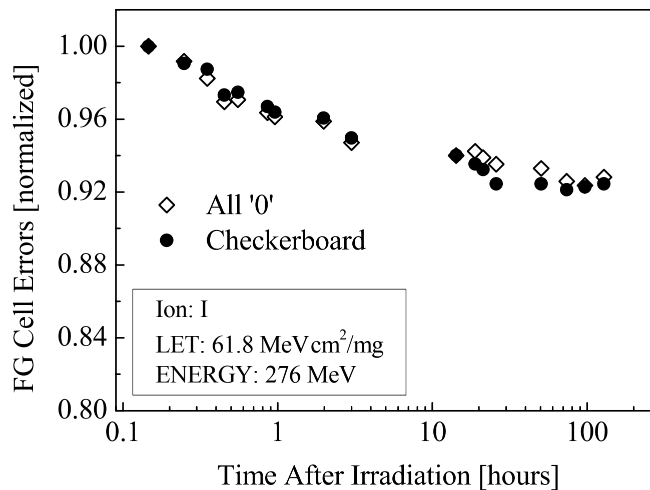


Fig. 4.8. Room temperature annealing (lin-log scale) of FG cell errors in a 70-nm NAND Flash after Iodine irradiation.

FG errors has been normalized at the same time after the exposure (a few minutes after the irradiation).

In all cases, a monotonic decreasing trend is observed, even though different rates of annealing are observed as a function of the ion LET.

In fact, despite the similar qualitative trends, the decrease of the errors in Fig. 4.6 is slower at the beginning than at the end (two slopes are clearly observable in the figure), whereas the opposite occurs in Fig. 4.8, and Fig. 4.7 represents an intermediate case. In other words, the reduction of the errors after higher-LET ion exposure is stronger at short times, and weaker at long times. Irradiations were performed with the NAND blocks programmed with both all zeroes and checkerboard pattern, and very similar results were obtained in the two cases, as seen in Figs. 4.6-4.8, if one considers only the FG programmed to ‘0’ (again, no errors were detected in FGs set to ‘1’). This means that no proximity effects occur (i.e., the error probability in a given cell is not affected by errors in the neighbor cells).

The scatter in the annealing data reported in Figs. 4.6-4.8 is due to intermittent errors. In fact, when the ion-induced V_{th} shift brings the cell V_{th} close to the reference voltage, that bit is sometimes read as 1 or as 0, depending on the noise on the cell and read-out circuits. By the way, this effect is exacerbated in very scaled technologies where the random telegraph noise of the FG cells is more severe. To quantitatively assess these variations (and error bars), the data were processed by removing the main trend (due to the annealing process) and calculating the fluctuations in the number of read errors. Fluctuations are 1% at most in Figs. 4.6-4.8.

An analogous behavior was observed in the 90-nm parts, but with different annealing rates (not shown here). Fig. 4.9 summarizes all the data we gathered on NAND memories. In particular, the graph depicts the percentage of annealed errors 120 hours after the heavy-ion exposure, as a function of the ion LET and technology node, for memories programmed with all zeros pattern before exposure. The percentage of annealed errors is calculated with respect to the errors detected 1 hour after irradiation:

$$Annealed\ Errors\,\% = \frac{Errors@1\,hour - Errors@120\,hours}{Errors@1\,hour} \tag{4.1}$$

In this way, we neglect the initial part of the annealing process, where the fluctuations in the number of errors, may be significant and alter our analysis.

The most striking feature we observe in Fig. 4.9 is the more pronounced annealing for errors in 90-nm devices compared to 70-nm ones. In fact, the annealed error percentage ranges from 4 to 10% in the smaller feature size devices, while for the larger technology node it reaches 34 to 74% in the considered LET range. In addition, as seen in the figure, for both 70-nm and 90-nm parts, the lower the particle LET, the higher the percentage of errors that anneal after 120 hours.

In order to explain this experimental data, we will now make some observations and modeling on the evolution of the threshold voltage distributions after exposure. Fig. 4.10

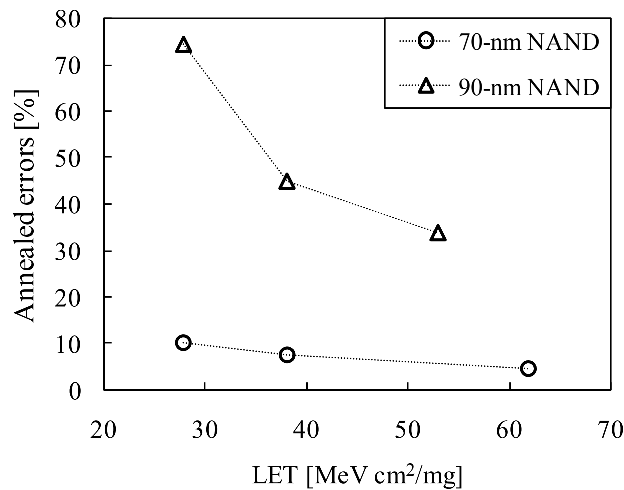


Fig. 4.9. Percentage of annealed errors for 70-nm and 90-nm SLC NAND detected 120 hours after irradiation, with respect to 1 hour after irradiation, as a function of ion LET. The errors refer to blocks programmed with all zeros pattern.

depicts a sketch of the cell distributions for our SLC NAND memories. We remark that in these memories the watershed between programmed ('0') and erased ('1') status is the read voltage (V_{read}). The ion-induced V_{th} shift causes some memory cells to move away from the distribution of the programmed cells, giving rise to a secondary peak, shown with solid line in Fig. 4.10, at an average distance ΔV_{th} (given by $\Delta V_{th,CL} + \Delta V_{th,CT}$) which corresponds to the distance between the peak of the primary and secondary distributions. A bit error occurs if the overall shift $\Delta V_{th,CL} + \Delta V_{th,CT}$ is large enough to bring the cell beyond V_{read}, so that the cell is incorrectly read. Depending on the amount of the two contributions $\Delta V_{th,CL}$ and $\Delta V_{th,CT}$, a given error may anneal or not after exposure, as we discussed in Section 4.4.1 and shown in Fig. 4.5.

All these considerations deal with average values, but to determine the amount of annealed errors and the rate and shape of the annealing curves, statistical distributions of the initial V_{th} and of the shifts induced by heavy ions are of great importance. If all the cell threshold voltages were Dirac delta distributed in the secondary peak, errors would disappear all at once, with a step-like function.

Conversely, different shapes of the secondary distributions lead to different error annealing curves. If we assume that $\Delta V_{th,CT}$ changes at a fixed rate (in a log scale), a wide secondary distribution determines a slower annealing than a narrow one, because in a fixed interval of time during the recovery process, the number of cells crossing V_{read} will be lower compared to a narrow distribution. On the contrary, a narrow distribution will cause a faster reduction in the FG errors, as schematically shown in Fig. 4.10. Wider secondary distributions are expected with smaller floating gate cells, because of the intrinsic higher variability that is associated with smaller feature size. This is certainly a reason for the technological trend observed in Fig. 4.9, where 70-nm memories exhibit a smaller percentage of annealed errors with respect to 90-nm parts (at least up to 120 hours).

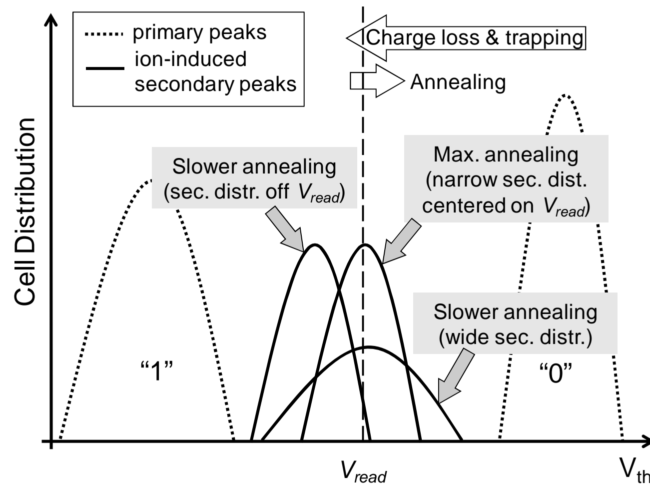


Fig. 4.10. Sketch of V_{th} cell distributions (in log-lin scale) for SLC NAND after irradiation. Secondary peaks induced by heavy ions are shown with straight lines, while primary distributions with dotted lines. Note that 'maximum' and 'slower' refer to the number of the annealed errors (not to the percentage).

An important parameter we should examine when comparing different technologies is the tunnel oxide thickness. In fact, the error recovery process is due to electrons tunneling into the oxide and either recombining with the holes, or forming compensating sites, as described by Lelis *et al.* in [Lelis1988]. It is well known that this tunneling process go faster in thinner oxides. Both the 90-nm and 70-nm samples used in this study have the same tunnel oxide thickness (8.5 nm). As a consequence, this parameter is not considered in the analysis.

Since secondary distributions move over time, because of charge detrapping and neutralization, the annealing rate for a single device may change as time elapses, depending on the point where V_{read} crosses the secondary distribution as a function of time, which is in turn determined by the amount of heavy-ion induced ΔV_{th}. This is in agreement with the experimental observations of Figs. 4.6-4.8, where variable annealing rates are present as a function of time (in the same device).

As depicted in Fig. 4.10, the maximum annealing (in terms of the absolute number of annealed errors) takes place when the secondary distribution is centered on the read voltage. The relative position of the secondary distribution with respect to the read voltage is a function of the ion LET. To a first order approximation, this is determined by the charge loss contribution. In fact, $\Delta V_{th,CL}$ dominates over $\Delta V_{th,CT}$, due to the very small thickness of the oxide layers, which display minimal charge trapping. As reported in previous works by Cellere at al., $\Delta V_{th,CL}$ is a function of the ion LET [Cellere2001]: the higher the LET, the larger the $\Delta V_{th,CL}$ produced by the ion. In particular, Fig. 4.11 shows the measured $\Delta V_{th,CL}$ generated in the NAND FG by the ions we used in this work, for both the 70-nm and 90-nm technology nodes. As seen in the figure, the trend is practically linear and very similar for both technologies, even though the charge loss impact on the V_{th} is higher for the 70-nm

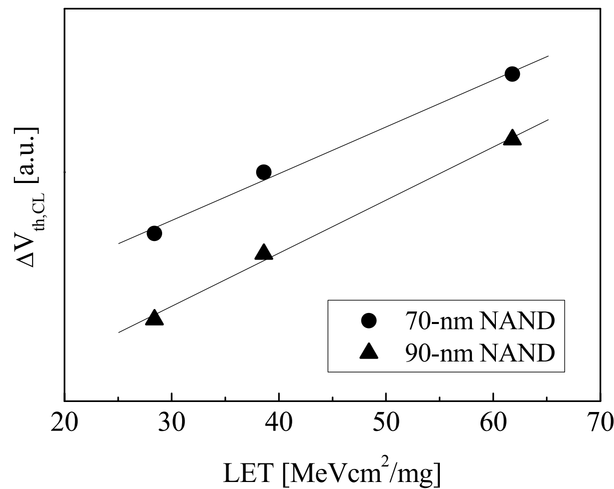


Fig. 4.11. Measured charge loss induced threshold voltage shift ($\Delta V_{th,CL}$) as a function of ion LET for the 70-nm and 90-nm SLC NAND samples used in this work.

parts, as expected, due to the lower number of carriers used to store information in a smaller cell.

Even though there is a simple enough relationship between charge loss and LET, the dependence of the annealing rate on the ion ionizing power is not straightforward at all. In fact, depending on the actual values, the read voltage may intersect the rising or the falling part of the secondary distribution, causing the absolute number of annealed errors to increase or decrease with ion LET. When considering the relative number of annealed errors (as in Figs. 4.6-4.8), one must also consider that the total number of errors (some of which will never anneal because they are too far from V_{read}) observed immediately after irradiation increases with LET for a given ion fluence. This obviously goes in the direction of lowering the percentage of annealed errors for increasing LET.

The dependence of charge trapping [Oldham1993] [Stapor1995] on the particle LET should be taken into account as well, to estimate the number of errors that may potentially anneal after exposure. It is clear that the larger the amount of trapped charge, the larger the amount of FG cell errors that may recover, crossing back V_{read}. The amount of trapped charge is proportional to the charge generated in the oxide by the impinging ion (i.e., the LET), multiplied by the fractional yield, which gives the amount of charge that survives recombination, and by the trapping coefficient of the studied oxide. Charge yield is, in turn, a function of LET. The relationship between fractional yield and LET has been theoretically and experimentally analyzed by Stapor *et al.* [Stapor1995]. Using the data in [Stapor1995], we can calculate the ratio between $\Delta V_{th,CL}$ and $\Delta V_{th,CT}$. It turns out that the ratio is reasonably constant with the LET (less than 10% in the range of interest). As a consequence, we can conclude that $\Delta V_{th,CT}$ goes in the direction of increasing the annealing rate for increasing LET. This term should be accounted for, together with the other factors we have discussed in this section, to determine the annealing behavior of the device.

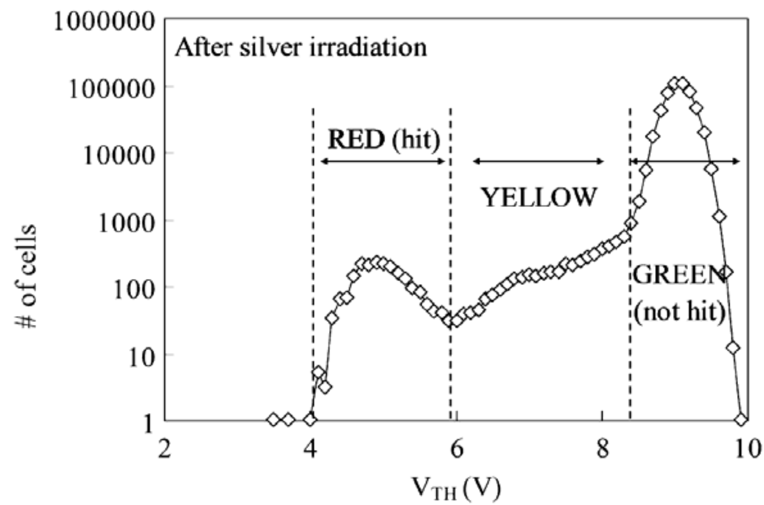


Fig. 4.12. Cell V_{th} distribution for a device irradiated with Silver. 'Yellow' cells, even though have not been hit by the ions, feature a non-negligible threshold voltage shift that cause a tail in the distribution [Cellere2006b].

It is worth to note that the above discussion is valid in the case the read voltage crosses the ion-induced secondary peak. As shown in [Cellere2006b], in addition to the secondary peak, a tail in the V_{th} distributions is created after irradiation, between the primary and the secondary peaks. This tail, as illustrated in Fig. 4.12, includes the cells that experience a non-negligible ΔV_{th}, even though they are not directly hit by the impinging ions. In the case the read voltage intersect the V_{th} distribution exactly in this tail, the analysis we have made up to now should be properly adapted.

4.1.3.3 Modeling of the annealing curves

To further analyze the aspects we have considered in the previous section and schematically summarized in Fig. 4.10, we modeled the error annealing curves, studying the impact of the technology. The main starting hypotheses for the model are:

i. Gaussian distribution for the cell V_{th} before irradiation (see [Cappelletti2000]);
ii. Gaussian distribution for the LET of the incoming ions, which is valid for particles with low energy over mass [Murat2008] (which is the case for the experimental conditions used in this work);
iii. Larger variance (σ) for the post-rad V_{th} distribution in smaller feature size devices (due to the intrinsic higher variability associated to smaller cells);
iv. Larger ΔV_{th} for the more scaled devices [Cellere2008].

Combining i. and ii., it follows that the ion-induced V_{th} secondary distributions can be modeled as a Gaussian function as well. Based on this, we can model the shape of the annealing curve, calculating the number of cells in the secondary distribution that cross the reference voltage due to positive charge detrapping.

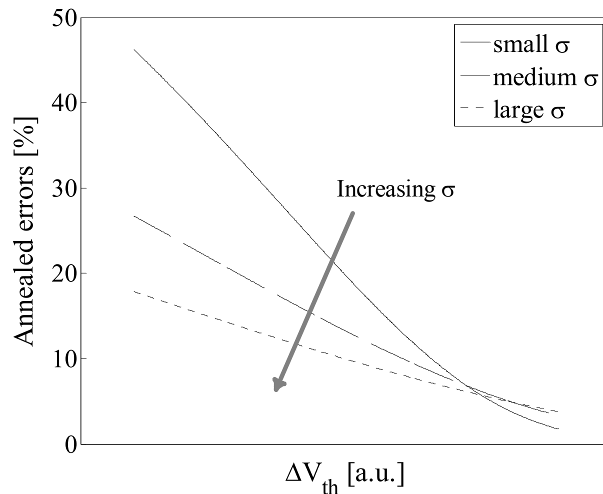


Fig. 4.13. Percentage of annealed errors as a function of ΔV_{th} ($\Delta V_{th,CL}$ + $\Delta V_{th,CT}$), which is directly related to the ion LET, obtained modelling the annealing curves with Gaussian distributions having different variance (σ).

As shown in Fig. 4.13, where realistic values are used for V_{read}, V_{th}, etc., the annealing rate strongly depends on the variance (σ) of the secondary distributions and on the position of the read voltage relative to the secondary peak (i.e., on ΔV_{th}), as qualitatively discussed in the previous section. The x-axis of the figure represents the ion-induced ΔV_{th} ($\Delta V_{th,CL}$ + $\Delta V_{th,CT}$) which is directly related to the particle LET. Fig. 4.13 therefore analytically confirms that the higher the LET (larger ΔV_{th}), the faster the annealing process, in agreement with the experimental results shown in Figs. 4.6-4.8. In addition to that, narrow secondary distributions (indicated in Fig. 10 with 'smaller σ') cause a more pronounced percentage of annealed errors than wider distributions ('larger σ'), at least if we consider small enough ΔV_{th} (see Fig. 4.13, for high values of ΔV_{th} the trend is reversed). Again, as mentioned in the previous section, this model only takes account for the case in which the read voltage crosses the V_{th} cell distributions in the heavy-ion induced secondary peak. We also find qualitative agreement between Fig. 4.13 and the experimental data discussed before (see Fig. 4.9), keeping in mind that for smaller feature size cells the ion-induced ΔV_{th} is larger with respect to larger cells.

4.1.3.4 Annealing in MLC NOR memories

Flash memories with Multi-Level Cell NOR architecture also exhibit an annealing of the observed FG errors. Fig. 4.14 illustrates the post-radiation error evolution for a 90-nm MLC NOR memory irradiated with Nickel. Again, the number of raw bit errors (i.e., measured without ECC) is maximum immediately after the exposure and then monotonically decreases as time goes by. As the experimental data are quite scattered (due to intermittent errors, as explained in Section 4.1.3.2), Fig. 4.14 also provides logarithmic fits of the number of FG errors that are useful as a guide to the eye.

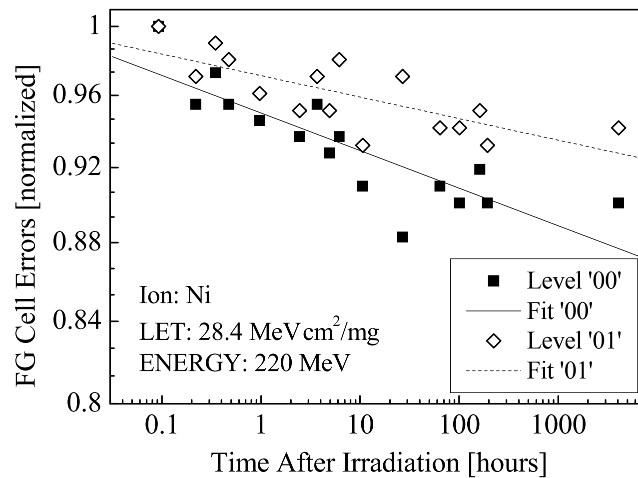


Fig. 4.14. Room temperature annealing of User Mode errors (no ECC) in a 90-nm NOR MLC Flash after Nickel irradiation. The errors are monitored in sectors programmed with the two highest V_{th} program levels ('00' and '01').

Interestingly enough, the evolution of the errors in the cells programmed with '01' (corresponding to the distribution at higher V_{th}) features a different behavior compared to the cells with pattern '00'. In fact, both the annealing speed and the number of annealed errors for cells programmed in the '01' state are lower with respect to the '00' state. In other words, the higher the V_{th} of the FG cell, the smaller the percentage of annealed errors for that program level. Something similar will be observed also after TID irradiation, as we will see in Section 4.2. Concerning the other two patterns, it is worth to remark that no errors were observed in the erased cells ('11') and in the cells programmed with the lower V_{th} level ('10'), due to the lower electric field.

Interestingly enough, the evolution in the number of errors in the cells programmed with pattern '01' (corresponding to the distribution at higher V_{th}) features a different behavior from the ones with pattern '00'. In fact, the annealing speed for the decrease of '01' errors are lower than that of '00' errors. In other words, the higher the V_{th} of the FG cell, the smaller the percentage of annealed errors for that program level.

If we analyze the behavior of V_{th} distributions, for MLC memories the situation is more complex than for SLC memories, as four primary distributions are present. Fig. 4.14 schematically depicts the cell V_{th} distributions for our MLC NOR devices after heavy-ion irradiation. As charge loss and charge trapping take place, the hit cells shift towards the neutral distribution that, for these samples, lies between the '11' and '10' peaks. Due to the different values of the electric field in the various program levels, the larger the distance from the neutral distribution, the larger the $\Delta V_{th,CL}$ of the hit cell. As mentioned before, $\Delta V_{th,CL}$ contribution largely dominates over $\Delta V_{th,CT}$. That is why ΔV_{th} increases for increasing cell V_{th}.

What is left to clarify is the different annealing rate and percentage of annealed errors observed in Fig. 4.14 for the two program patterns. One possibility is to assume that the '01'

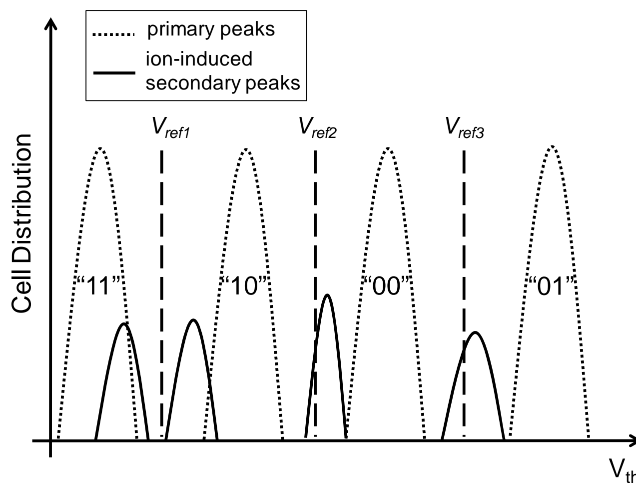


Fig. 4.15. Sketch of V_{th} cell distributions (in log-lin scale) for Multi-Level Cell NOR memories after heavy-ion irradiation. Secondary peaks induced by heavy ions are shown with straight lines, while primary distributions with dotted lines. Reference voltages are represented with vertical dashed lines.

secondary peak is more spread than '00' one (as depicted in Fig. 4.15), because of the shape of the primary distributions those cells come from (the '01' distribution is usually more spread than the '00' one in MLC devices). A narrow distribution, as reported in the previous Sections, means a slower annealing of the raw bit errors, thus explaining the behavior observed in Fig. 4.14.

4.1.4 Summary

We have shown that heavy-ion induced Floating Gate errors anneal at room temperature after irradiation. This phenomenon occurs in both NAND and NOR architectures, with different rates depending on the memory cell size and the impinging ion LET. Several factors can influence the annealing dynamics. The shape and position of the secondary distribution (which contains the cells hit by the ions), relative to the read voltage are the most important ones. These two factors are mainly determined by the ion LET, cell parameters, and their statistical variations. Concerning the shape of the secondary peak, the more spread the secondary distribution, the slower the annealing. As for the position of the peak with respect of the read voltage, the number of errors that anneal is maximum when the secondary distribution is centered on the read voltage. These findings are supported by an analytical model through which we modeled the annealing curves assuming Gaussian distributions for the secondary peaks.

For Multi-Level Cell memories, things can be even more complex. In fact, depending on the amount of the threshold voltage shift and on the shape of the pre-irradiation distribution (which obviously affects the shape of the secondary distribution), errors in cells

programmed with different patterns anneal with different rates. Accurate modeling and prediction can be made only through proper statistical distributions of the V_{th}, available only to the manufacturer.

4.2 Annealing after TID exposure

In this section, the features of post-radiation annealing after TID will be described. Interestingly enough, it will shown that not always does the annealing go in the direction of reducing the number of FG errors, depending on the cell program level.

4.2.1 Device, irradiation, and experimental

For this work, we studied 90-nm NOR (M58PR256J) Multi-Level Cell (MLC), 2-bit-per-cell Flash memories and 4-Gbit 70-nm Single Level Cell (SLC) NAND Flash (NAND04G-B2B), all manufactured by Numonyx.

Irradiations were performed at the Laboratori Nazionali di Legnaro (LNL), INFN (Italy). We irradiated the devices with both 10-keV X-ray (dose rate 500 rad(Si)/s) and 4.2-MeV protons delivered by the CN Van Der Graaff accelerator (dose rate 2.4 krad(Si)/s). The memory peripheral circuitry (charge pumps, row decoder, etc.) was protected during all irradiations with 5-mm thick Aluminum shields in order to prevent the onset of errors other than FG cell errors and damage to the peripheral circuitry.

All the experiments were performed with the following procedure:

i. We programmed the memory, typically one block/sector or a part of it, with different patterns (either all zeroes ‘00’ or checkerboard ‘55’, for SLC devices; all the four program levels for MLC devices);
ii. We irradiated the part unbiased, shielding all the control circuitry;
iii. We repeatedly read the device after exposure up to 5000 hours. SLC NAND memories were only read with UM routines (i.e., detecting rough bit errors); on the other hand, for MLC NOR devices we used a testing board that was developed in conjunction with Numonyx: this board allowed us to use ad-hoc Test Mode routines to measure the threshold voltage of each floating gate cell, and enable/disable error correction code during read operation.

Irradiated samples were kept at room temperature during irradiation and the subsequent post-radiation monitoring. In some of the irradiated samples and in some unirradiated ones as well, we also performed some read cycles at different temperatures (from 5°C to 60°C), to analyze how the number of UM errors and the V_{th} distributions are affected by changes in the operating temperature. The maximum storage temperature specified in the datasheet is 85°C. Note that exposing the device to higher temperatures may cause the programmed cells to be emptied of the charge stored in the FG.

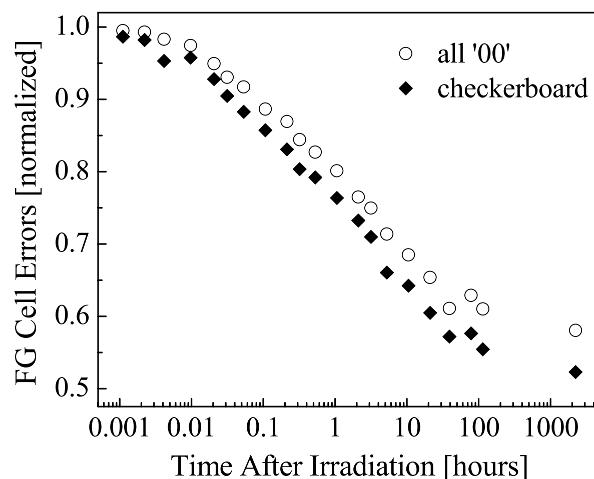


Fig. 4.16 Room–temperature annealing of FG cell errors in 70-nm NAND Flash memory after X-ray irradiation (85krad(Si)).

It is worth to underline that in this work, for both NAND and NOR memories, mandatory Error Correction Codes (ECC) algorithms were not implemented/enabled, to have the maximum visibility on radiation-induced errors. As described in Section 4.2.2, a special Test Mode in our NOR setup enables the deactivation of ECC during read operations.

4.2.2 Experimental results and discussion

In this section, we will first discuss the results obtained through UM routines (analyzing raw bit errors after exposure). Then we will analyze the post-radiation evolution of the threshold voltage shifts with Test Mode routines and after that we will compare User Mode with Test Mode results. Finally, we will present the impact of temperature and we discuss the effects of the program pattern on the annealing process.

4.2.2.1 Evolution of raw bit errors

After TID exposure, several read errors were found both in NAND blocks and in NOR sectors (Figs. 4.16-4.18). Errors are randomly distributed across the tested part of the array, as determined based on scrambling information on the physical bit mapping. These errors are related to a V_{th} shift in the FG (peripheral circuitry was shielded), which has been attributed to the discharge of the FG as illustrated in Chapter 2 [Cellere2004a] [Oldham2006]. Several mechanisms contribute to the shift of the FG V_{th}, including charge generation/recombination/drift, charge trapping, and photoemission.

Concerning SLC NAND memories (Fig. 4.16), we observe a monotonic decrease of the number of errors in all irradiated devices, after both X-ray and proton exposure. Fig. 4.16 shows the decrease of FG cell errors for a 70-nm NAND device irradiated with X-rays (85 krad(Si)).

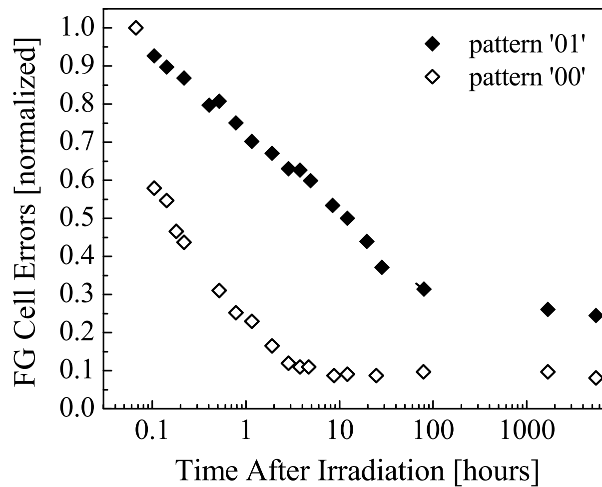


Fig. 4.17. Room–temperature annealing of FG cell errors (patterns '01' and '00') in 90-nm NOR Flash memory after 4.2-MeV proton irradiation (200krad(Si)). The total number of errors for each program pattern is normalized by the number of detected errors for each pattern, immediately after irradiation.

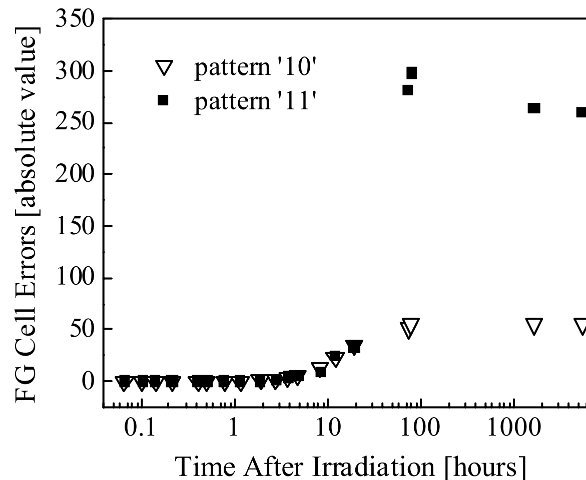


Fig. 4.18. Room-temperature evolution of FG cell errors (patterns '10' and '11') in 90-nm NOR Flash memory after 4.2-MeV proton irradiation (same device part as Fig. 4.17).

The device was programmed with two patterns, all '00' and checkerboard. Errors were observed only in the FGs set to '0', i.e., filled with electrons. As seen in the graph, the errors logarithmically decrease at a constant rate until about 100 hours after the exposure. After that, the decrease still continues, but at a much reduced rate. The two program patterns show a similar percentage of annealed errors, as well as the same decreasing trend as a function of time (the two characteristics have the same slope).

A similar situation occurs in NAND devices irradiated with protons (not shown here).

Figs. 4.17-4.18 show the evolution of FG cell errors in MLC NOR memories after 4.2-MeV proton exposure (200 krad(Si)), highlighting the dependence on the program pattern

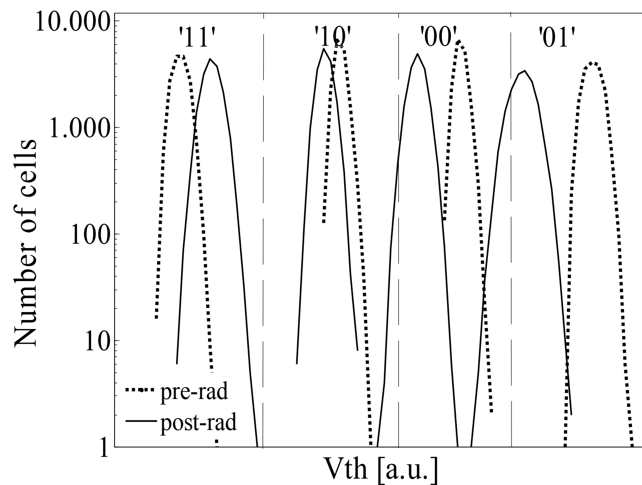


Fig. 4.19. V_{th} distributions for a 90-nm NOR sector before and immediately after exposure to 4.2-MeV protons (same memory as Figs. 4.17-4.18). References voltages are shown with vertical lines.

stored in the cells. Immediately after irradiation, we detected errors only in the cells programmed at the two highest voltage levels (‘00’ and ‘01’), and their number (see Fig. 4.17) shows a decreasing logarithmic trend similar to Fig. 4.16. Once again, for the program pattern corresponding to higher V_{th} (i.e., ‘01’) the error decrease rate slows down between 100 and 1,000 hours after the exposure, likely approaching a saturation. A faster annealing is observed with ‘00’ program level, for which the decrease of errors is faster and moves towards saturation about 10 hours after exposure.

On the other hand, it is interesting to observe that the cells programmed with the lower levels (‘10’ and ‘11’) do not show errors until 2 hours after exposure (Fig. 4.18), when raw bit errors begin to appear and continue to increase until 100 hours and finally begin to saturate around 1000 hours.

4.2.2.2 Evolution of FG cell threshold voltage

Up to now we have presented only results obtainable through User Mode routines, available to the end user. Based on similar data (related to heavy-ion exposure), charge detrapping was supposed to occur in the irradiated FGs in Section 4.1. However, it is not clear how the charge detrapping compares to the discharge mechanisms discussed in [Cellere2004a] [Cellere2005a] [Cellere2007b]. We address this problem thanks to a dedicated setup, which allows us to measure V_{th} as a function of time, and to follow the evolution with time of every single cell after it has been hit by radiation.

As an example, Fig. 4.19 shows the V_{th} distribution of irradiated cells before and immediately after proton irradiation for the same memory as the one considered in Figs. 4.17 and 4.18. Prior to exposure, the memory sector was programmed so that the cells were equally distributed in the four program levels. After irradiation, as seen in Fig. 4.19, the V_{th} distributions shift towards the neutral distribution (located between the ‘11’ and ‘10’ peaks,

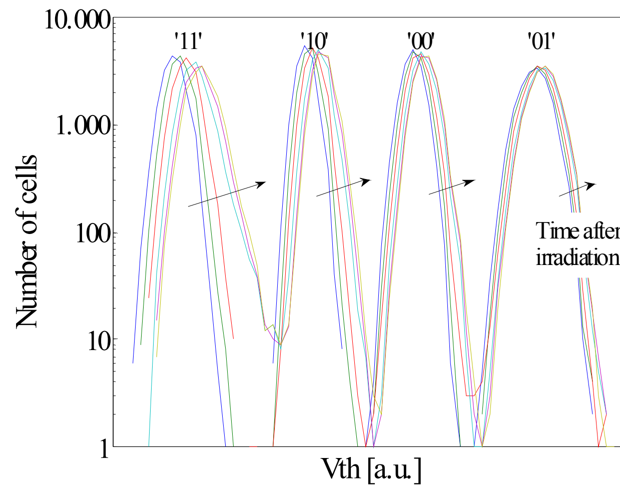


Fig. 4.20. Evolution of the V_{th} distributions for the same NOR memory as Figs.4.17-4.19. The distributions are plotted immediately after irradiation, 1 hour, 10 hours, 80 hours, 1600 hours, and 5500 hours after exposure.

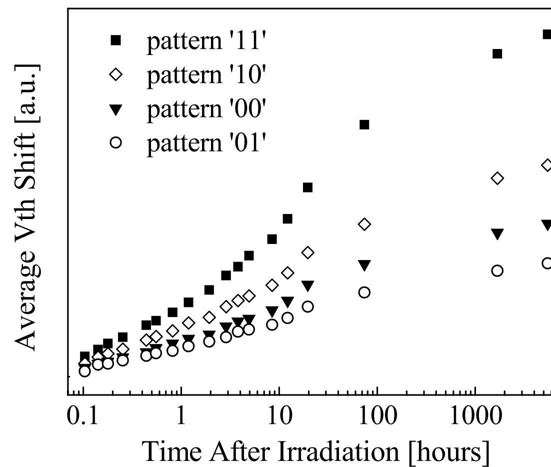


Fig. 4.21. Time evolution of the average threshold voltage shifts for the same NOR memory as Figs. 5.17-4.20. The average ΔV_{th} has been calculated separately for each program pattern.

see Fig. 4.2). This same figure also shows that the larger the distance from the neutral level of the initial distribution, the larger the radiation-induced shift. To distinguish it from the phenomena occurring in the time frame following irradiation, we will call this shift "post-rad shift" ($\Delta V_{th,post\text{-}rad}$).

Note that the high dose rate available at CN accelerator allowed to irradiate devices in very short time (order of seconds), so it is reasonable to neglect those FG errors that anneal during exposure itself.

If we monitor the V_{th} distributions in the hours following the irradiation (Fig.4.20), we observed a second V_{th} shift. In the following, we will refer to this shift as "annealing shift" ($\Delta V_{th,annealing}$). As seen in Fig. 4.20, the V_{th} distributions progressively shift rightwards,

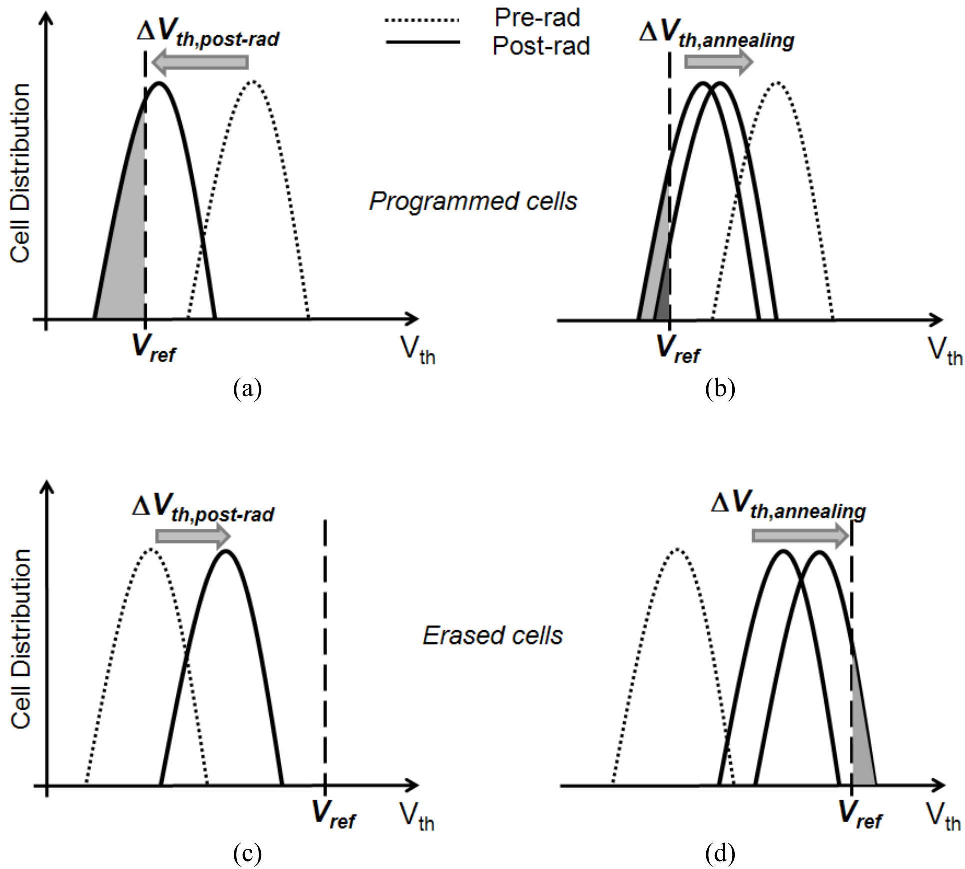


Fig. 4.22. Sketch of V_{th} cells evolution for programmed cells (a), (b) and for erased cells (c), (d), after TID irradiation and during room temperature annealing, respectively. (a) and (c) depict the situation immediately after irradiation where the distribution shifted $\Delta V_{th,\ post\text{-}rad}$ towards the neutral distribution.

towards higher V_{th} values. Besides, the shift is larger for the lowest program level ('11'), and monotonically decreases going from '10' to '01', through '00'.

Fig. 4.21 illustrates the evolution of the average V_{th} shifts for the cells programmed in all the four program levels and gives a straight idea of the magnitude of the shifts as a function of time elapsed after the exposure. As qualitatively observed in Fig. 4.20, Fig. 4.21 confirms that the average V_{th} shift increases with decreasing program level (i.e., for cells with lower V_{th}). It is worthwhile to note that the observed V_{th} shifts are not a measurement artefact. In fact, Figs. 4.19-4.21 refer only to the irradiated cells. Indeed, during irradiation, part of that same sector was covered with shields and the V_{th} of the shielded cells was checked and found unchanged after exposure. Since the reference cells are the same for all the FGs in the sector, we can definitely rule out any damage to the peripheral circuitry, and therefore attribute the V_{th} shift to the irradiated FG cells themselves.

4.2.2.3 User Mode vs Test Mode results

The behavior of the V_{th} shifts in MLC NOR samples we have just described is

perfectly consistent with the evolution of rough bit errors observed in Figs. 4.17-4.18.

Let us first consider the cells belonging to the distribution featuring the highest V_{th}. Immediately after irradiation, part of these cells go below the highest reference voltage due to $\Delta V_{th,post-rad}$, as observed in Fig. 4.19 and this explains the appearance of User Mode errors. The phenomena we are describing are schematically depicted in Fig. 4.22. Fig. 4.22(a) shows a sketch of the programmed cell distribution that experienced a $\Delta V_{th,post-rad}$ shift immediately after exposure. The integral of the curve highlighted in gray gives the cells that are wrongly read, being below V_{ref}. Yet, as time goes by, as illustrated in Fig. 4.22(b), the V_{th} distribution moves towards higher values due to $\Delta V_{th,annealing}$, and some of the cells cross back the reference voltage, causing the corresponding errors to disappear (the gray portion in Fig. 4.22(b) is smaller than in Fig. 4.22(a)). The rate of the post-radiation error reduction depends on the value of the V_{th} distribution, evaluated at the reference voltage: the larger this value, the larger the number of cells for which even a small shift in the V_{th} can cause a large number of errors to disappear after irradiation. In other words, errors anneal because the shift observed as a function of time after irradiation is opposite in sign to the one occurring right after irradiation.

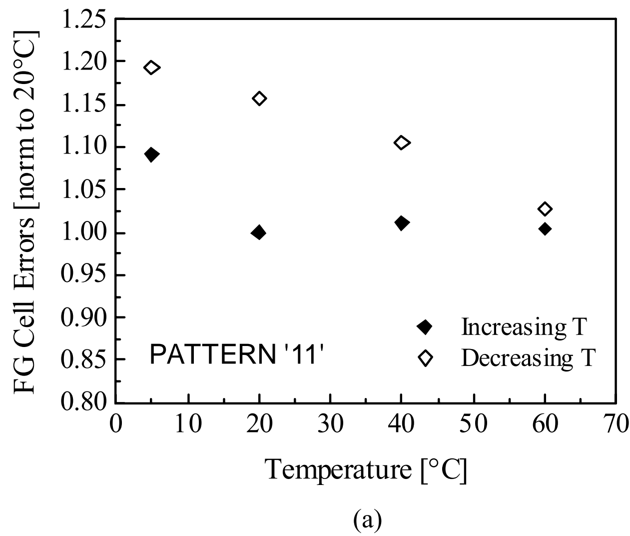
However, this is not true for all the program levels. In fact, for the ‘11’ level (erased cells), both shifts bring the cell V_{th} to the same direction, that is towards higher values. This situation is depicted in Figs. 4.22(c)-(d). As a consequence, even though no raw bit errors are detected immediately after exposure, some errors appear later, when the combined effect of the two shifts, $\Delta V_{th,post-rad}$ and $\Delta V_{th,annealing}$, causes some cells to cross the lowest reference level.

In all cases, the magnitude of both $\Delta V_{th,post-rad}$ and $\Delta V_{th,annealing}$ depends on the received dose, and so does the number of FGs whose V_{th} is above or below the reference level, causing the post-radiation behavior to be a complex function of the pre-rad distributions, of the received dose, and dose rate. Concerning this last point, it is worth remarking that our irradiations have been performed at high dose rates so that annealing during exposure was minimal.

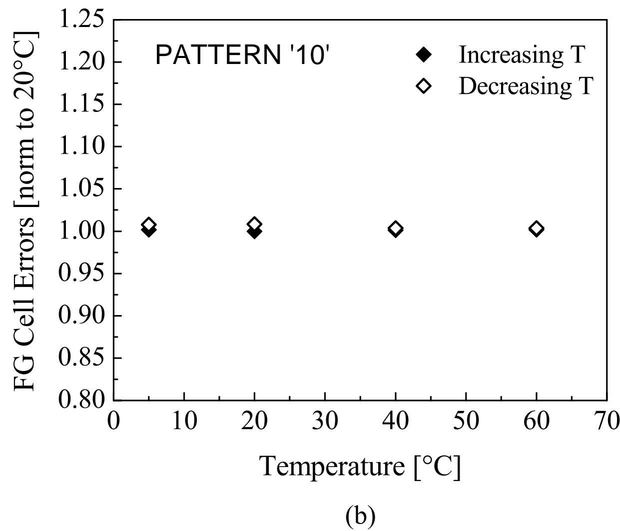
4.2.2.4 Temperature effects

Another important factor we should consider in the analysis is that the device temperature affects the number of observed errors. Figs. 4.23-4.24 show that the number of read errors in an irradiated memory depends on the device temperature, with a behavior that changes with the program patterns. Note that in these experiments, both irradiation and annealing were always done at room temperature, only the error measurement was performed at different temperatures.

As seen in the graphs, for ‘01’ cells (Fig. 4.23(d)), reading the FG array at higher temperature causes more rough bit errors. This is not true neither for ‘10’ cells, for which temperature does not substantially affect the error number (Fig. 4.23(b)), nor for ‘00’ and ‘11’ cells, for which we detect a slight decrease in the rough bit errors at high temperature, as



(a)

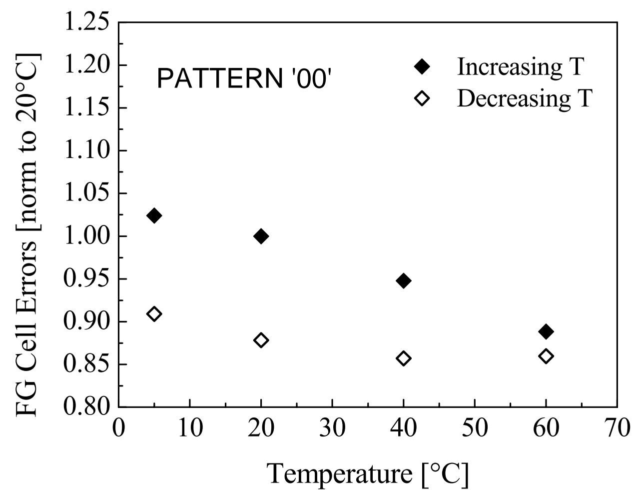


(b)

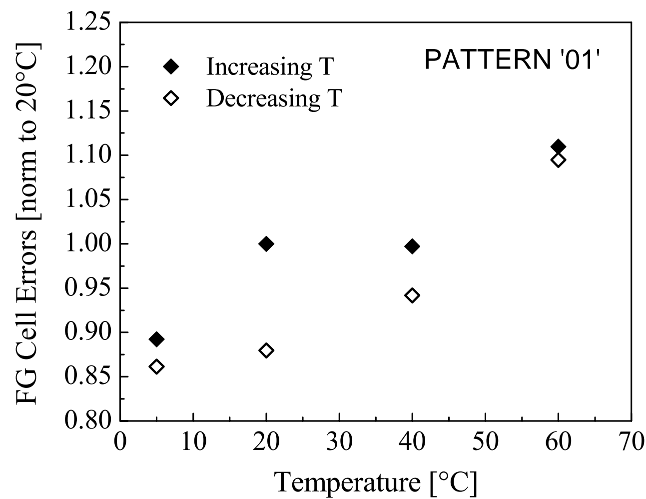
Fig. 4.23. Temperature dependence of rough bit errors, for program, levels '11' and '10', for a 90-nm NOR irradiated with X rays. The evolution is shown for both increasing and decreasing temperature: we started at 5°C and went up to 60°C, after that we went from 60°C down to 5°C. In both cases, the number of errors was normalized to the errors detected at 20°C during the increasing temperature ramp.

illustrated in Figs. 4.23(a)-(c).

All these graphs show experimental data for both increasing and decreasing temperature characterizations. Hysteresis is present due to the acceleration of charge detrapping/neutralization at high temperatures. In fact, for pattern '11' (holes in the FG), after the first characterization at high temperature we observe an increase of the number of FG errors; in this case, detrapping of positive charge brings to an increase in the FG errors. On the contrary, for the other three program levels, all corresponding to excess electrons in the FG (that is, removal of positive charge from the oxide means a reduction in the observed errors), we detect a decrease in the raw bit errors after heating the device.



(c)



(d)

Fig. 4.23. Temperature dependence of rough bit errors, for program, levels '00' and '01', for the same 90-nm NOR sample and same experiment as Fig. 4.23(a)-(b).

To better understand the rough bit error dependence on temperature, we measured the cell V_{th} distribution as a function of temperature. The result is depicted in Fig. 4.24: a shift of all curves towards lower values of V_{th} is detected at high temperatures. However, Fig. 4.24 does not explain the behavior depicted in Figs. 4.23. In fact, both the FG array and the reference cells are affected by changes in the operating temperature in the same manner. As a result, one would expect that if both the V_{th} of a given FG cell and that of the reference cells change to the same extent, the number of raw bit errors remains constant.

Yet, we should also take into account that the number of User Mode errors is influenced by FG cells and peripheral circuitry noise (thermal and RTS - Random Telegraph Signal [Monzio2007]), and this is larger at higher temperatures.

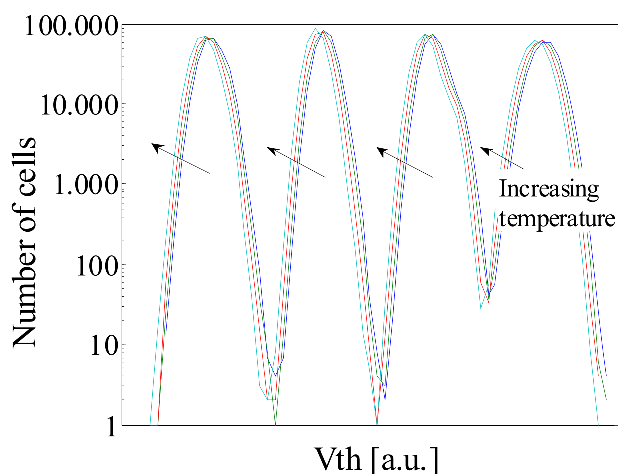


Fig. 4.24. Temperature dependence of V_{th} distributions for the same irradiated 90-nm NOR sample shown in Fig. 4.23. The cell threshold voltages were measured at 5°C, 20°C, 40°C, and 60°C.

The impact of noise on detected FG errors is schematically illustrated in Fig. 4.25. All other things being equal, a larger noise means an increase in the number of cells that can be erroneously read, but at the same time, some cells that are always incorrectly read at lower levels of noise, may be read correctly at a higher levels of noise. It is the balance between these two populations that determines whether the number of raw bit errors increases or decreases with noise (hence with temperature).

Fig. 4.25 depicts a situation of increasing errors with temperature, as is the case for pattern '01' in Fig. 4.23(d). In fact, the number of cells that may be read incorrectly with increasing noise is larger than the number of bits that may be read properly with increasing noise. In simple words, this happens when the V_{th} distribution is higher on the side of V_{ref} where the cells are read correctly (dashed region in Fig. 4.25). If this is not the case (because the reference voltage intersects the distribution on a tail where its shape is quite irregular), as for all the other patterns shown in Figs. 4.23(a)-(c), the errors may stay constant or even decrease with increasing temperature.

4.2.2.5 Mechanism and Program Pattern Effects

After linking the presence of read errors to the V_{th} shifts, we can now discuss the physical origin of $\Delta V_{th,post\text{-}rad}$ and $\Delta V_{th,annealing}$, with a focus on the impact of program pattern on the annealing dynamics. Previous works analyzed the V_{th} shift in irradiated FGs a few days after TID exposure both in NAND and NOR memories [Cellere2004a] [Cellere2005a] [Cellere2007b], i.e., when $\Delta V_{th,annealing}$ was practically stable.

Our data show that the main effect produced by irradiation is charge loss from the FGs, in agreement with previous work (at least, for cells programmed at higher V_{th}). Indeed, following irradiation, the cells tend to move towards the neutral distribution ($\Delta V_{th,post\text{-}rad}$) and

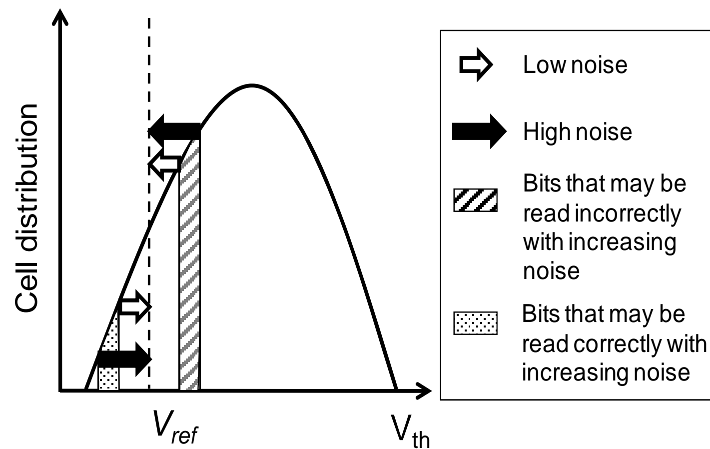


Fig. 4.25. Sketch of the effect of the temperature-induced noise on V_{th} distributions. In this scenario more cells are erroneously read at high temperature rather than at low temperature (cf. Fig. 4.23(d)).

the shift is larger for the cells that are programmed at higher level (thus featuring higher electric fields) [Cellere2007b]. Yet, in addition to charge loss, charge trapping (and interface traps generation) can also occur in the oxide surrounding the FG, in particular in the tunnel oxide, which is ~10nm thick in our NOR devices. In this case, neutralization of the positive charge may induce a shift $\Delta V_{th,annealing}$ (towards higher V_{th}). This shift, if large enough, may cause the error either to disappear (for levels '01' and '00'), similarly to what we observed after heavy-ion exposure and extensively analyzed in Section 4.1, or to appear (levels '11' and '10') as explained before.

The dependence of the annealing rate on the cell program level is not straightforward (Figs. 4.20-4.21). First of all, even though there is no conclusive evidence, given the time scale (tens of thousands of hours) which would be needed to properly examine saturation, we can reasonably assume that errors in the different patterns saturate at different values (see rough bit errors in Fig. 4.18, but also average V_{th} shifts in Fig. 4.21). This means that:

i) either different amounts of charge are trapped in FG cells programmed at different levels
ii) or the same amount of charge is distributed along the oxide thickness in different ways (charge that is closer to the Si/SiO_2 interface has a greater effect on the V_{th}).

It is well known that the oxide trap capture cross section is a function of the oxide electric field, with a peak at intermediate fields [Shaneyfelt1990] [Haran2008]. As a result, the oxide layers of a FG cell experience an amount of trapped charge that depends on the program level. If we assume a maximum of the trap capture cross section at less than 1 MV/cm [Haran2008], we can conclude that the amount of charge trapping is minimum at the highest program level ('01'), in good agreement with our experimental observations. In fact, less trapped charge means slower annealing and the errors in '01' level anneal slower than all the other ones. On the other side, the error in the cells programmed at level '11' (i.e., with

holes in the FG) are the fastest to anneal, because plenty of electrons close to the Si/SiO_2 interface are available to tunnel into the oxide and recombine the charge trapped therein (where it is most effective on the V_{th}).

In addition, also the spatial distribution of trapped charge can significantly vary as a function of the cell program level. In fact, for the erased cells ('11'), charge stored in the FG is positive: this means that the electrons generated by radiation will be pulled to the FG, and holes will be pushed to the Si interface. For the other levels, the FG is increasingly negative for increasing V_{th}, which means that holes will be pulled toward the FG, more strongly for the higher program levels. Therefore, the spatial distribution of trapped holes is different for each level. As a consequence, the farther the holes are from the interface, the longer it will take the tunneling front to reach them. This explains the experimental data discussed before (see Fig. 4.21) very nicely.

4.2.3 Summary

In this section, we have shown that after significant total ionizing dose exposure, the threshold voltage of Floating Gate cells shifts due to a combination of charge loss and positive charge trapping in the oxides surrounding the FG. Charge loss induces a permanent V_{th} shift, whereas charge trapping brings to a reversible alteration of the threshold voltage that can be recovered due to charge detrapping and neutralization. As a result, in the time following exposure, the number of FG cell errors can either increase or decrease, depending on the initial program level. Due to the peculiar read out paradigm of Flash memories, even a small V_{th} shift during the annealing may result in a large change in the number of errors, depending on the value of the V_{th} distribution, evaluated at the reference voltage. Operating temperature can modify the number of read errors as well, because it may introduce an alteration in the V_{th} distributions due to an increase of the FG cell and peripheral circuitry noise (thermal and random telegraph).

These findings show that accelerated tests may significantly overestimate (or sometimes underestimate, if proper care is not taken) the error rate in real operating conditions. In particular, it is worth to highlight that tests at high dose rate usually overestimate the number of FG errors: the larger the dose rate, the lower the percentage of errors that may anneal during irradiation. Conversely, in typical applications, for instance during a space mission, the dose rate is much lower than in accelerated tests. As a result, in such a scenario we can imagine that, for the same total received dose, the number of Floating Gate cell errors is lower (or higher for low-field cells) due to annealing process.

Chapter 5

Neutron Induced Soft Errors

Atmospheric neutrons are a known source of soft errors in a number of electronic devices. Most of the data in literature refer to static and dynamic CMOS memories.

No report exists describing neutron effects in Flash memories, even though, based on heavy-ion data presented over the last decade, these devices are expected to show sensitivity to neutrons as well.

In this chapter, it is shown for the first time that atmospheric neutrons are able to induce soft errors in Flash memories. Detailed experimental results provide an explanation linking the Floating Gate cell soft error rate to the physics of the neutron-matter interaction. User mode results are combined with test mode routines to study the values of the threshold voltage of the irradiated memory cells. As we will see in the following sections, the neutron sensitivity is expected to increase with the number of bits per cell and the reduction of the feature size, but the issue is within the limit of current Error Correction Code schemes capabilities and will likely remain so in the foreseeable future.

5.1 Devices, experimental, and irradiation

In this work we studied different kinds of devices which main features are summarized in Tables 5.I and 5.II. In particular, Table 5.I shows the devices manufactured by STMicroelectronix/Numonyx, where reserved test modes were available to measure and map the threshold voltage (V_{th}) of all FG MOSFETs. On the other hand, Table 5.II illustrates the commercial devices we could only address through user mode routines. Overall, the used samples are representative of all the major vendors and NAND technologies that are currently on the market, including FG, nitride trapping, Single Level (SLC), and Multi-Level Cell (MLC) devices.

With regards to the experimental procedure, the devices were programmed with all the program levels (in the following numbered from the lowest to the higher V_{th} as L0, L1, L2, and L3) and they were measured out of the beam: in the devices that could only be addressed in User Mode the number of raw bit errors (i.e., without ECC) was detected in

Architecture	Feature size [nm]
FG NAND	90
FG NAND	70
FG NOR MLC	90
FG NOR MLC	65

Table 5. I. Main characteristics of the devices studied with test mode routines (i.e., in terms of V_{th} distributions).

Vendor	Architecture	Feature size [nm]	Capacity
A	FG NAND MLC	65	8 Gbit
A	FG NAND MLC	50	32 Gbit
B	FG NAND MLC	90	8 Gbit
B	FG NAND MLC	65	4 Gbit
B	FG NAND SLC	65	4 Gbit
B	FG NAND MLC	51	32 Gbit
C	FG NAND MLC	70	8 Gbit
C	FG NAND MLC	60	8 Gbit
C	FG NAND MLC	48	32 Gbit
D	Nitride trapping NAND	90	512 Mbit

Table 5.II. Main characteristics of the devices studied with user mode routines (i.e., in terms of raw bit errors).

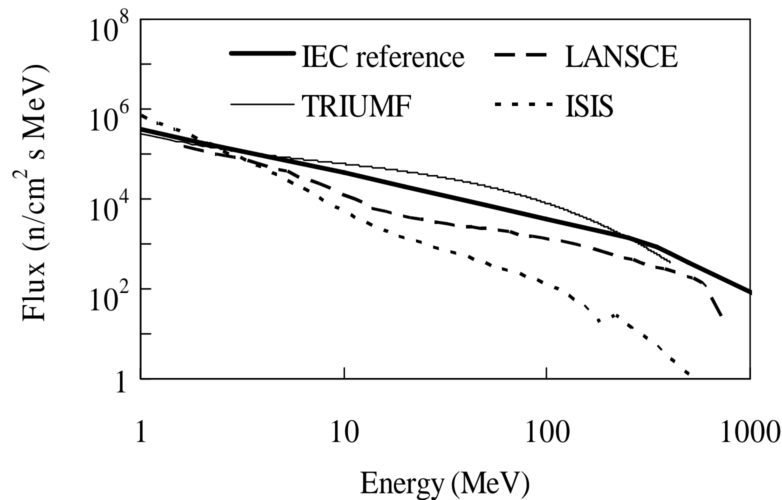


Fig.5.1. Differential flux as a function of energy for the neutron sources used in this work, compared with the IEC standard (terrestrial neutron flux accelerated by a factor of 10^8) and with Los Alamos facility (LANCSE).

all memory blocks, while in Numonyx samples the V_{th} of some memory blocks were measured.

After this pre-radiation characterization, the devices were irradiated at different facilities. All irradiations were made on unbiased devices, at room temperature and normal incidence. For each exposure run, thousands of errors were gathered, assuring the statistical significance of the results.

The samples were finally measured again after irradiation. Measurements were carried out with some delay - weeks/months - due to sample activation induced by neutron irradiation, so the annealing phenomena described in Chapter 4 are practically over in this section. Non-irradiated reference devices were also kept alongside the irradiated ones and measured at the same time.

The devices were irradiated at two different wide-energy neutron sources:

– TRIUMF (Vancouver, Canada)
– ISIS (Rutherford Appleton Laboratories, Didcot, UK).

At both TRIUMF and ISIS, the neutron beam mimics the atmospheric neutron field, accelerated by several orders of magnitude, as depicted in Fig. 5.1, where the neutron differential flux is plotted as a function of energy. It is interesting to examine the LANSCE-equivalent neutron fluence on the samples, that is a measure of the effectiveness of the beam at ISIS compared to LANSCE [Platt2008]). According to [Platt2008], this value is $1.68 \cdot 10^{10}$ n/cm^2, corresponding to about 148000 years at New York City.

As we will see in the following sections, this approach allows us to estimate the real soft error rate of actual devices in the terrestrial environment. In addition to this, the study of the actual threshold voltage shifts of the hit FG cells enables a comparison with the V_{th} shifts induced by heavy ions, hence a detailed study of the neutron reaction byproducts.

Manufacturer	Array size	Technology	# of tested devices	Logic level	cross section (cm^2)	cell FIT per Gbit (without ECC)
A	8Gbit	FG NAND, MLC 65nm	14	00	8.53×10^{-19}	11.9
				01	2.31×10^{-18}	32.3
				10	9.61×10^{-19}	13.5
				11	4.14×10^{-21}	0.1
B	8Gbit	FG NAND, MLC 90nm	13	00	3.53×10^{-18}	50.2
				01	3.33×10^{-18}	46.6
				10	3.82×10^{-20}	0.5
				11	4.14×10^{-21}	0.1
B	4Gbit	FG NAND, MLC 65nm	18	00	4.30×10^{-18}	60.2
				01	4.45×10^{-18}	62.2
				10	3.55×10^{-20}	0.5
				11	0	0.0
B	4Gbit	FG NAND, SLC 65nm	13	00	1.91×10^{-21}	0.0
C	8Gbit	FG NAND, MLC 70nm	4	00	1.12×10^{-17}	157.5
				01	7.94×10^{-18}	111.2
				10	9.94×10^{-20}	1.4
				11	0	0.0
D	512Mbit	Nitride trapping NAND 90nm	8	0	7.21×10^{-19}	10.1

Table 5.III. Neutron-induced raw bit errors (without ECC and excluding the intrinsic errors) detected in commercial Flash irradiated at ISIS. The total fluence was 1.1×10^{10} n/cm^2, corresponding to ~82,000 years at ground level and to ~27 years at airliners cruise altitude.

5.2 Raw bit errors

The first experimental results shown in this section are the numbers of raw bit errors after neutron irradiation at the ISIS facility. In other words, we will examine the output logic data that are available to the final user of the device. The results refer to two different irradiation campaigns, both at the ISIS facility.

The first campaign was performed in May 2008 and the results are summarized in Table 5.III. As we can see, all the tested devices, regardless of vendor and technology, exhibit neutron-induced errors (intrinsic errors that were present also in the non-irradiated memories have been removed) after an exposure equivalent to ~ 82,000 years at ground level (~ 270 years at avionic altitudes [Goldhagen2002]). In Table 5.III, two significant parameters have been calculated:

- the error cross section (σ) expressed in cm^2, i.e., the number of bit errors divided by the total received neutron fluence;
- the failure rate expressed in cell FIT per Gbit (Failure In Time, i.e., the number of errors in 10^9 years of operation), as computed before the application of ECC algorithms required in NAND Flash.

Two are the striking features about these values. First, the bit cross section strongly depends on the cell program pattern and, second, it is larger in MLC implementations with respect to SLC ones (for the samples of vendor B). It is worth to note that the number of

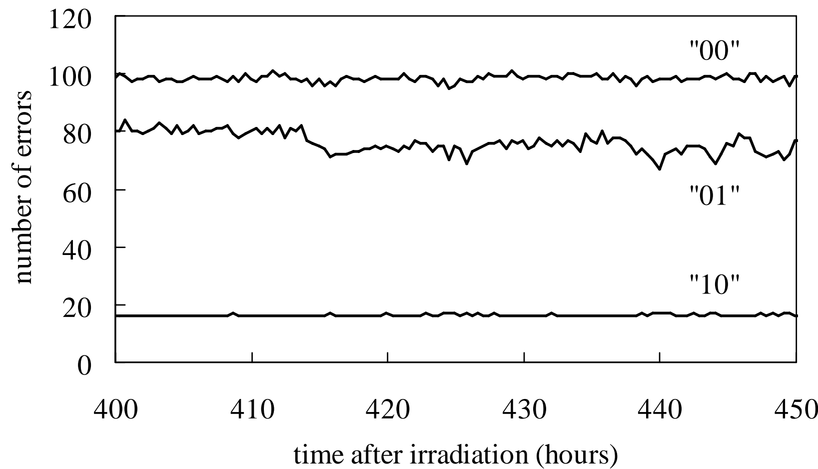


Fig. 5.2. Evolution of the number of errors for different program states in one single 8Gbit device from Vendor B. Qualitatively identical behavior were found for all irradiated devices (regardless of the vendor).

errors slightly fluctuates as a function of time, as illustrated in Fig. 5.2.

Let us now examine the results of the beam shift we perfromed in March 2009, where we tested the most advanced devices (feature size down to 48 nm).

It is interesting to evaluate the effects of technology evolution on neutron sensitivity. Figs. 5.3-5.4 show the raw cross section per bit (σ) attributable to neutrons, as a function of the cell feature size, in MLC NAND manufactured by vendors A and B. As seen in the graphs, for both manufacturers, the most affected bits are those belonging to the highest program levels, L2 and L3. For these bits, in both cases σ increases more than one order of magnitude in two generations.

As seen in Fig. 5.3, for MLC NAND Flash manufactured by vendor A, the increase in the error rate from 65 to 50-nm node is more than three orders of magnitude. The absolute value of σ reaches a value of 10^{-15} cm^2, for the worst-case pattern and smallest feature size. Fig. 5.4 depicts a similar figure for the samples produced by vendor B: in this case, the increase from one generation to the other is less large than in Fig. 5.3, and also the absolue value is lower, being less than 10^{-16} cm^2. It is worth to highlight that the worst-case values that we observe for the smallest feature size cells are about a factor of 100 smaller than for a typical SRAM cell.

Fig. 5.5 shows the cross section for raw bit errors in 48-nm memories manufactured by vendor C. Only the highest program level in these devices displayed a significant number of errors, while the lower V_{th} program levels and the erased one show less or no errors.

The cross sections previously described can be used to calculate the raw bit error rate on the field for a given location on the earth, using correspondent data on the neutron flux. Assuming a value of 13 $n{\cdot}cm^{-2}{\cdot}hour$ at NYC, the raw bit error rate due to atmospheric neutrons over a period of ten years in the worst case (Vendor A, level L3) is $1.13{\cdot}10^{-9}$, not

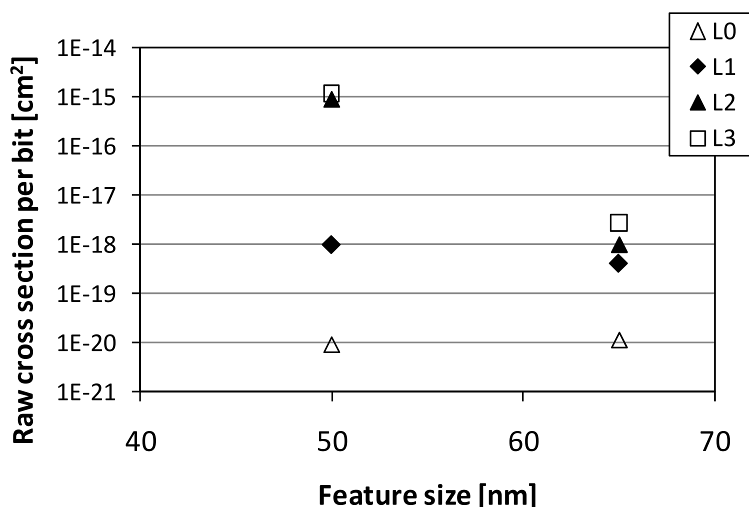


Fig. 5.3. Cross section for raw bit errors induced by wide-spectrum neutrons in 50-nm MLC NAND Flash memories from manufacturer A.

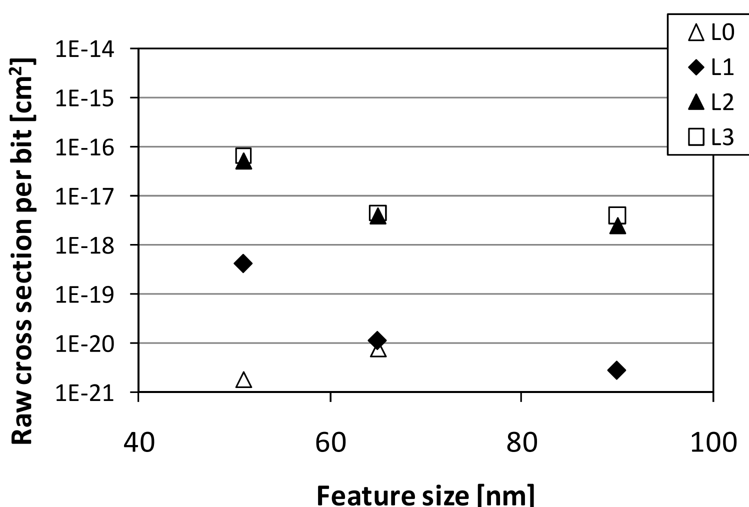


Fig. 5.4. Cross section for raw bit errors induced by wide-spectrum neutrons in 51-nm MLC NAND Flash memories from manufacturer B.

enormous but comparable to other mechanisms of bit errors [Mielke2008].

Let us consider the uncorrectable bit error rate that is the probability that more errors are generated in an ECC codeword than those that can be corrected. Assuming an ECC algorithm capable of correcting 8 bits and an ECC codeword of 539 bytes, as prescribed by the manufacturer datasheet, the uncorrectable bit error rate will be, according to the binomial distribution, much less than $1{\cdot}10^{-18}$. At avionics altitudes, the neutron flux can be 300 times higher than at sea-level, resulting in a worst-case raw bit error rate of $3.4{\cdot}10^{-7}$, which translated to uncorrectable bit errors is still well below $1{\cdot}10^{-18}$. The other tested memories exhibit much lower raw bit error rates.

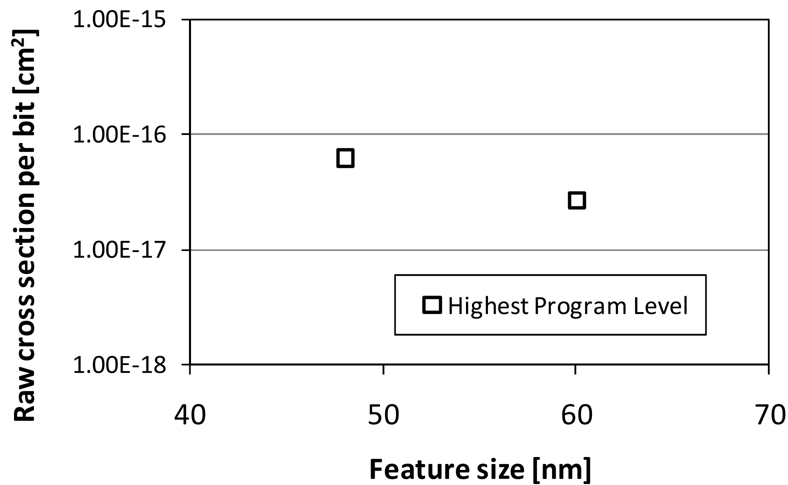


Fig. 5.5. Cross section for raw bit errors induced by wide-spectrum neutrons in 48-nm MLC NAND Flash memories from Vendor C.

5.3 Threshold voltage shifts

To deeply investigate the origin of the results shown in the previous section, we measured the threshold voltage of irradiated cells in some test chips (Table 5.I) and other commercial memories manufactured by Numonyx where we have access to Test Mode routines.

Figs. 5.6-5.7 show the cumulative probability distributions before and after exposure of the FG cell threshold voltage in 90-nm and 70-nm NAND devices irradiated at TRIUMF with a neutron fluence equivalent to ~102,000 years at ground level. As seen in the graphs, neutron irradiation results in the formation of a tail of low-V_{th} Floating Gate cells and this tail is much larger in irradiated devices than in reference ones. Interestingly, in devices with the smaller feature size the radiation-induced tails extend to lower V_{th} values (cf. Fig. 5.6 and Fig. 5.7).

The low-V_{th} tails cannot be attributed to intrinsic leakage phenomena, such as Stress Induced Leakage Current (SILC), for at least two reasons:

a) in reference devices the tails comprise much less FG cells with respect to irradiated devices, as we can see in Figs. 5.6-5.7
b) blocks programmed at different initial average V_{th} display tails with the same number of FG cells.

In case the tails were induced by SILC, the number of FG cells in the tails would be proportional to the electric field (i.e., with the cell V_{th}), as qualitatively illustrated in Fig. 5.8. On the contrary, each tail present in Figs. 5.6-5.7 contains the same number of cells, which is determined by the number of cells that were hit by neutron by-products.

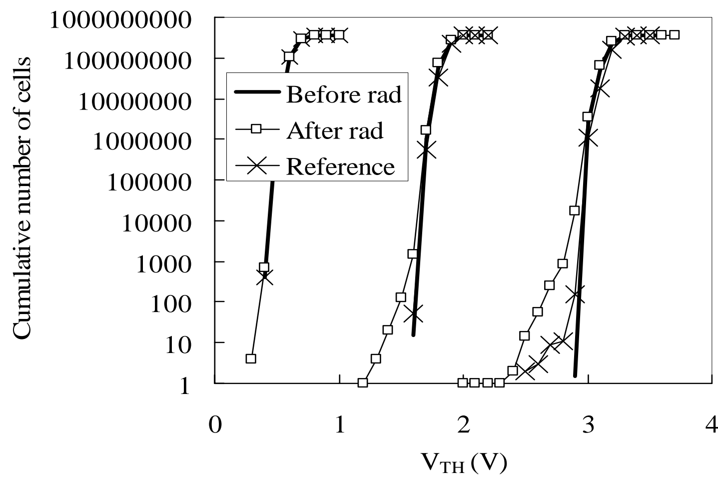


Fig.5.6. V_{th} cumulative probability distributions of three blocks for device 90-nm NAND by vendor C programmed at different initial V_{th}, before and after neutron exposure (performed at TRIUMF). Reference (non irradiated) devices are also shown.

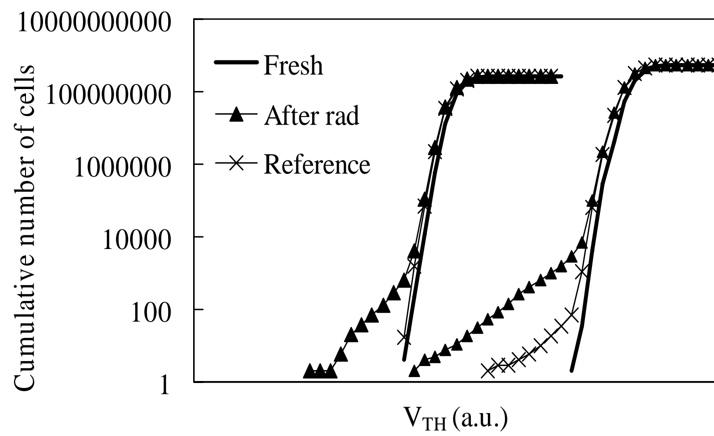


Fig. 5.7. V_{th} cumulative probability distributions of three blocks for device 90-nm NAND by vendor C programmed at different initial V_{th}, before and after neutron exposure (performed at TRIUMF). Reference (non irradiated) devices are also shown.

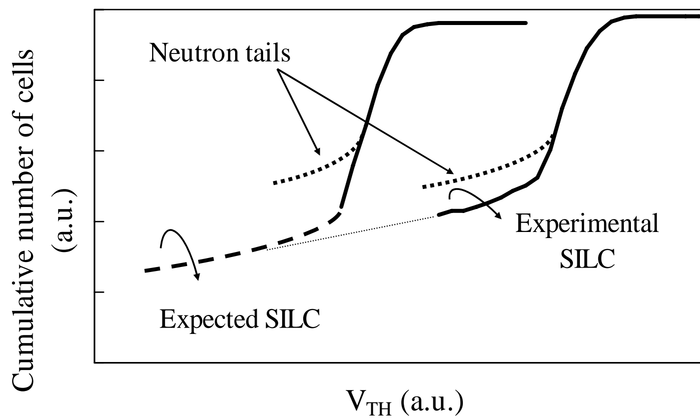


Fig. 5.8. Qualitative comparison between SILC and neutron-induced threshold voltage tails in FG cells.

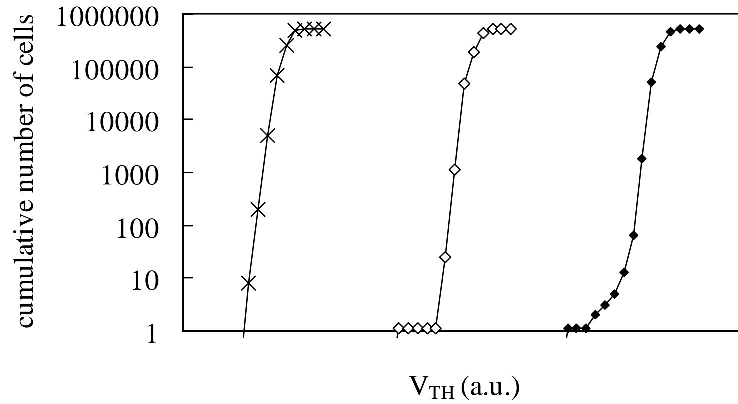


Fig. 5.9. Cumulative distribution of threshold voltage for a 90-nm NOR device after neutron exposure at TRIUMF.

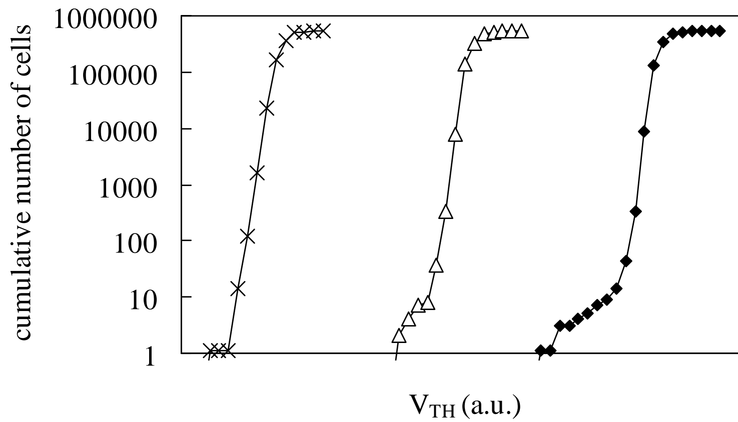


Fig. 5.10. Cumulative distribution of threshold voltage for a 65-nm NOR device after neutron exposure at TRIUMF.

Very similar results were also found in NOR devices, as illustrated in Figs. 5.9-5.10. For the same reasons as those previously observed, intrinsic leakage from the Floating Gate cells can be excluded for NOR memories as well. Figs. 5.9-5.10 show the cumulative V_{th} distributions for 90-nm and 65-mn NOR devices, respectively, after neutron exposure at TRIUMF. Post-rad distributions exhibit a tail in the V_{th} distribution, and, similarly to NAND memories, we notice a larger V_{th} shift in smaller feature size cells (Fig. 5.10) with respect to larger ones (Fig. 5.9).

Let us now examine how the threshold voltage shifts depend on the initial V_{th} of the cell. Fig. 5.11 illustrates the distribution of the V_{th} shifts (ΔV_{th}) in a 65-nm NOR device, as a function of the pre-rad V_{th}. As seen in the figure, ΔV_{th} is larger for FG cells programmed at higher average V_{th}.

It is worth to remark that all the FG cells in the tails, both in memories with NAND and NOR architecture, feature reduced noise margins. As a result, in the cells whose V_{th} is very close to the read voltage we will likely observe some read fluctuations similar to those seen in

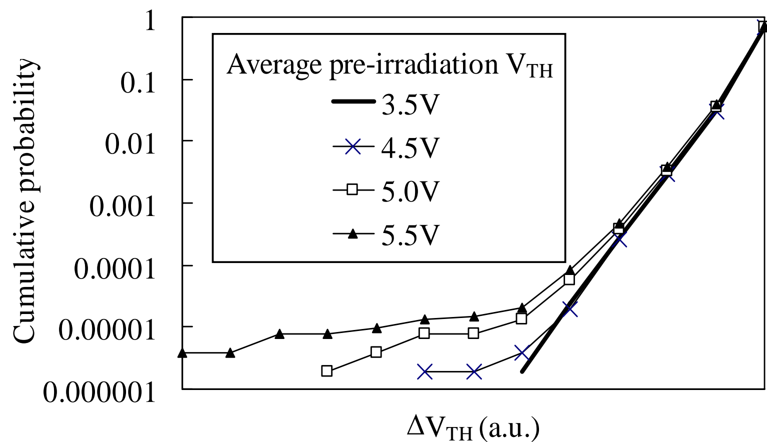


Fig. 5.11. Probability density functions for the threshold voltage shifts in T4 NOR devices (cf. Fig. 5.10).

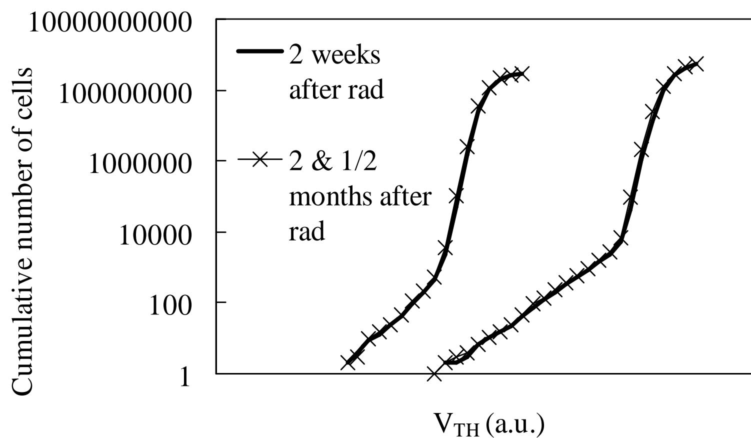


Fig. 5.12. V_{th} distributions right after neutron irradiation and after 2 months anneal at room temperature.

Fig. 5.3. On the contrary, the FGs whose V_{th} has been shifted to the lowest part of the tail, far from the read voltage, display a permanent bit flip. The threshold voltage shift is stable 2 months after the first measurement, as depicted in Fig. 5.12.

With regards to the more advanced devices we irradiated at the ISIS facility, the test mode results are depicted in Figs. 5.13-5.14.

Fig. 5.13 shows the pre- and post-irradiation V_{th} distribution for a 60-nm MLC NAND. Increasingly longer tails appear in the distributions for increasing threshold voltage; in other words, the higher the V_{th} of the hit cell, the larger the ΔV_{th}, while the number of FG cells in the tail are always the same no matter the V_{th}.

Interestingly, if we compare the V_{th} distributions before and after irradiation for two different technology nodes (60 nm and 48 nm), we find the result illustrated in Fig. 5.14. Note that the two devices were irradiated with the same neutron fluence. It is clear how both

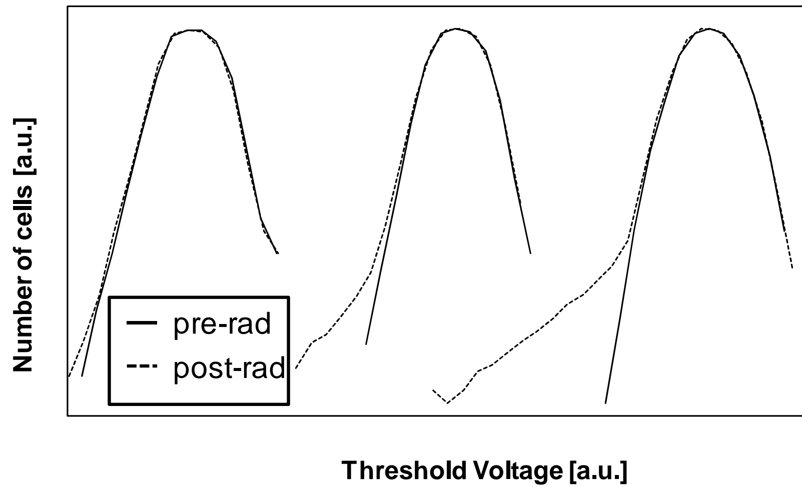


Fig. 5.13. Threshold voltage distribution for a 60-nm MLC NAND Flash Memory irradiated with wide-spectrum neutrons at ISIS.

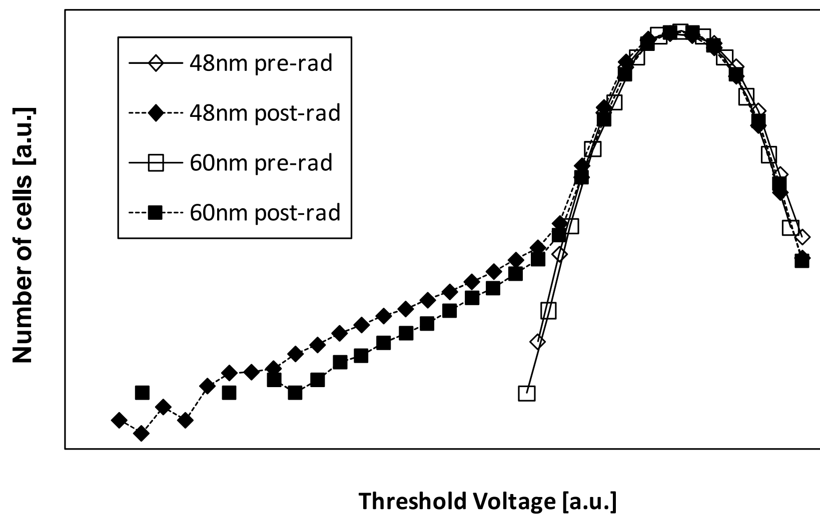


Fig. 5.14. Comparison between the threshold voltage distributions before and after wide-spectrum neutron irradiation for two MLC NAND Flash Memories with two different feature sizes.

the number of FG cells in the low-V_{th} tail and the maximum ΔV_{th} increase with decreasing feature size.

5.4 Discussion

Neutrons interact with the chip materials through nuclear reactions that generate charged secondary particles, i.e., heavy ions. As described in detail in previous sections, these

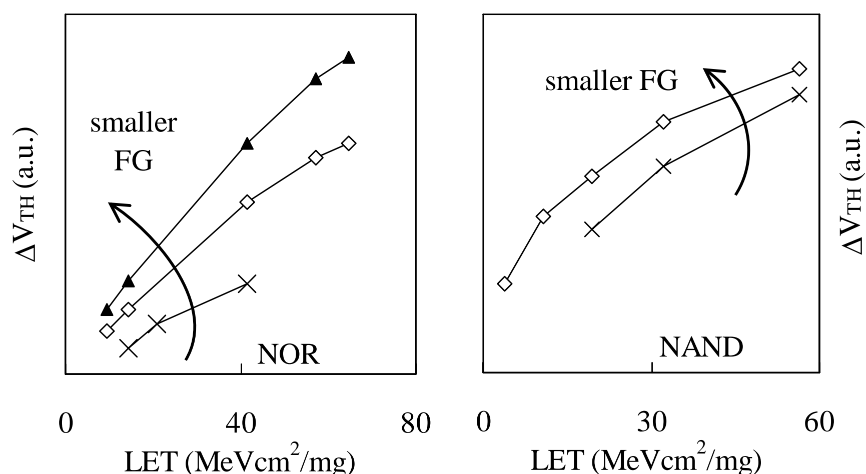


Fig. 5.15. Average ΔV_{th} for different technologies with NOR (left) and NAND (right) architectures, as a function of the heavy-ion LET.

secondary by-products can cross FG cells, inducing charge loss and, to a lesser extent, charge trapping in the oxides surrounding the FG [Cellere2001] [Oldham2006] [Guertin2006].

Extensive studies on the impact of heavy ions have shown that the amount of induced charge loss is more or less linear with the impinging particle LET, as shown in Fig. 5.14, for both NAND and NOR devices. Furthermore, the V_{th} shift is larger in FG cells with smaller feature size, and we will come back to this aspect at the end of this section.

In turn, the LET of the impinging particle depends on its mass and energy: the higher the mass, the higher the LET. The tails we observed in the figures in the previous section are more or less linear in a log-lin scale, meaning that the distribution of threshold voltage shifts induced by neutron byproducts is exponential. This distribution arises from the fact that the generated secondary byproducts have a wide spread in energy, range, and LET.

The dependence of charge loss on the electric field has been investigated in detail for heavy ions [Cellere2006b]. A larger electric field across the tunnel oxide increases the discharging current triggered by the ion. This translates into a higher charge loss, and explains very well the level dependence of the experimental data we provided in sections 5.2 and 5.3: both the numbers of raw bit errors and the low-V_{th} tails are more pronounced for the cells programmed at higher V_{th} (hence higher electric field).

Although neutron nuclear interactions with Si are by far the most common, byproducts originating from reactions with high-Z materials employed in the CMOS flow (such as Tungsten) can be very important, because they generate high-LET particles. Fig. 5.15 plots the LET as a function of energy for the by-products generated in neutron-Silicon nuclear reactions. In fact, by-products of neutron reactions with materials heavier than silicon need to be considered to justify the experimental data.

In principle, all the NAND memories share the same architecture, so it is at first surprising to see such large differences in their raw bit error rate. However, even relatively minor differences in the materials surrounding the FG or in the back-end can significantly

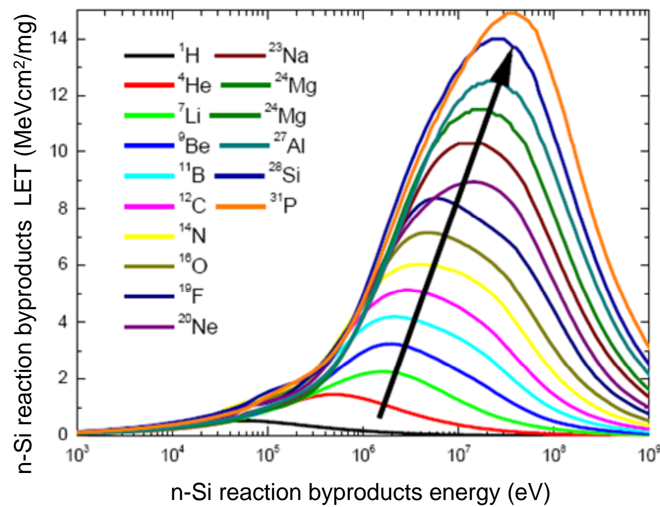


Fig. 5.16. Linear Energy Transfer as a function of energy for secondary by-products generated in neutron-Silicon reactions.

alter the spectrum of particles impinging on the FG. This argument can explain the observed differences in the raw cross section between the manufacturers examined throughout this work (see Section 5.2).

The other possibility is that the spectrum of particles generated by neutrons is the same in all the devices, but the FG sensitivity changes, even for nominally identical feature sizes, or the read window margin changes. This interpretation, however, is not fully convincing since experimental data obtained with heavy ions [Schmidt2008] on different vendors do not exhibit significant differences, as far as the FG cross section is concerned.

Finally, with regards to the feature size dependence, the results shown in Table 5.III, as well as the scaling trend illustrated in Figs. 5.3-5.5 clearly point to an increased number of raw bit errors as the feature size is scaled, as predicted in [Butt,Alam2008]. The phenomenon can also be seen in terms of V_{th} shifts (Figs. 5.13-5.14): the smaller the FG cell, the larger the ΔV_{th}. This trend reflects the fact that the charge used to store a bit of information decreases with each new generation, whereas the ion track remains the same. However, changes in the materials, for instance the replacement of Tungsten with lighter elements, like Cobalt and Copper, could offset this trend. In addition, SLC devices are less sensitive than MLC (for the same technology node) (Table 5.III) because of their larger noise margin.

5.5 Summary

We have shown that atmospheric neutrons can induce observable effects in Flash memories, threshold voltage shifts that, if large enough can produce read errors. In fact, neutrons can trigger nuclear reactions inside the device, generating secondary byproducts that can lead to charge loss and, to a lesser degree, charge trapping in the Floating Gate

cells. These findings pose new issues for the use of Flash memories in dependable applications at terrestrial level (medical, automotive, banking, etc.).

Our experimental results showed that the cross section for raw bit errors increases with decreasing feature size, with large differences from vendor to vendor, and MLC devices display larger sensitivity with respect to SLC ones (for the same technology node). From the data and discussion presented in this chapter, it is clear why neutron-induced errors are present in state-of-the-art technologies but were not in older ones. In older devices, the errors were simply not detectable, because in larger FG cells the threshold voltage shifts were too small to result in observable errors.

The good news is that the cross section for neutron-induced raw bit errors is low enough not to threat the capability of current ECC schemes. One thing is certain: the sensitivity to atmospheric neutrons is expected to increase in the future technology generations. In some conditions, the neutron threat will likely be of some significance, if compared to the other mechanisms that can lead to bit errors in Flash devices (program disturb, erratic tunneling, stress induced leakage current, etc.). Despite this, neutron bit error rate will likely remain within the limits of capability of ECC schemes, at least in the foreseeable future.

Chapter 6

Temperature Dependence of Soft Error Rate

SRAMs are one of the most common benchmarks to assess the Soft Error Rate (SER) of a given CMOS technology node. They are widely used in electronics, for instance in the page buffer of Flash memories.

Several electronic circuits are required to operate in wide temperature ranges, especially for high-performance and dependable applications (e.g., space, automotive, military). However, SER testing is usually performed at room temperature and JDS89a standard does not even mention temperature, differently from SEL experiments that must be conducted at high temperature.

Few reports are available in the literature describing SER as a function of temperature. This chapter aims at identifying the main factors that influence the Single Event Upset susceptibility of SRAMs. New experimental data are provided on neutron and alpha-particle irradiations. Furthermore, SPICE simulations and analytical modeling are used to assess the critical charge and collection efficiency as a function of temperature, in order to interpret the experimental data.

6.1 Devices, irradiation, and experimental

For this work we used commercially-available SRAM chips manufactured by different vendors, whose features are illustrated in Table 6.I. All the tested memories have the same size (4 Mbits), the same organization (8 x 512 Kbits) and were purchased from electronic components distributors during 2007. The likely CMOS technology node of the samples were evaluated from the die size: devices with the same die area have been associated to the same CMOS technology node.

The memories were irradiated with both neutrons and alpha particles.

Neutron irradiations were performed at the ISIS facility of the Rutherford Appleton Laboratory, Didcot, (UK). ISIS is a spallation neutron source, which uses 800-MeV protons to produce neutron beams with different energy spectra characteristics.

Both the VESUVIO and ROTAX instruments were used in this work.

- The VESUVIO beam adequately matches the terrestrial neutron flux with an acceleration factor between 10^7 and 10^8, containing both high-energy and thermal neutrons (see Fig. 6.1). The VESUVIO beam can be correlated with the LANSCE facility flux (the *de facto* standard for soft error measurements [LANSCE2008]) using the LANSCE-equivalent flux, which is a measure that accounts for the effectiveness of a beam in producing single event effects with respect to LANSCE. The LANSCE-equivalent flux in the sample positions has been calculated according to [Platt2008] and is about $5.5 \cdot 10^4$ n/cm^2/s.
- The ROTAX beam features only the low energy part of the spectrum (thermal and epi-thermal neutrons).

In addition to neutron sources, 5.4-MeV alpha-particles from an Am-241 radioactive source were used to irradiate those memories, where exposing the die was feasible at low cost without rebonding (Device E, which was packaged in DIL, was delidded through

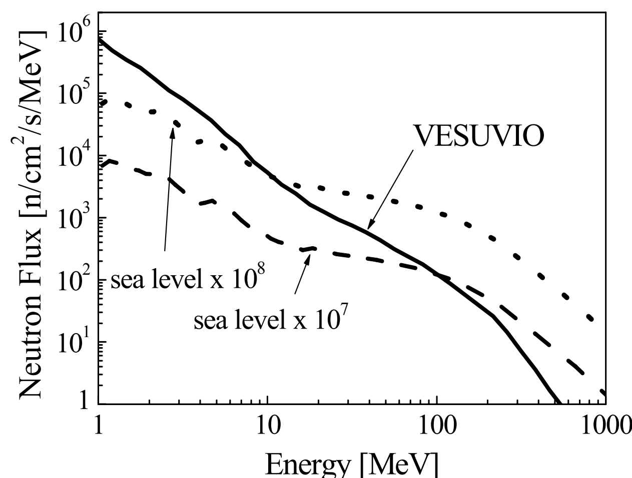


Fig. 6.1. VESUVIO differential neutron flux as a function of energy, compared to the terrestrial flux (multiplied by 10^7 and 10^8).

chemical attack).

The memories were programmed (with checkerboard pattern) and periodically read under irradiation at different operating voltage and temperature. Heating elements placed around the devices were used to raise the chip temperature during exposure. The temperature of the memories was constantly monitored during irradiation. Also the current drawn by the devices was measured under exposure to detect latch-up occurrence.

Finally, SPICE simulations have been performed to evaluate both the behavior of a single transistor and of an entire SRAM cell at different temperatures, using freely available models of different technologies available through MOSIS [MOSIS2008].

6.2 Experimental results

Some of the irradiated parts (Devices D and E) exhibited frequent Single Event Latch-up with wide-spectrum neutrons even at room temperature and at the lowest possible supply voltage, and were therefore discarded from the analysis. It is interesting to remark that SEL can lead to more severe consequences than soft errors, possibly to the destruction of the component, and commercially available parts may still suffer from this problem, also in relation to neutrons.

One of the tested memories (Device C) was sensitive to thermal neutrons, due to the likely presence of BPSG inside the chip, and was separately studied to analyze the temperature dependence of the errors induced by thermal neutrons.

No dependence of the error rate on the supply voltage was observed for devices A and B with high-energy neutrons, whereas C exhibited increased sensitivity at lower supply voltage with thermal neutrons (Fig. 6.2). We do not have detailed architectural information on these samples, but, given the results, we can speculate that devices A and B are equipped with internal voltage regulators that maintain the supply voltage of the memory

Device	Vendor	Size	Supply Voltage	Temperature Range	CMOS node
A	STM	4 Mbit	3V	0 to 70°C	180nm
B	Renesas	4 Mbit	3V	-40 to 85°C	180nm
C	ISSI	4 Mbit	3V	0 to 70°C	130nm
D	Cypress	4 Mbit	3V	-40 to 85°C	90nm
E	BSI	4 Mbit	2.4-5.5 V	0 to 70°C	250nm

Table 6.I. Features of the SRAM devices used throughout this work.

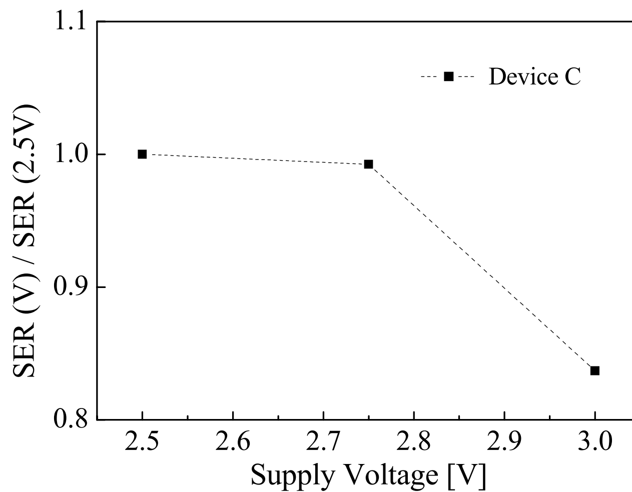


Fig. 6.2. Experimental soft error rate as a function of supply voltage normalized to V_{dd}=2.5V for Device C irradiated with thermal neutrons at room temperature.

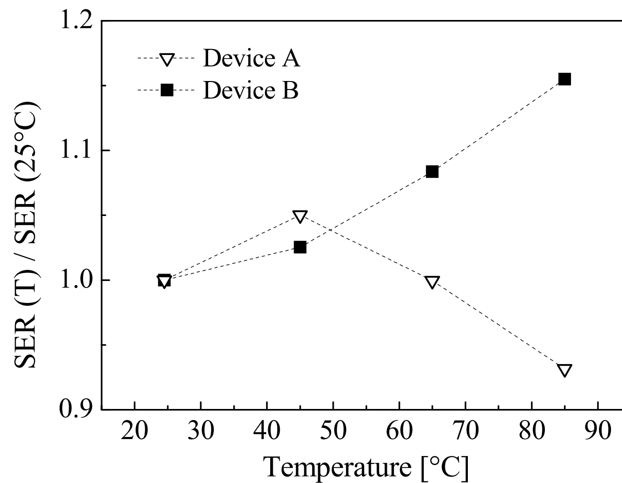


Fig. 6.3. Experimental cross section per bit as a function of temperature during high-energy neutrons exposure for Devices A and B.

cells always at the same level, irrespective of the external bias; on the contrary, in device C the cell voltage varies with the external supply voltage.

In the following, we will analyze the dependence of the SER on the temperature. Fig. 6.3 displays the normalized error rate as a function of temperature for Devices A and B. Thousands of events were collected for each experimental point in order to achieve a good statistical accuracy, in order to observe even small variations (> 2%). Besides, irradiation runs at different temperatures were carried out in different orders to detect possible temperature hysteresis effects, which were not observed. The two memories feature a different behavior. In Device A, the cross section slightly decreases (< 7%), whereas in Device B, SER increases by 15% in the temperature range 25-85°C. It is interesting to remark that these devices were manufactured in the same technology node by different foundries.

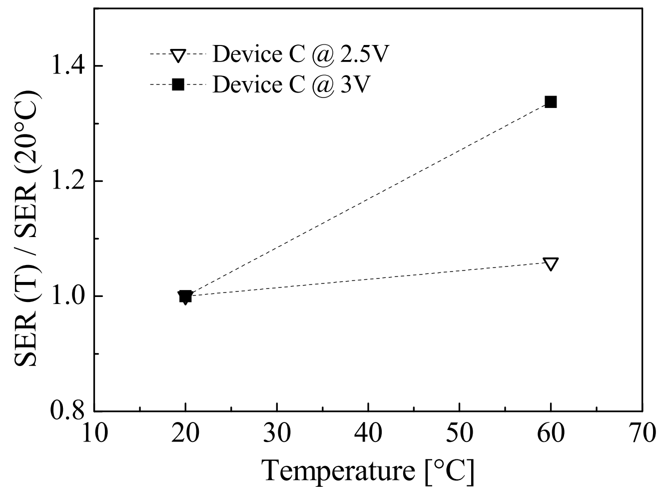


Fig. 6.4 Experimental soft error rate normalized to T=20°C as a function of temperature during thermal neutrons exposure for Device C.

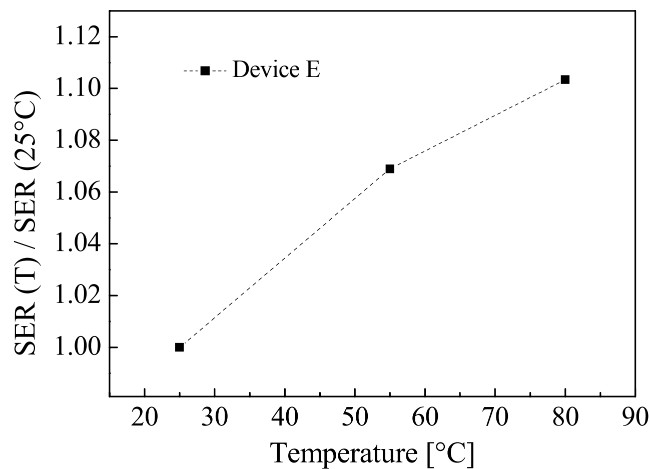


Fig. 6.5. Experimental soft error rate normalized to T=25°C as a function of temperature during alpha-particle exposure for Device E.

Fig. 6.4 displays the normalized error rate at 20°C and 60°C for Device C irradiated with thermal neutrons at two different supply voltages. The dependence on temperature is greatly enhanced at higher supply voltage (even though the overall error rate is lower at high V_{dd}, Fig. 2). At 2.5V the increase in sensitivity is about 6%, while at 3V the error rate at high temperature is more than 30% larger than that at room temperature for the same voltage.

Fig. 6.5 illustrates the error rate as a function of temperature for Device E irradiated with alpha particles. The alpha-sensitivity increases by 10% from room temperature to 80°C.

6.3 Discussion

As we just described, different devices exhibit different SER trends with respect to temperature. According to the information we gathered from the memory datasheets, all the devices should feature 6-transistors cells, so the observed changes are not related to increasing resistance of the pull-up resistors as in [Sexton1989].

A full cell 3D or a mixed-mode simulation would be needed to accurately reproduce the temperature dependence. This would require knowledge of the memory cell structure and doping profiles, which is obviously not available for commercial memories. The purpose of this discussion is therefore to pinpoint the main parameters governing the SER temperature dependence. To this end, we will use a simplified approach that combines SPICE simulations and analytical modeling. The conclusions we will draw are mostly qualitative, but, nevertheless, can provide good insight.

We may relate the SER temperature dependence on either differences in the MOSFET characteristics, leading to a change in the circuit response, or to alterations in the particle-induced pulses.

Despite the difficulties in defining the concept of critical charge [Dodd1995], the SER of a memory chip (even in scaled devices [Heijmen2005]) can still be fitted by the well-known empirical expression [Hazucha,Svensson2000], where the temperature (T) dependence has been put in evidence:

$$SER(T) = \kappa A_{diff,n} \exp\left(-\frac{Q_{crit,e}(T)}{\eta(T)} \right) \qquad (6.1)$$

κ is an overall (technology-dependent) scaling factor, $A_{diff,n}$ is the diffusion area, $Q_{crit,e}$ is the critical charge, and η is the charge collection efficiency. The last two parameters may vary with temperature, as indicated in (6.1). The critical charge will be calculated through SPICE simulations by injecting a current pulse in the cell (Section III.B). The collection efficiency η represents a measure of the charge collected by the circuit node after an ion strike and will be discussed in Section 6.3.3. For simplicity, we will focus on strikes occurring in or near the drain of the off NMOSFET, which still accounts for most of the SEUs even in scaled devices [Correas2007].

6.3.1 Temperature impact on the circuit response

MOSFETs have a positive temperature coefficient, meaning that the drive current decreases as temperature increases. This reduction is mostly due to a lower mobility at high temperature because of the increased phonon scattering. For instance, the hole mobility temperature dependence (as a function of doping) in bulk Silicon can be expressed by the following empirical formula [Arora1982]:

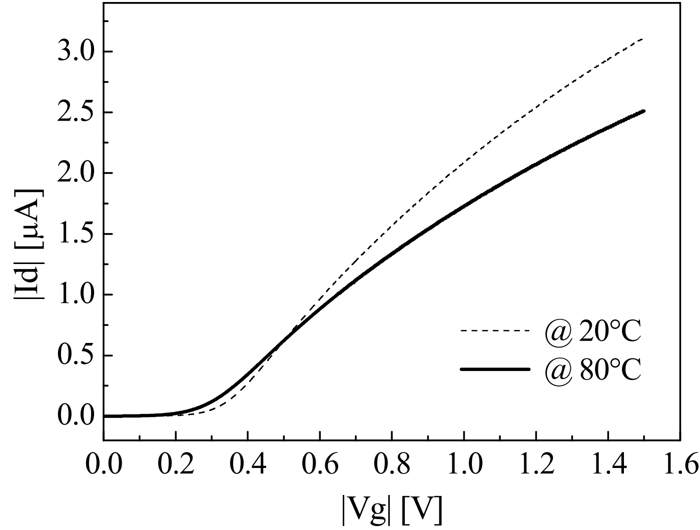


Fig. 6.6. Simulated I_{ds}-V_{gs} characteristic for a PMOSFET (180 nm) (V_{ds} = 25 mV), performed at 20°C and at 80°C.

$$\mu_p = 88 \cdot T_n^{-0.57} + \frac{1.36 \cdot 10^8 \cdot T^{-2.33}}{1 + \frac{N}{1.26 \cdot 10^{17} \cdot T_n^{2.4}} \cdot 0.88 \cdot T_n^{-0.146}} \tag{6.2}$$

where T is the temperature (in °K), T_n is the temperature divided by 300°K, and N is the doping concentration. A similar expression exists for the mobility of electrons [Arora1982]. Other scattering mechanisms come into play (surface roughness, carrier-carrier scattering, quantum effects) to determine the mobility in the channel, which can be lumped together in the following simplified equation, used also by BSIM3 and BSIM4 models:

$$\mu = \mu(T_0) \cdot \left(\frac{T}{T_0} \right)^{\mu Te} \tag{6.3}$$

where T_0 is a reference temperature and μTe a fitting parameter. The threshold voltage depends on the temperature as well, although in a less pronounced way, causing the MOSFET temperature response to be dominated by mobility changes. Temperature also impacts the junction capacitance, although in a minor way.

Some of the most interesting experimental data we collected (Fig. 6.3) are relative to the 0.18 μm CMOS node, so this feature size will be used in the following SPICE simulations. Data on 90-nm cell will also be shown to illustrate scaling trends. Fig. 6.6 shows the simulated I_{ds}-V_{gs} characteristics of a 180-nm PMOS transistor in the linear region (V_{ds} = 25mV). The electrical characteristic at high V_g shows a decrease in I_{ds} current

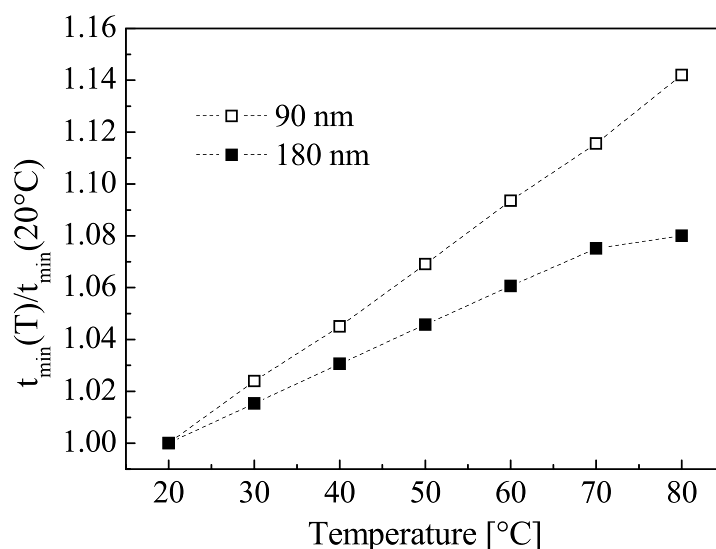


Fig.6.7. Simulated minimum write pulse needed at the word line for a 6-T SRAM cell as a function of temperature.

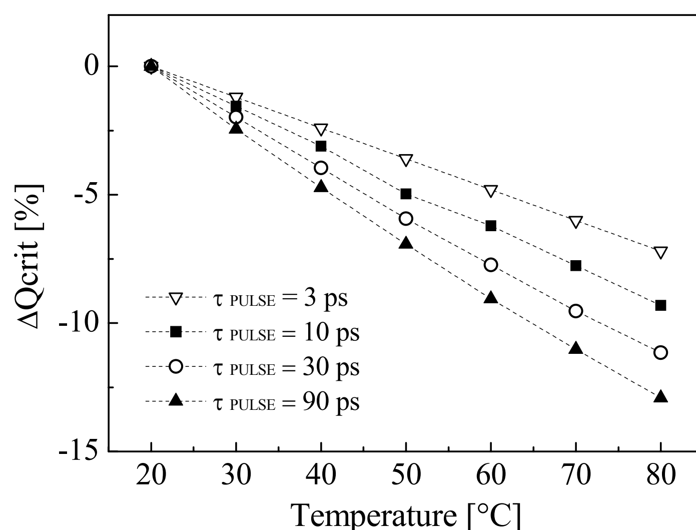


Fig.6.8. Simulated percentage variation in the critical charge as a function of temperature, normalized to 20°C for different pulse widths (180 nm SPICE models, V_{dd} = 1.5 V).

at high temperature compared to room temperature. This means that the PMOS at higher temperature is less strong than at room temperature, and this has a detrimental effect on the SER of the memory cell.

On the other hand, we can simulate the behavior of an entire 6-T SRAM cell. Fig. 6.7 reports the speed of the cell at different temperatures; in particular, the figure shows the simulated minimum pulse width duration (t_{PW}) that is required at the word line to write the cell. The minimum t_{PW} monotonically increases with temperature, for both a 90-nm and a 180-nm cell, the memory cell resulting slower at higher temperature.

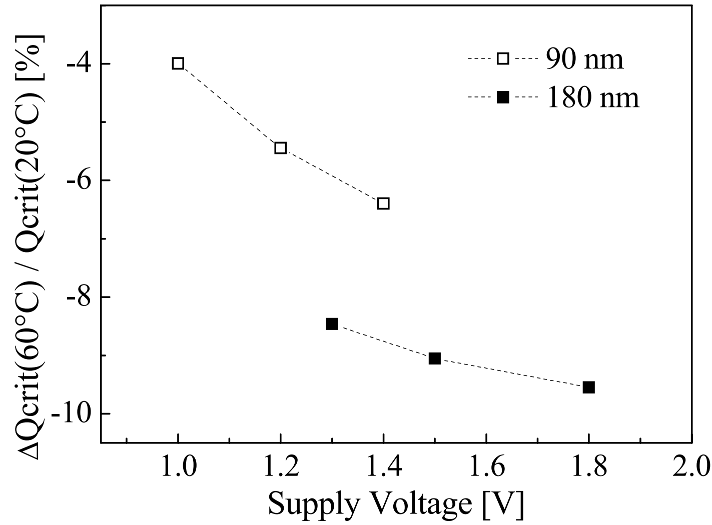


Fig. 6.9. Simulated percentage variation in the critical charge at 60°C as a function of supply voltage normalized to ΔQ_{crit} at 20°C, for a 6-T SRAM cell.

If we consider the two effects we described so far, their contributions go towards opposite directions, concerning the soft error sensitivity. On one hand, the ability of the PMOSFET to restore the state of the struck cell is reduced at high temperature, due to the lower drive current of the device, which has a detrimental effect on the radiation sensitivity of the cell. On the other hand, the speed of the cell is reduced at high temperature, which should be beneficial for the error rate, since pulses injected by ionizing particles propagate more slowly and the ion-induced spike is less likely to be latched.

These effects can be accounted for in the following formula [Roche1999]:

$$Q_{crit} = C_n \cdot V_{dd} + t_{FLIP} \cdot I_{RESTORE} \tag{6.4}$$

where C_n is the total capacitance of the struck node, t_{FLIP} the flipping time, and $I_{RESTORE}$ the restore current. Also C_n depends on temperature, since, for instance, the size of the depletion regions varies, as we shall see later.

Fig. 6.8 displays the simulated critical charge of a memory cell as a function of temperature and pulse duration. The current pulse injected into the sensitive node is modeled through an exponential multiplied with a power law [Heijmen2006]:

$$I_{pulse}(t, \tau_{pulse}, Q) = \frac{2}{\sqrt{\pi}} \cdot \frac{Q}{\tau_{pulse}} \cdot \sqrt{\frac{t}{\tau_{pulse}}} \cdot \exp\left(\frac{t}{\tau_{pulse}}\right) \tag{6.5}$$

where τ_{pulse} is the width of the current pulse and Q is the total amount of injected

charge. τ_{pulse} has been varied to simulate the effect of current pulses with different durations, corresponding to strikes in different locations/angles, etc. [Palau2001]. As observed in Fig. 6.8, SPICE simulations show a net decrease of the critical charge for long pulses, meaning that at high temperature the detrimental reduction in the PMOSFET restore current overcomes the beneficial (from the SER standpoint) reduction in the cell speed. The effect is less pronounced for short pulses. From a circuit-only perspective (i.e., neglecting the impact of temperature on the pulse amplitude, shape, and duration), we expect that the error rate due to particles going through the drain is less affected by temperature than that due to particles passing close to the drain.

Fig. 6.9 shows the simulated dependence of the critical charge at 60°C on the supply voltage. The impact of temperature is enhanced at high voltage. This may explain the experimental data illustrated in Fig. 6.4, where we observe an enhanced temperature dependence at high supply voltage.

The above discussed results are not restricted to these models. Indeed, we performed the same simulations with parameter sets from other vendors and belonging to different technology nodes and found qualitatively the same dependences.

Besides MOSFET drive current, temperature also affects the resistivity of the interconnects, further reducing the speed of the cell (this is not considered in our simulations but would likely go in the direction of improving the SER susceptibility).

6.3.2 Temperature impact on the particle-induced current pulse

In addition to critical charge, the current pulse induced by the striking particle may be affected by temperature as well.

Charge collection depends on several factors related to the impinging particle (LET, energy, angle, secondary particles), device structure (size, doping, etc.), and external circuit (node impedance). To add more complexity, several charge transport mechanisms are involved in determining an upset, from simple drift to ambipolar diffusion. It is almost impossible to analytically account for all the different terms that determine the charge collection in a struck cell, but we can capture the main parameters which show a dependence on temperature.

For strikes passing through the drain, charge is collected at a sensitive node in two stages: drift and diffusion [Edmonds1991]. Roche et al. [Roche1999] demonstrated that the peak of the drift current is expressed by the following equation:

$$I_0 = < \mu E_{field} > LET \qquad (6.6)$$

Since mobility decreases with temperature and the electric field E_{field} weakly depends on temperature, the peak of the drift current decreases at high temperatures. This has been

Parameter	T dependence	Impact on SRAM SER	Variation Range*	Ref	Main driver	Description
LET	≈	≈	< 1.5%		E_g	Linear energy transfer
I_{DS}	↓↓	↑↑	< 20%		$\mu_{channel}$	MOSFET drain current
t_{write}	↑↑	↓↓	< 8%		$\mu_{channel}$	Cell write time
I_0	↓↓	↓↓	10% to 20%		μ_{track}	Peak drift current
x_d	↑	↑	< 2%			Depletion region width
$l_{funneling}$	↑↓	≈	-3% to 3%		μ_e/μ_h	Funneling length
L_{diff}	↑↓	↑↓	n.a.	[Edmonds1991]	D*, τ	Diffusion length
D*	↑↓	↑↓	-7% to 11%		$(\mu_e\mu_h)/\mu_e+\mu_h$	Ambipolar diffusivity
τ	↑	↑	n.a.	[Guo2004] [Tyagi1983] [Goebel1992] [Huldt1979] [Lochmann1980]	SRH(T), Auger(T)	Minority carrier lifetime

Table 6.II. Main factors impacting the Soft Error Rate temperature dependence.

both verified with 3-D simulation tools [Truyen2007] and experimentally observed in [Guo2004],[Laird2008] (in diode structures and in inverters, respectively). Also the LET varies with temperature, as the bandgap increases with it, but the variation is modest.

The size of the depletion region is weakly affected by temperature. Indeed x_d depends on the square root of the applied reverse bias plus the built-in potential V_i , the last term determining the temperature dependence to a first order. Calculating the depletion width for a large range of conditions, we found that the DR only marginally (< 1%) shrinks at high temperature. Unless otherwise stated, in the following the reported maximum percentage changes refer to the 20-80°C temperature range.

Funneling (which may not necessarily impact the SER [Dodd1995]) depends on the ratio between the mobility of holes and electrons, μ_e/μ_h [Arora1982],[Edmonds1991] according to the equation proposed by Edmonds:

$$Q_{tot} = Q_{drift}\left(1 + \frac{\mu_e}{\mu_p}\right) + Q_{diff} \tag{6.7}$$

We studied the term μ_e/μ_h as a function of temperature, using Eq. (6.2) and its counterpart for electrons. For doping levels greater than 10^{18} cm^{-3}, the ratio grows, for lower levels, it either decreases or is non-monotonic in the range we consider. In any case, the variation is smaller than 5%.

After the first prompt collection, charge can be collected by diffusion in the vicinity of the depletion (and funnel) regions. Actually, diffusion may be the main driver for those strikes that do not intercept the drain, which are the majority with secondary byproducts of neutrons [Palau2001]. The width of the regions that can provide electrons depends on the diffusion length, $L = \sqrt{D^* \cdot \tau}$, where D^* is the ambipolar diffusion constant, and τ is the minority carrier lifetime in the bulk p substrate.

D^* increases or decreases with temperature, depending on the doping level (11% with N=10^{18} cm^{-3}, -9% with N=10^{17} cm^{-3}), according to the following expression:

$$D^* = {2kT}/{q} \cdot \frac{\mu_e(T) \cdot \mu_h(T)}{\mu_e(T) + \mu_h(T)} \tag{6.8}$$

The minority carrier lifetime τ is determined by Shockley-Read-Hall (SRH) and Auger recombination, which both increase with T. The net result is an increase in the diffusion length, but since there is no consensus on the lifetime dependence on temperature [Huldt1979] [Lochmann,Haug1980] [Tyagi,vanOverstraeten1983], no estimate is possible.

6.3.3 Soft error rate versus temperature

As shown in the previous sections, temperature may impact the SER in many different ways. In particular, temperature effects can be divided in two main categories, the first connected with the circuit response, and the second regarding the shape of the particle-induced current transient. In other words, temperature alters independently:

a) the characteristics of the memory cells, in terms of write speed and strength of the restoring device;
b) the current pulse generated by the impinging particles affecting the transport properties of the charge generated by ionizing particles.

The most important parameters are summarized in Table 6.II, where the temperature dependence, the effect on the SER, the expected variation range, and the main driving phenomena of these factors are highlighted.

Our analysis shows that there is no clear dominant factor. Some of the terms we analyzed go in the direction of raising the sensitivity at high temperature (transistor drain current); some others have the opposite effects (drift collection); and some others again (ambipolar diffusion) may raise or lower the SER depending on technological parameters that are usually unknown, such as substrate doping and well engineering.

The behavior emerging from Table 6.II is confirmed by the experimental data, which

show either a SER increase or a slight decrease (Figs. 6.2 and 6.3), even though the first behavior seems to be prevalent.

6.4 Summary

In the work presented in this chapter, we irradiated different SRAMs with neutron beams (both thermal and wide-spectrum) and with alpha particles, studying the impact of temperature on the soft error rate. We observed that, depending on the tested vendor, temperature may or may not increase soft error sensitivity, and different behaviors were found even in devices belonging to the same technology node.

On one hand, SPICE simulations were used to investigate the temperature dependence of circuital parameters, like the feedback time and the restoring current of the cell. On the other hand, the shape and magnitude of the particle-induced transient current was discussed as a function of temperature.

The performed analysis shows that no dominant parameter exists, and that the temperature dependence results from a complex mix of factors. The variability in the temperature response experimentally observed was attributed to the balance of contrasting factors (some of which strongly depend on technological parameters), such as cell slowing down and increased diffusion collection with increasing temperature.

As a result, contrary to Single Event Latch-up, it is not possible to identify a worst-case condition for Soft Error Rate experiments with respect to temperature. Anyway, given the variety of different behaviors that were experimentally observed, we can conclude that SER testing at high temperature is recommended for those devices that are expected to operate in wide temperature ranges. In fact, our data suggest that performing the experiments at room temperature may result in underestimation of the terrestrial SER (of less than 20%) in the operating range typical of commercial devices.

Conclusions

This work provided several original contributions to the field of radiation effects in Flash memories and SRAMs. A thorough investigation of Commercial-Off-The-Shelf Flash memories has been performed, using x-rays, heavy ions, and neutrons, to emulate both the space and terrestrial environments.

With regards to total ionizing dose results (Chapter 2), the failure doses of the floating gate memory matrix, the charge pump circuitry, and the row decoder were assessed by selectively irradiating the device building blocks, in contrast to the common procedure of exposing the whole device. As already reported in the literature, the charge pump circuitry has been confirmed to be one of the weakest part. However, this work demonstrated that raw bit errors in the floating gate array may appear even before the charge pump failure, due to charge loss and charge trapping.

In Chapter 3, dedicated to single event effects, the role of the page buffer was elucidated and the dependence of page buffer errors on the operating conditions (e.g., the read activity) during heavy-ion irradiation was clarified. Interestingly, it has been shown that depending on the ion species, on the program pattern, and on the way the memory is operated during exposure, the sensitivity of either the floating gate array or the page buffer may be predominant. An ‘effective’ device cross section has been proposed that measures the device sensitivity, accounting for the main usage patterns.

Annealing effects in floating gate errors have been discussed several times before this thesis work after heavy-ion exposure, but apparently collided with observations on the floating gate charge loss. Innovative experiments have been performed in this work (Chapter 4) putting in evidence how charge loss from the floating gate and charge trapping in the cell oxides can coexist, and nicely explain the experimental observations. In fact, even a

relatively small threshold voltage shift during the annealing process can cause a large number of raw bit errors to either disappear or, interestingly, also to appear, after exposure.

Chapter 5 shows for the first time that atmospheric neutrons are able to induce observable effects in advanced Flash memories. This was predicted before, based on heavy-ion data, but never experimentally measured. We started examining the raw bit errors induced by neutron irradiation and then we focused on the threshold voltage distributions before and after exposure. Even though the results illustrated in this section raise new issues on the use of Flash memories at sea level, it has been demonstrated that the neutron bit error rate is not so large to threaten current error correction code schemes, which are strictly required in these devices due to intrinsic bit error mechanisms.

The final chapter illustrated the main factors determining the temperature dependence of soft error rate. The section is focused on SRAM cell, which is present in virtually all integrated circuits, for instance in the page buffer of Flash memories. Experimental results on different commercial samples, SPICE simulations, and analytical modeling agree on the fact that no clear trend exists due to the complex mixture of parameters at play. Even though the current JEDEC standard for soft error rate measurement does not consider temperature as key factor, the analysis has shown, on the whole, that performing soft error rate testing at room temperature may result in an underestimation up to 20% in the 20-80°C operating temperature range, typical of commercial devices.

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