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AM-PM and AM-AM Distortion Reduction Techniques for Fully-integrated Silicon-Germanium 5G Power Amplifiers

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Abstract

The fifth generation cellular network technology (5G) is expected to ramp up during 2020. To accommodate ever increasing bandwidth requirements, the 5G employs high spectral efficiency modulation schemes and carrier frequencies in the millimeter-wave frequency (mmWave), where large portions of unused spectrum are available. Since the path loss increases with the frequency, massive multiple-input multiple-output (MIMO) technologies will focus the RF energy onto the receiver using hundreds of antenna elements. Each antenna element is driven by a power amplifier (PA) which, being the last element in the transmit (TX) chain, dominates the efficiency and linearity performance of the whole transmitter. Moreover, higher order modulation schemes are more taxing in terms of linearity requirements both as to amplitude-to-amplitude (AM-AM) and to amplitude-to-phase (AM-PM) distortion.

This thesis focuses on circuit solutions to obtain high linearity PAs suitable for high data rate mmWave applications. Several fully-integrated silicon-germanium (SiGe) PAs targeting 20 dBm output power are proposed. Starting from a class J design used as a reference, the main source of AM-PM distortion is demonstrated to be the BJT input impedance variation with the input signal amplitude. As a first solution to address the issue, a ladder filter based input matching network (IMN) is used to offer a 5-fold improvement on AM-PM distortion over a simple resonant IMN with minimum PAE penalty. To further reduce the impact of nonlinearities in the transmitted signal, another PA is proposed, combining the linearity of a CMOS predriver with the high power handling capability of a SiGe output stage. This PA features 1.5° AM-PM distortion at 1-dB compression point (P_{1dB}) with 20 % maximum PAE.

Those solutions seem lead to a reduction in efficiency when continuous-wave measurements are considered. However, compared to the reference designs, less backoff is needed for the same amount of error vector magnitude (EVM) and thus, higher average efficiency can be achieved. Other techniques such as changing the bias point of the PA with the signal envelope or the Doherty amplifier can also be used to recover the lost efficiency.

Sommario

Lo standard di quinta generazione per reti cellulari (5G) subirà un'accelerazione durante il 2020. Per far fronte ai requisiti di banda sempre in aumento, il 5G fa uso di schemi di modulazione ad alta efficienza di spettro e frequenze portanti nelle onde millimetriche, dove sono ancora disponibili ampie bande inutilizzate. Dal momento che l'attenuazione in spazio libero aumenta con la frequenza, soluzioni massive a ingressi e uscite multiple (MIMO) concentrano l'energia RF sul ricevitore utilizzando centinaia di elementi di antenna. Ciascuna antenna è pilotata da un amplificatore di potenza (PA) che, essendo l'ultimo elemento della catena RF, domina sulle prestazioni in termini di linearità ed efficienza dell'intero trasmettitore. Inoltre, schemi di modulazione dall'ordine elevato impongono requisiti più stringenti in fatto di linearità e distorsione.

Questa tesi si concentra su soluzioni circuitali tese ad ottenere PA ad alta linearità, compatibili con applicazioni ad alta velocità di trasmissione dati nelle onde millimetriche. Sono proposti alcuni amplificatori interamente integrati in tecnologia Silicio-Germanio (SiGe) con potenze di uscita nell'intorno dei 20 dBm. A partire da un progetto in classe J di riferimento, la principale fonte di distorsione da ampiezza a fase (AM-PM) è individuata nella variazione dell'impedenza di ingresso dei transistor bipolari con la potenza del segnale di ingresso. Per mitigare il problema è proposta una prima soluzione che vede una rete di adattamento in ingresso basata su un filtro *ladder* e che mostra una riduzione della distorsione AM-PM di un fattore cinque rispetto ad una semplice rete risonante con poca riduzione di PAE. Inoltre è stata progettata e realizzata una seconda soluzione: un PA che combina uno stadio di ingresso a dispositivi CMOS dalla massima linearità con uno stadio a bipolari in SiGe. Il circuito ha mostrato un'AM-PM pari a 1.5° al punto di compressione di 1 dB con una massima PAE del 20 %. Queste soluzioni sembrano causare una riduzione dell'efficienza nelle misure ad onda continua. In realtà, rispetto ai progetti di riferimento, è richiesto meno *backoff* per ottenere la stessa EVM e quindi l'efficienza media può risultare maggiore. Altre tecniche come l'adattamento del punto di lavoro del PA all'inviluppo del segnale o l'amplificatore Doherty possono inoltre essere utilizzate per recuperare l'efficienza persa.

Contents

Acronyms

3G third generation cellular network technology. 1

4G fourth generation cellular network technology. 1, 5

5G fifth generation cellular network technology. i, 1–3, 5, 8–12, 31–34, 47, 63, 64, 87, 91, 99, 101

ACPR adjacent channel power ratio. 28, 33, 34

AESA active electronically-scanned phased-array. 47

AM-AM amplitude-to-amplitude. i, 5, 8, 22, 29, 33, 71, 99, 101

AM-PM amplitude-to-phase. i, 5, 8, 16, 17, 23, 27, 29, 31, 33, 51, 69–71, 73, 76–78, 80, 83, 84, 87, 89–91, 93, 96, 97, 99–101

BER bit error rate. 8, 9, 32

BJT bipolar junction transistor. i, 12, 54, 69, 70, 78, 79, 99, 100

CAD computer-aided design. 30

CB common-base. 87, 89, 93

CE common-emitter. 79, 87, 89, 93

CMOS complementary metal–oxide–semiconductor. i, 12, 43, 93, 100, 101

DAC digital-to-analog converter. 47, 48, 56

DUT device under test. 30

ESD electrostatic discharge. 49

EVM error vector magnitude. i, 5, 16, 30, 33, 34, 91, 101

FSK frequency shift keying. 8

HBT heterojunction bipolar transistor. 12

IC integrated circuit. 5, 12, 63, 91

IM intermodulation. 24, 25, 28

IMN input matching network. i, 70, 77–80, 84, 89, 100

IoT internet of things. 1, 2

IPn nth-order intercept point. 26

KVL Kirkhoff voltages law. 36

LNA low-noise amplifier. 4, 11, 33

LTE long term evolution. 1

LUT look-up table. 34

MIM metal-insulator-metal. 69, 83

MIMO multiple-input multiple-output. i, 3, 5

MMIC Monolithic Microwave Integrated Circuit. 9, 32, 80

mmWave millimeter-wave frequency. i, 2, 3, 5, 9, 12, 33, 87

OMN output matching network. 40, 42, 45, 70, 80, 87, 99, 100

P_{1dB} 1-dB compression point. i, 17, 22, 26, 29, 58, 71, 72, 76, 82–84, 90–93, 97, 100, 101

P_{sat} saturated output power. 56, 58, 60, 63, 67, 82–84, 100

PA power amplifier. i, 4, 5, 8–17, 19, 27, 28, 32–45, 47–51, 53, 56, 58, 60, 63, 64, 66, 67, 69–72, 74–76, 78–81, 84, 87–91, 93–95, 97, 99–101

PAE power-added efficiency. i, 5, 8, 9, 15, 16, 58, 60, 64, 67, 69, 70, 83, 84, 87, 89–91, 93, 95, 97, 99–101

PAPR peak-to-average power ratio. 9, 29, 63, 83, 101

PEP peak envelope power. 29

PGA programmable gain amplifier. 47–49, 56

PHD polyharmonic distortion. 30, 31

PSK phase shift keying. 8

PVT process, voltage and temperature. 34

Q quality factor. 70

QAM quadrature amplitude modulation. 8

QOS quality of service. 69

RF radio frequency. i, 4–6, 9, 11, 12, 15, 16, 20, 27–29, 34, 35, 40, 47, 48, 71, 78

RX receive. 11, 26, 33

SiGe silicon-germanium. i, 12, 43, 47, 56, 58, 63, 69, 76, 80, 84, 87, 93, 100

SNR signal-to-noise ratio. 26, 32–34

SOA safe operating area. 55

SPI serial peripheral interface. 47, 56

T/R transmit-receive. 47

TX transmit. i, 11, 26, 33

VGA variable gain amplifier. 4, 11

WLAN wireless local area network. 2

Chapter 1

Introduction

Digital circuits? I'd rather fight than switch.

Robert John (Bob) Widlar (1937 - 1991)

1.1 Motivation

During the first quarter of 2019, the total number of mobile subscriptions was around 4.9 billion and grew at 2 % year-on-year. The long term evolution (LTE) accounts for 47 % of the total subscriptions; GSM/EDGE-only subscriptions have declined by 80 million during 2019 [1]. During the second quarter of 2019, several markets switched on 5G following the introduction of new 5G-compatible smartphones. Network deployments are expected to ramp up during 2020, creating the foundation for massive adoption of 5G subscriptions. There is a strong commitment and an increasing focus from chipset and device manufacturers on this new standard: the first devices, launched in 2018, were pocket routers while the first smartphones were launched in the second half of 2019, in line with the first commercial 5G services launches worldwide.

Mobile wireless networks were originally built for voice and messaging with limited connectivity. With the introduction of the third generation cellular network technology (3G) mobile broadband became more widely available and fourth generation cellular network technology (4G) networks have further enhanced the mobile broadband capabilities. Now 5G will need to meet new and increased performance levels and cover diverse applications such as high-capacity, low-latency communications as well as low-power machine-type communications with modest data-rate requirements. Moreover, the growing demand for increasing data transfer capabilities and the advent of Industry 4.0 and the internet of things (IoT) will lead to an extensive growth of wireless

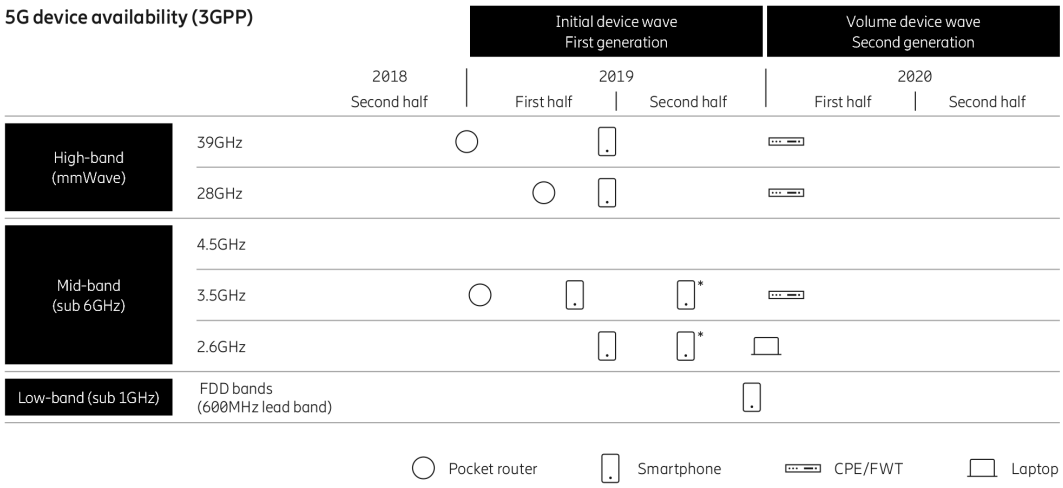


Figure 1.1: Current and projected 5G device availability [1]. First mmWave devices are expected to be available during 2019.

network users. The expected workloads are extremely different: on one hand, cellular networks will require very high data rates, low latency and high energy density, while, on the other hand, a massive number of IoT devices will need to access the channel in an asynchronous way. The challenge is exacerbated by the fact that the IoT devices can be highly heterogeneous in terms of computation and energy capabilities, as well as in their latency, reliability and data rate requirements.

As a result, 5G will bring much more than just performance enhancements with respect to the previous standards [1]. New complementary technologies include:

Beamforming For directional signal transmission and reception and to offset the path loss in the mmWave bands.

Front- and backhaul To enable faster data transfers and more dense coverage. They are connected together using high-speed optical fiber.

Hot spots Local internet access points offering 5G connectivity alongside wireless local area network (WLAN).

Small cells Portable miniature base stations that require minimal power to operate and can be placed every 250 meters or so throughout cities to provide more targeted and efficient use of the spectrum.

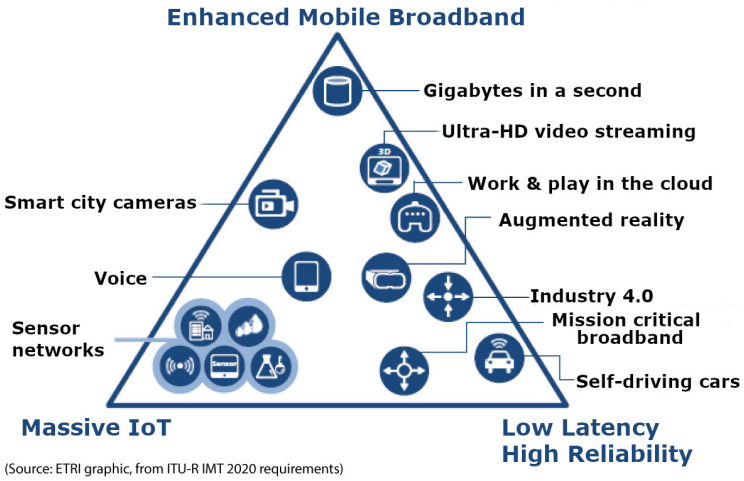


Figure 1.2: Range of applications covered by 5G.

In order to offer a set of integrated radio-access technologies jointly enabling the long-term networked society, today's high-power, few-antenna systems will soon be replaced with highly integrated active antenna systems. Those systems will have up to hundreds of individually driven low-power radios operating with wideband signals. This leads to several radio-access research challenges such as increasing the spectrum allocation flexibility, the development of array-antenna techniques and enabling efficient device-to-device communication.

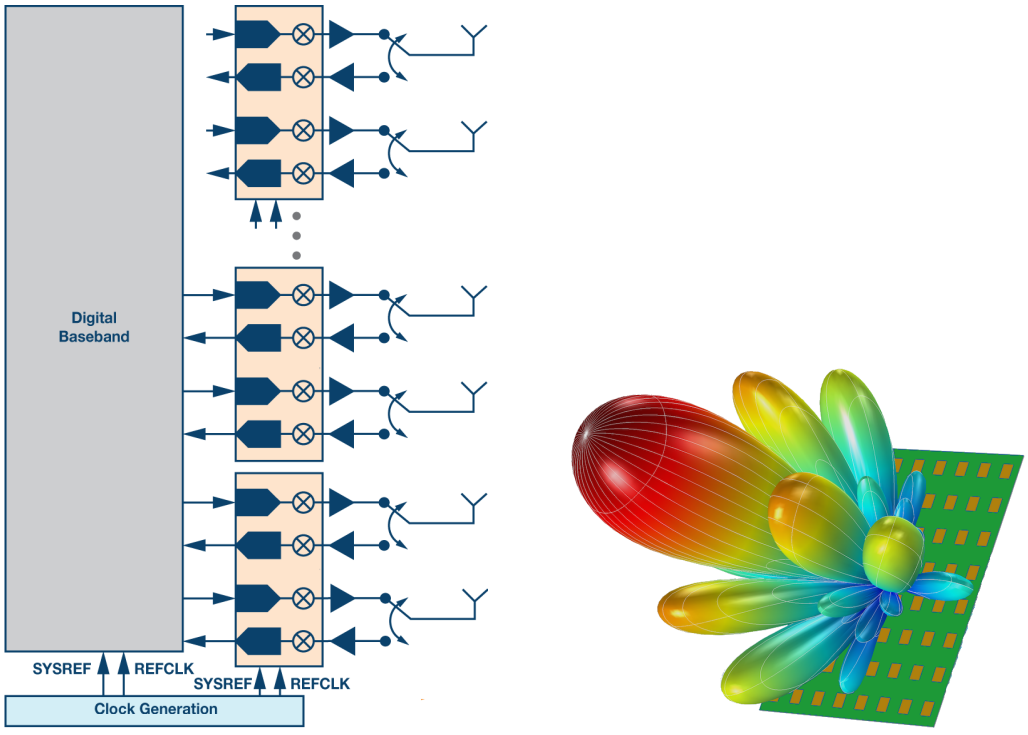
In December 2015, the World Radio-communication Conference promoted cellular applications in bands below 6 GHz and in ranges between 24 GHz to 84 GHz [2], where vast spectrum currently exists with light use. For bands below 6 GHz, the baseline requirements will be similar to the current cellular conditions. At mmWave, due to the higher path losses [3], to maintain useful link budgets, beamforming and massive MIMO [4] are required. These lossy mmWave channels can be made more reliable, and in some cases with smaller propagation losses, than today's cellular networks by using highly directional steerable antennas and beam combining techniques [3, 5, 6]. Such solutions imply new, previously overlooked, transmitter issues such as spatial selectivity, antenna crosstalk and interference levels for adjacent channels, but also provide many new radio-design opportunities.

1.2 Challenges

As already discussed, 5G in the mmWave employs array-antenna systems to focus the radiated power in the desired direction to reduce the path loss

and improve the link budget [3]. In a typical transmitter, the antennas are connected to radio frequency (RF) front-end units that support from 4 to 24 (depending on the target application) antennas each, and provide PA, low-noise amplifier (LNA), switch, phase shifter and variable gain amplifier (VGA) for each antenna element. A number of these RF front-end components will then connect with RF transceivers, responsible for the signal generation, modulation and demodulation. A block diagram for this architecture is shown in Figure 1.4(a) and the antenna radiation pattern obtained by a phased array is depicted in Figure 1.4(b).

Figure 1.3: 5G bandwidth allocations, as promoted by WRC15 [2].



(a) (b)

Figure 1.4: Conceptual block diagram of a typical phased array (a) and antenna radiation pattern (b) showing improved directivity.

Due to the increased system complexity and performance requirements, RF integrated circuit (IC) design for high speed cells offer new possibilities but also pose new design challenges. In such context, PAs are emerging as key elements of the technology mix, whose characteristics (particularly, efficiency and linearity) may become a limiting factor for the overall system performance. Compared to their 4G forerunners, system requirements for 5G in the mmWave pose significant new issues that need to be addressed and that together make meeting such requirements more daunting. The most important are:

Higher carrier frequencies which, as shown by the literature survey in Figure 1.5(a) and 1.5(b), reduce the maximum output power and power-added efficiency (PAE).

Wider signal bandwidths also reduce the maximum PAE because, due to the Bode-Fano limit [7, 8], it is harder to obtain good power matching over a wide frequency band.

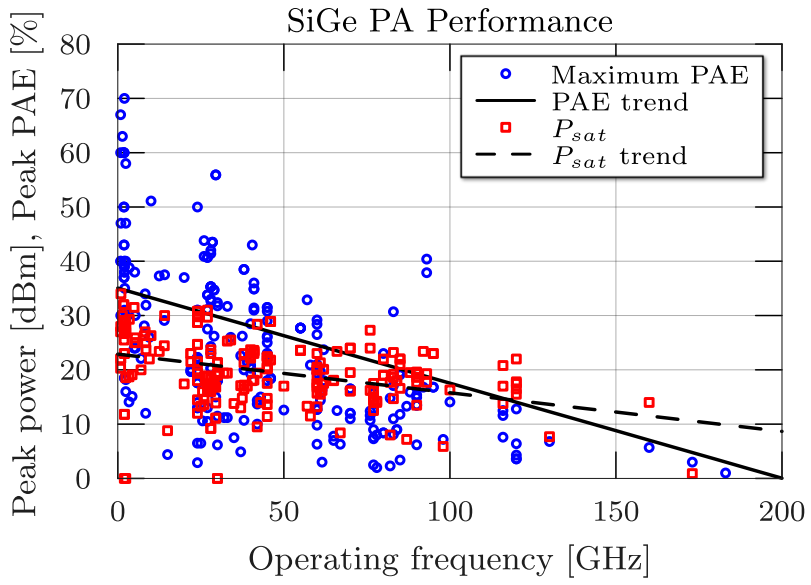
Modulations with Higher peak-to-average power ratios force the PA to operate with lower average power for the same amount of EVM thus lowering efficiency and device utilization.

Complex signal constellation that demand high linearity, both in terms of AM-PM and AM-AM, in order not to compromise signal integrity.

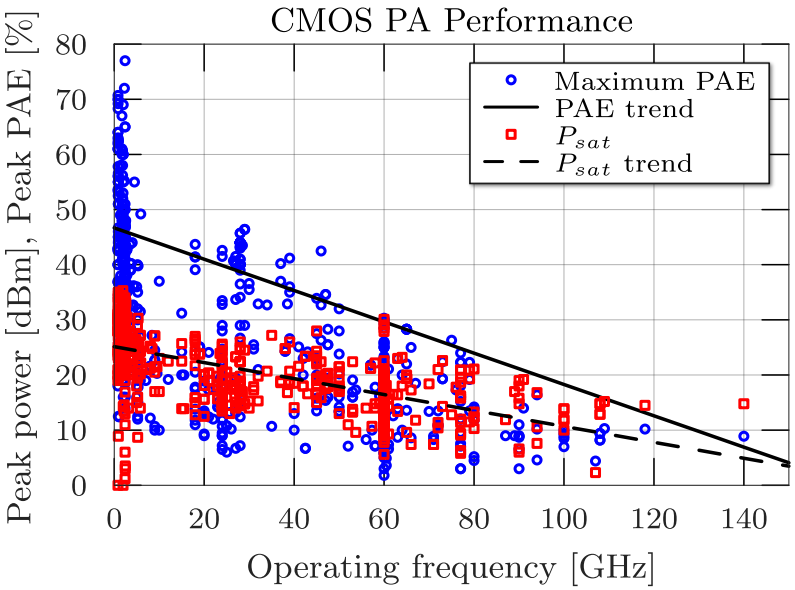
Moreover, when a PA is operating in a phased array, mutual coupling between antenna elements causes their active port impedance to change with the scan angle [9], invalidating the assumption of a constant $50\,\Omega$ PA load impedance in active antenna transmitters. This effect is even worse in massive MIMO, with individually controlled amplifiers and complicated variations of the load impedance. In the absence of isolators (which are costly and lossy components), the transmitter branches interact through the antenna array. Signals will thus travel in both directions at the antenna-PA interface as a consequence of antenna mismatch and mutual coupling [9]. The loading conditions of a PA will deviate from the design values. This may have a negative impact on its linearity, on its efficiency and on the power it can deliver to the antenna. Modeling such effects and making PAs less sensitive to such variations is thus of primary importance.

The PA is one of the most critical hardware components in mobile communications transceivers. The requirements combine specifications on output power, energy efficiency, and linearity, which are challenging to meet. This holds for the handset as well as for the base station side, with different implications. Because of its high signal power, the final-stage PA typically dominates the

nonlinear characteristics of the transmitter and is also the most power-hungry component of the RF chain [9, 10].



(a)



(b)

Figure 1.5: Relationship between saturated output power (P_{sat}) and PAE versus operating frequency for PAs fabricated in SiGe (a) and CMOS (b). Both metrics are inversely proportional to the frequency. As we move higher in the spectrum, the harder it becomes to obtain both high efficiency and high power PAs. Data points refer to publications reported in [11].

Figure 1.6 depicts the typical behaviour of output power, AM-PM distortion and PAE of a generic amplifier where we can distinguish two PA operating regions: a low-power and high linearity region where the efficiency is low, and a high-power low linearity region where the efficiency is at its peak. The output power and the efficiency of PAs are maximum when the devices are pushed to the limits of their voltage and current handling capability, which also implies higher distortion. In this region (red right part of Figure 1.6) if a constant amplitude modulation scheme, such as frequency shift keying (FSK) or phase shift keying (PSK), is used then, the PA offers its maximum efficiency with no penalty on the bit error rate (BER) whatsoever. Any amplitude or phase imbalance is constant and thus can be easily corrected at the transmitter or receiver side. However, if the amplitude of the signal changes with the symbol being transmitted, which is the case for the quadrature amplitude modulation (QAM) modulation used by the 5G, memory effects, AM-PM and AM-AM distortion come into play and degrade the BER. If, on the other hand, the PA is operated in the low distortion region (blue left section in Figure 1.6) then the effect of distortion is minimized at the expense of reduced PAE. Figures 1.7(a) and 1.7(b) show the effects of operating the PA in the linear (blue left) region or in the saturated (red right) region, respectively, on a 64-QAM modulated signal. In the case of Figure 1.7(a) the shape of the constellation is hardly affected when passing through the amplifier, whereas, in the case of Figure 1.7(b), where the PA is operating at its maximum output power the symbols are hardly recognized.

To sum up, the development of 5G transmitters, both in terms of base station and handset application, poses new design challenges and opportunities for Monolithic Microwave Integrated Circuits (MMICs) design. One of the key elements in the RF chain is the power amplifier which is the last element before the antenna. As a result, it is required to handle high-power signals and transmit them with the maximum possible fidelity in order to have low BER at the receiver. Moreover, at mmWave frequencies, phased arrays with hundreds of antenna elements are employed to counteract the effect of the increased path loss. In this scenario, having high efficiency is also of maximum importance and the PA is once again the most power-hungry block of the chain. As outlined before, there is however an inherent trade off between efficiency and linearity when PAs are required to transmit high peak-to-average power ratio (PAPR) modulations. Thus, having both power-efficient and linear transmission is challenging. Pushing the envelope further in the direction of both high PAE and low distortion is an ongoing research topic which, thanks to the development of 5G, is actively pursued.

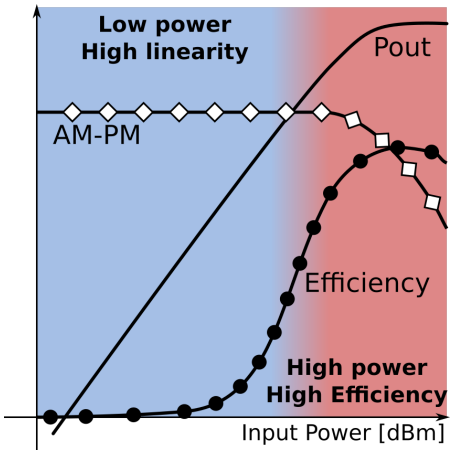
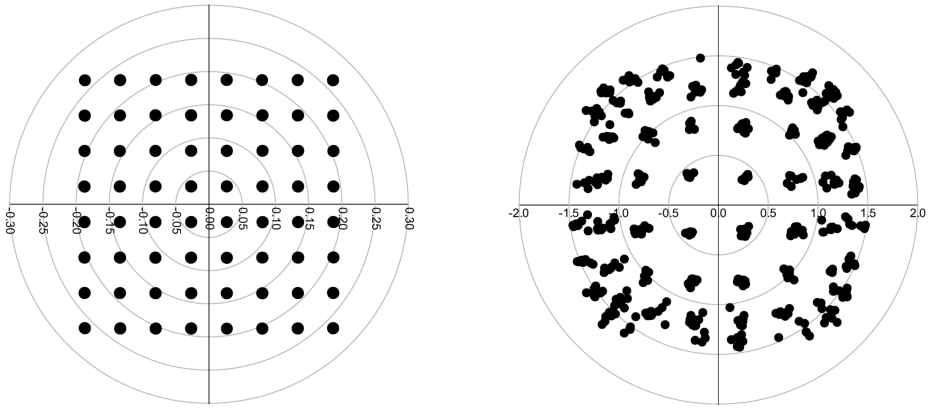


Figure 1.6: Typical PA output power, PAE and AM-PM distortion versus input power. Two regions are identified: the red right one where the power and efficiency is high but the linearity is at the lowest and the blue left one where linearity is maximized but PAE and output power are low.



(a) (b)

Figure 1.7: Constellation diagram obtained by operating the PA in Section 4.4 in the high linearity region (a) and in the maximum power region (b). While in (a) the symbols of the 64-QAM modulation are easily recognized, in (b) the diagram is heavily distorted.

1.3 Thesis Outline

This thesis is organized as follows. In Chapter 2 some fundamentals about the transmitter architecture and PA figures of merit will be given. The chapter will then discuss how system-level specifications translate into PA specifications and delve into some fundamental theory about amplifier distortion. Finally the previously developed theory will be used to analyze PA operating classes and class J amplifiers design. Chapter 3 shows the realization of class J PAs both for millimeter wave radar at 10 GHz and for 5G applications at 28 GHz. The results are compared against a class AB PA to assess the effectiveness of class J in improving the efficiency. Then, Chapter 4 shows some techniques which have been used to improve the linearity performance of the designs presented in Chapter 3. Conclusions are drawn in Chapter 5.

Chapter 2

Radio Transmitters and PAs

This chapter aims to provide some theoretical background upon which the works in the next chapters are built. First, an overview of a typical transmitter architecture for phased array applications will be given. Then, the main figures of merit used in the design of PAs are discussed and some theoretical analysis on the topic of distortion is provided. The effects of distortion are evaluated both on continuous-wave signals and with modulated signals. Then, the previously developed theory will be used to translate system level specifications for 5G transmitters into PA design specifications. And finally, the different linear amplifier classes are discussed with a focus on class J.

2.1 Transmitter Architecture Overview

Figure 2.1 shows the block diagram of a single transceiver element for phased array applications. Hundreds of such blocks comprise a typical 5G base station, whereas, due to space and power consumption constraints, a mobile phone may employ an order of magnitude less elements in its RF subsystem. Each block includes both the TX and the receive (RX) chain. They can be either active at the same time (in the case of a duplex transmitter where the TX and RX chains are operating on different carrier frequencies) or selectable by a switch controlled by the baseband.

The RF transmit chain receives a modulated signal from the baseband and is responsible for upconversion, amplitude and phase shifting for beam steering and power amplification. In its simplest form, the transmitter consists of a carrier signal generator, a modulator and a high-frequency PA that drives the antenna. The RX chain instead receives a weak signal from the antenna, amplifies it first via a LNA and then also via a VGA in order to drive the following stages with enough power. The signal is then phase-shifted to perform

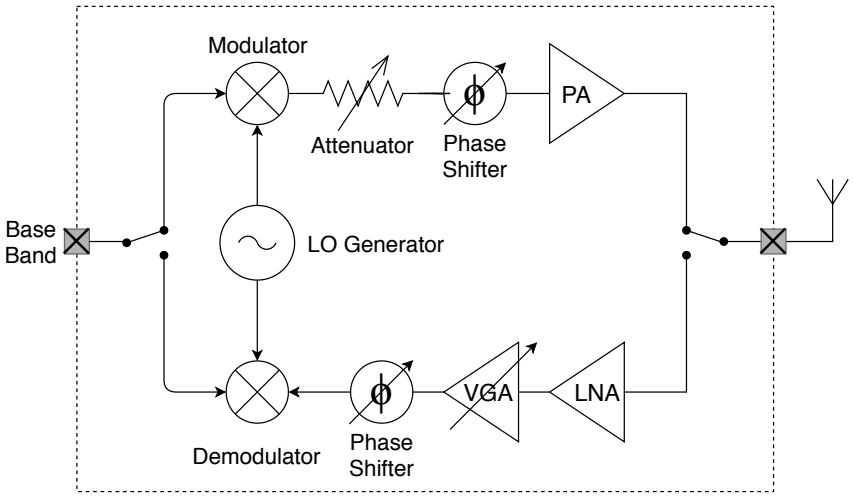


Figure 2.1: Phased array transceiver architecture.

beam steering and then downconverted and fed to the baseband [12].

To keep the overall cost down, the trend goes towards the integration of an increasing number of building blocks in the same package and also towards the implementation of more channels within a single integrated circuit [13, 14]. The BiCMOS SiGe technology enables the integration of heterojunction bipolar transistors (HBTs) alongside complementary metal–oxide–semiconductor (CMOS) devices, thus combining the best of both worlds. The high f_T, low noise and the large current driving capability of bipolar junction transistors (BJTs) can be exploited in the design of the RF chain while, CMOS devices, thanks to their low cost and high level of integration, make it possible to realize a complete transceiver module composed of analog, RF and digital building blocks within a single IC.

The design of integrated RF building blocks for 5G mmWave applications presents many challenges, and the PA is no exception. Depending on the type of modulation the PA operates in a linear or saturated regime. The regime in which the PA operates has important ramifications for the efficiency and power consumption of the entire transmitter, as well as for the feasibility of integrating the PA monolithically along with the other blocks of the transmitter [15].

2.2 Definition of Power Amplifier Parameters

Regardless of its physical realization, the task of a PA is to increase the power level of the signal at its input in a given frequency band, up to a predefined level at its output. Therefore the absolute output power level, as well as the

power gain, become the PA's primary performance metrics. The output power P_{out} is the power delivered to the external load (usually $50\,\Omega$) at the frequency of interest f:

$$P_{out} = P_{out}(f) = \frac{1}{2}\Re\{V_{out}(f) \cdot I^*_{out}(f)\} \tag{2.1}$$

while the input power P_{in} is the available input power at the same frequency:

$$P_{in} = P_{in,av}(f) = \frac{1}{2}\Re\{V_{in}(f) \cdot I^*_{in}(f)\} \ . \tag{2.2}$$

The power gain G_P is defined as the ratio between the output and input power, calculated at frequency f:

$$G_P(f) = \frac{P_{out}(f)}{P_{in}(f)} \ . \tag{2.3}$$

Due to the broad dynamic range of the signals involved in a PA, power quantities are usually expressed in decibel-milliwatts [dBm]. If the logarithmic scale is adopted, then the gain can be expressed in decibel [dB] and the ratio becomes a subtraction:

$$G_P^{(dB)} = P_{out}^{(dBm)} - P_{in}^{(dBm)} \ . \tag{2.4}$$

The power gain, due to the nonlinear PA behaviour which will be analyzed in the following section, depends on the input signal level. For very small drive levels, the amplifier behaves almost linearly and it is possible to define the linear gain G_L as:

$$G_L(f) = \lim_{P_{in}\to 0}[G_P(f)] \ . \tag{2.5}$$

On the other hand, when the input drive is sufficiently high, the gain starts to approach 0 decibel and the output power becomes virtually constant (in logarithmic scale). This power level is called saturated output power and is defined as:

$$P_{sat}(f) = \lim_{P_{in}\to\infty}[P_{out}(f)] \ . \tag{2.6}$$

There are actually four definitions for the power gain [16, 17]. If the input and output ports are all matched then all the definitions of power gain converge to the same expression. An important gain metric to be considered in PA design is the transducer power gain, defined as the ratio of the power delivered to the load to the power available from the source. For a two-port network, its definition is based on the circuit S-parameters

$$G_T = \frac{P_L}{P_{av,S}} = \frac{|S_{21}|^2(1-|\Gamma_S|^2)(1-|\Gamma_L|^2)}{|(1-S_{11}\Gamma_S)(1-S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_S\Gamma_L|^2} \tag{2.7}$$

where Γ_S and Γ_L are the reflection coefficients at the input and output port, respectively, which are defined as follows:

$$\Gamma_{S,L} = \frac{Z_{S,L} - Z_0}{Z_{S,L} + Z_0} \ . \tag{2.8}$$

Typical active devices are unilateral ($|S_{12}|^2 \ll 1$) so (2.7) can be recast into the unilateral power gain:

$$G_{TU} = \frac{|S_{21}|^2(1 - |\Gamma_S|^2)(1 - |\Gamma_L|^2)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L)|^2} \ . \tag{2.9}$$

Thus the maximum available gain is the product of the transistor transducer power gain $|S_{21}|^2$, diminished by the power reflected at the input and output ports and increased by the gain due to matching at the input port $|(1-S_{11}\Gamma_S)|^{-2}$ and matching at the output port $|(1 - S_{22}\Gamma_L)|^{-2}$. The unilateral gain is maximized when the network is conjugately matched at the input and output ports. As will be discussed in Section 2.5, in order to maximize the efficiency the PA output network is rarely designed for power matching.

2.2.1 Stability Analysis

Any amplifier with power gain can be made to oscillate by parasitic feedback effects that lead to poor isolation between the input and output ports. The stability analysis of power amplifiers is complex: it has to be performed on all internal two-ports having active devices and on the complete circuit and it is further complicated by nonlinear effects. It has been proposed in [18] to classify oscillations in microwave power amplifiers into five categories: even mode, odd mode, parametric, spurious parametric and low frequency. Only an introduction to the theme of stability will be given in this thesis.

Small-signal stability against oscillation can be examined by using two-port S-parameters [18]. The parameters S_{12} and S_{21}, depending on their values and on the source and load impedance, may form a feedback loop that can support oscillations. In an ideal amplifier, S_{12} would be zero and the amplifier would be unconditionally stable. Having defined Γ_S and Γ_L as in (2.8), the input reflection coefficient Γ_{in} and the output reflection coefficient Γ_{out} can be expressed as [17]:

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.10}$$

$$\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \ . \tag{2.11}$$

If the circuit is unconditionally stable, any source or load impedance may be connected to the input or output of the circuit without oscillations. This means that the following inequalities must be simultaneously satisfied:

$$\begin{array}{l} |S_{11}| < 1 \ , \quad |S_{22}| < 1 \\ |\Gamma_{in}| < 1 \ , \quad |\Gamma_{out}| < 1 \end{array} \tag{2.12}$$

Those conditions can be summarized by defining the *K stability factor* [17] as follows, where (2.12) lead to the requirement:

$$K = \frac{1 + |S_{11}S_{22} - S_{12}S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|} > 1 \ . \tag{2.13}$$

To graphically asses the stability of an RF circuit, if $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are set equal to unity, a boundary is established beyond which the device is unstable. In the Smith chart [19], each condition will give a solution of a circle. Those circles are called *source stability circle* and *load stability circle* depending whether they are generated by the condition $\Gamma_{in} = 1$ or $\Gamma_{out} = 1$, respectively. If the circuit is potentially unstable ($K < 1$), input or output impedances Z_S and Z_L that fall outside of the circle will result in no oscillation and the amplifier is said to be conditionally stable. If $K > 1$, the circles will fall outside of the Smith chart and the circuit is stable for any passive source and load terminations [17]. The two-port stability analysis just described is known as even mode and is applicable only to the sensitivity of the two ports to external impedances, not to internal oscillations.

2.2.2 Power Amplifier Efficiency

As will be discussed later in Section 2.5, RF power amplifiers can be designed to operate under a variety of PAE and linearity conditions. In practice, all amplifier classes will operate at a reduced efficiency, compared to the theoretical calculation, due to inherent parasitic losses and non ideal operating conditions [17].

From an energetic point of view, and regardless of the specific application, a PA may be ultimately regarded as a component converting DC power from its supplies (P_{DC}) into RF power (P_{out}). Assuming a single supply with voltage V_{DC}, the PA will sink from it a current $I_{supp}(t)$ which varies depending on the output signal. Assuming a periodic PA excitation, the average power absorbed from the supply is thus:

$$P_{DC} = V_{DC} \cdot \frac{1}{T} \int_0^T I_{supp}(t) dt \tag{2.14}$$

where $T = 1/f$ is the period of $I_{supp}(t)$. The efficiency is the measure of how effective the amplifier is in converting DC power into RF power and is defined as the ratio between output power and supplied DC power

$$\eta = \frac{P_{out}}{P_{DC}} \ . \tag{2.15}$$

To differentiate this metric from other efficiency definitions, the ratio is also specified as *drain efficiency* (η_d) or *collector efficiency* (η_c), depending on the type of devices employed in the PA.

A more meaningful efficiency parameter is the power-added efficiency (PAE) that also takes into account the power needed to drive the input of the PA (P_{in}). This power is supplied by the active circuitry preceding the amplifier so the PAE is a more realistic metric of the efficiency of the PA in a typical scenario. It takes into account only the power that is *added* by the PA, i.e., the net increase of the signal from input to output and it is defined as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} = \frac{P_{out} \cdot \left(1 - \frac{1}{G}\right)}{P_{DC}} = \eta \cdot \left(1 - \frac{1}{G}\right) \tag{2.16}$$

If non-constant envelope signals have to be handled by the PA, then an *average efficiency* can be defined as in(2.15), where the quantities in the expression are replaced by their average over an envelope period T_e and weighed by the envelope probability density function $PDF(t)$ [20]

$$\eta_{AVG} = \frac{P_{out,AVG}}{P_{DC,AVG}} = \frac{\frac{1}{T_e}\int_0^{T_e} P_{out}(t)PDF(t)dt}{\frac{1}{T_e}\int_0^{T_e} P_{DC}(t)PDF(t)dt} \ . \tag{2.17}$$

The efficiency is an important power amplifier parameter for several reasons. If the circuit is battery powered, the battery life will be degraded if the efficiency is low. Equally important, the power not converted into RF energy is dissipated as heat, which must be removed to preserve the reliability of the amplifier.

2.3 Distortion Analysis

Higher-order digital modulation schemes set more stringent constraints on PA linearity performance, especially concerning AM-PM distortion (which will be defined later in this chapter). Such schemes increase linearity requirements on the whole transmit chain and the PA is no exception. To put the problem into the right perspective, consider that a 5° AM-PM in a system employing a 64-QAM modulation scheme degrades EVM as much as a 1 dB gain compression [21]. Moreover, to maximize efficiency, the PA has to run as close to

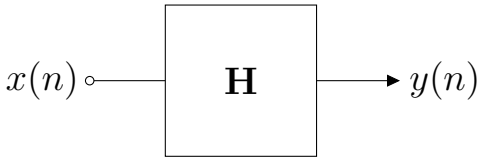


Figure 2.2: Model of a discrete-time system where $x(n)$ is the input signal, **H** is the transfer function and $y(n)$ the output signal.

saturation as possible. Having the P_{1dB} not very far from the saturated region and a low AM-PM distortion helps in further reducing the back-off amount. This in turn leads to an increased average power efficiency with modulated signals. It is therefore of primary importance to understand and model such effects.

2.3.1 Power Series and Volterra Series

The power series and the Volterra series are a model for the representation of non-linear systems in signal processing and system identification. The power series deals with non linear systems, and the Volterra series is also able to capture the memory effect of devices like capacitors and inductors in the circuit. They can be thought as a natural extension to the classical representation of linear systems without memory represented in Figure 2.2 and described by the equation:

$$y(n) = h \cdot x(n) \tag{2.18}$$

where the output y at instant n only depends on the input x at that instant only through the linear gain h. If the system is nonlinear and memoryless, the transfer function H can be expressed as a Taylor series and the model becomes:

$$y(n) = H_0 + H_1 \cdot x(n) + H_2 \cdot x^2(n) + \ldots = \sum_{i=0}^{n} H_i \cdot x^i(n) \ . \tag{2.19}$$

In the case of linear, discrete, causal and time-invariant system with memory, the output is obtained by summing all the effects of past inputs with proper weights:

$$y(n) = \sum_{i=0}^{n} h(\tau_i) \cdot x(n - \tau_i) \tag{2.20}$$

where $h(\tau)$ is the impulse response of the system. Equation (2.20) is also called *discrete-time convolution*. To model also the non linearities of a system then,

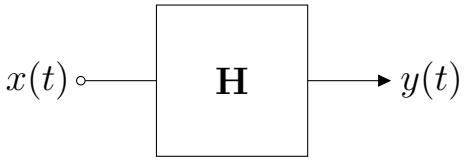


Figure 2.3: Model of a continuous-time system where $x(t)$ is the input signal, $\mathbf{H}$ is the transfer function and $y(t)$ the output signal.

the formula (2.20) is extended as follows to become the *Volterra series*:

$$y(n) = h_0 + \sum_{q=1}^{Q} \sum_{\tau_1=a}^{b} \cdots \sum_{\tau_q=a}^{b} h_q(\tau_1, \cdots, \tau_q) \prod_{j=1}^{q} x(n - \tau_j) \tag{2.21}$$

where the terms $h_q(\tau_1, \cdots, \tau_q)$ are called q-th order Volterra Kernels and represent the q-th order impulse response of the system.

As usual, in the continuous time domain (Figure 2.3) the convolution sum becomes a convolution integral and the system is modeled as follows:

$$y(t) = h_0 + \sum_{n=1}^{N} \int_a^b \cdots \int_a^b h_n(\tau_1, \cdots, \tau_n) \prod_{j=1}^{q} x(n - \tau_j) d\tau_j \ . \tag{2.22}$$

To build an analogy on the nonlinear memoryless system represented by (2.19) a nonlinear system with memory can be described with the equation:

$$y(t) = \mathbf{H_0} + \mathbf{H_1}[x(t)] + \mathbf{H_2}[x(t)] + \cdots + \mathbf{H_n}[x(t)] \tag{2.23}$$

in which $\mathbf{H_n}[x(t)] = \int_a^b \cdots \int_a^b h_n(\tau_1, \cdots, \tau_n) x(t - \tau_1) \cdots x(t - \tau_n) d\tau_1 \cdots d\tau_n$ is called the n-th order Volterra operator.

Generally, estimating the Volterra kernel coefficients is complicated since the basis functionals of the Volterra series are correlated, so to derive the n-th order term it is required to know all the $n-1$ kernels that precede it. Moreover, in the time domain, it is difficult to determine the order of the system which instead, in the frequency domain, can be obtained by observing the number of harmonics in the output signal when one or more sinusoidal signals are applied as an input. Therefore, especially in the case of electronic circuits, it is sometimes more convenient to determine the Volterra Kernel in the frequency or Laplace domain.

Let us suppose that a circuit is excited by the signal $s(t)$ which contains, in general, a number of individual sinusoidal excitation components having noncommensurate frequencies [22], described by the formula:

$$s(t) = \frac{1}{2} \sum_{q=-Q}^{Q} V_q \, e^{j\omega_q t} \tag{2.24}$$

where $V_{-q} = V_q^*$ and $\omega_{-q} = -\omega_q$. The term V_q implies that the signal is a voltage, as it is usually the case in microwave circuits, but it could be of any kind, such as a current or power. Moreover, we assume that the excitations do not include DC components so, from now on, we can consider $q \neq 0$.

The output of the linear circuit with input $s(t)$ is $v(t)$ in Equation (2.25). The signals $s(t)$ and $v(t)$ correspond, in Figure 2.3, to $x(t)$ and $y(t)$ respectively.

$$v(t) = \frac{1}{2} \sum_{q=-Q}^{Q} V_q \cdot H(\omega_q)\, e^{j\omega_q t} \tag{2.25}$$

If a nonlinear circuit is considered, we can substitute $s(t)$ into (2.19) for $x(t)$. The response of the system is denoted as $w(t)$ to differentiate it from the linear response $v(t)$ and follows the formula:

$$\begin{aligned} w(t) &= \sum_{n=1}^{N} K_n [v(t)]^n \\ &= \sum_{n=1}^{N} \frac{K_n}{2^n} \sum_{q1=-Q}^{Q} \cdots \sum_{qn=-Q}^{Q} V_{q1} \cdots V_{qn} \\ &\qquad H(\omega_{q1}) \cdots H(\omega_{qn}) \cdot e^{j(\omega_{q1}+\cdots+\omega_{qn})t} \end{aligned} \tag{2.26}$$

which is called the *power series*.

If we apply the signal (2.24) as an input to the system in Figure 2.3 (which we now suppose is a non-linear system with memory) the response to such excitation can be described by a Volterra series in the frequency domain:

$$w(t) = \sum_{n=1}^{N} \frac{1}{2^n} \sum_{q1=-Q}^{Q} \cdots \sum_{qn=-Q}^{Q} V_{q1} \cdots V_{qn} H_n(\omega_{q1}, \ldots, \omega_{qn}) \cdot e^{j(\omega_{q1}+\cdots+\omega_{qn})t}. \tag{2.27}$$

The only formal difference between 2.27 and 2.26 is that 2.27 contains a single function $H_n(\omega_{q1}, \ldots, \omega_{qn})$ instead of the product of linear transfer functions $K_n H(\omega_{q1}) \cdots H(\omega_{qn})$. By comparing the two, we can see that the power series is a special case of the Volterra series in which the nonlinear transfer function $H_n(\omega_{q1}, \ldots, \omega_{qn}) = K_n H(\omega_{q1}) \cdots H(\omega_{qn})$. Finally, Equations 2.26 and 2.27 show that a large number of new frequencies can be generated by the nonlinearities. The effect of such frequencies on the behaviour of PAs will be discussed later on in this section.

One important drawback to be considered when the Volterra-series analysis is performed is that, like the power-series analysis, the assumption of a weakly nonlinear circuit must hold in order for the results to be accurate. A nonlinear

circuit may indeed generate DC components in its output in response to a sinusoidal excitation. When the excitation is small and the non linearities are weak, the DC components generated by the non linearities are very small, and invariably negligible. The practical effect of the generation of DC components is to offset the bias currents and voltages slightly from their quiescent values. In cases where significant bias offset occurs, for example, in a class-B amplifier, Volterra and power-series analyses may require too many terms to be accurate and become unpractical [22, 23].

2.3.2 Effects of Circuit Nonlinearities

While analog and RF circuits can be approximated by a linear model for small-signal operation, nonlinearities often lead to interesting and important phenomena that are not predicted by small-signal models. The following analysis will consider systems whose input/output characteristic is described by (2.27).

Single-tone Excitation

Let's consider a real-valued nonlinear system with non linearity degree N. To such system it is applied a signal described by (2.24) with order $Q = 1$:

$$s(t) = \frac{V_q}{2}\left(e^{j\omega t} + e^{-j\omega t}\right) = V_q\,\cos(\omega t)\ . \tag{2.28}$$

If we solve equation (2.27) for the first degree term ($n = 1$) the output of the system is given by:

$$w_1(t) = \frac{1}{2}V_q\left[H_1(\omega)\,e^{j\omega t} + H_1(-\omega)\,e^{-j\omega t}\right] = |H_1(\omega)|V_q\,cos(\omega t + \phi_{1,1}) \tag{2.29}$$

where we used the real-valued system hypothesis such that H_n is an even-symmetric complex function ($H_1(-\omega) = H_1^*(\omega)$) to rewrite the formula. Moreover, we named $\phi_{1,1}$ the phase angle associated with $H_1(\omega)$. Equation (2.29) represents the usual first-harmonic response of linear systems.

Then we can consider Equation (2.27) for the second degree term, corresponding to $n = 2$. The output of the system is:

$$w_2(t) = \frac{1}{4}V_q^2\,H_2(\omega_{q1}, \omega_{q2})\,e^{j(\omega_{q1}+\omega_{q2})t} \tag{2.30}$$

where $\omega_{q1} = \pm\omega$ and $\omega_{q2} = \pm\omega$ so we have 4 choices for the frequencies, two of which result in a DC term (frequency = 0) and two at twice the input frequency

(assuming again a real-valued system where $H_2(\pm\omega, \pm\omega) = H_2^*(\mp\omega, \mp\omega)$). The output for $n = 2$ can be recast as follows:

$$w_2(t) = \frac{1}{2} V_q^2 \left[|H_2(\omega, -\omega)| \cos(\phi_{2,0}) + |H_2(\omega, \omega)| \cos(2\omega t + \phi_{2,2}) \right] \tag{2.31}$$

where we can see that the second-order non linearities can alter the DC operating point of the circuit and produce a second harmonic term.

Finally we can consider the third-degree term of the Volterra series for which the system output is:

$$w_3(t) = \frac{1}{8} V_q^3 \, H_3(\omega_{q1}, \omega_{q2}, \omega_{q3}) \, e^{j(\omega_{q1}+\omega_{q2}+\omega_{q3})t} \tag{2.32}$$

where possible values for ω_{q1}, ω_{q2} and ω_{q3} are summarized in Table 2.1. Writing each term of the series explicitly gets complicated very quickly, as for each value of n and Q there are $(2Q)^n$ frequency terms to be computed. Like the results for the second-order expansion, in this case we also get two terms: one at the input frequency and one at three times the input frequency:

$$\begin{aligned} w_3(t) = \frac{1}{4} V_q^3 \left[3 \, |H_3(\omega, \omega, -\omega)| \cos(\omega t + \phi_{3,1}) + \right. \\ \left. |H_3(\omega, \omega, \omega)| \cos(3\omega t + \phi_{3,3}) \right] . \end{aligned} \tag{2.33}$$

The total response of the system is the sum of all the $n = 1, \cdots, N$ terms: $w(t) = w_1(t) + w_2(t) + w_3(t) + \cdots + w_N(t)$. From this equation we can make the following observations. First, even-order non linearities introduce DC offsets and also affect the other even-order non linearities of lower degree. Second,

ω_{q1}	ω_{q2}	ω_{q3}	Output Frequency
$+\omega$	$+\omega$	$+\omega$	$+3\,\omega$
$+\omega$	$+\omega$	$-\omega$	$+\omega$
$+\omega$	$-\omega$	$+\omega$	$+\omega$
$+\omega$	$-\omega$	$-\omega$	$-\omega$
$-\omega$	$+\omega$	$+\omega$	$+\omega$
$-\omega$	$+\omega$	$-\omega$	$-\omega$
$-\omega$	$-\omega$	$+\omega$	$-\omega$
$-\omega$	$-\omega$	$-\omega$	$-3\,\omega$

Table 2.1: Third-degree frequency terms of the single-tone Volterra series.

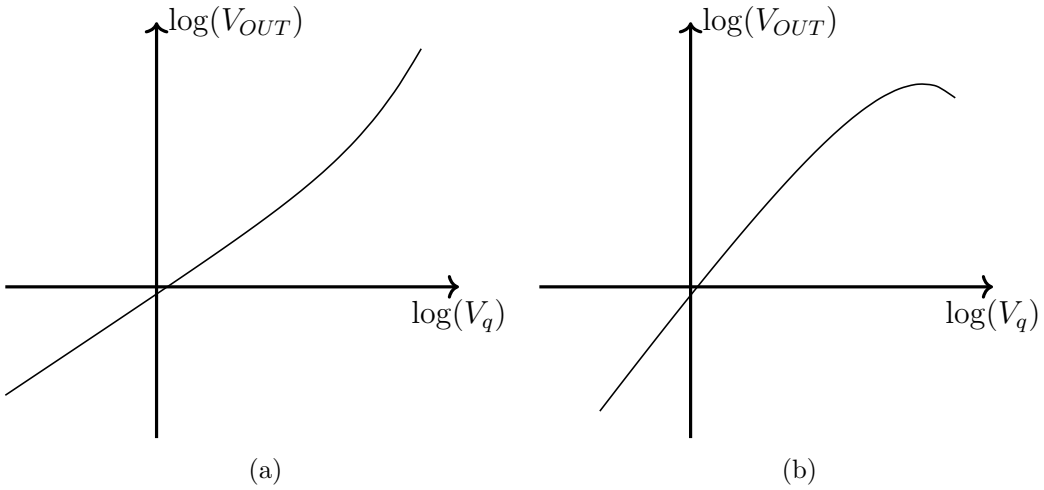


Figure 2.4: Examples of (a) expansive and (b) compressive characteristics.

odd-order non linearities affect the fundamental component and the other odd-order non linearities of lower degree. Third, the amplitude of each term of degree n is proportional to V_q^n.

One of the first and most notable effects of non linearities is *gain compression*. Equation (2.29) and (2.32) indicate that the gain experienced by $V_q \cos(\omega t)$ is equal to $|H_1(\omega)| \cos(\phi_{1,1}) + \frac{3V_q^2}{4} \cdot |H_3(\omega, \omega, -\omega)| \cos(\phi_{3,1})$ and hence varies appreciably as V_q becomes larger, causing a variation of the slope of the input/output characteristic with the input level. This phenomenon is called amplitude-to-amplitude (AM-AM) distortion. If $\cos(\phi_{1,1}) \cos(\phi_{3,1}) > 0$ then the slope increases with V_q yielding an *expansive* behaviour (Figure 2.4(a)). This happens, for example, in an ideal bipolar transistor operating in the forward active region producing a current proportional to e^{V_{BE}/V_T}. On the other hand, if $\cos(\phi_{1,1}) \cos(\phi_{3,1}) < 0$ then the slope is decreased as V_q increases leading to a *compressive* characteristic (Figure 2.4(b)).

With $\cos(\phi_{1,1}) \cos(\phi_{3,1}) < 0$ the gain of the circuit falls as V_q rises. This effect is quantified by the 1-dB compression point (P_{1dB}), defined as the input (output) signal level that causes the gain to drop by 1 dB. Moreover, from Equation (2.32) is obtained an additional term which is altering the behaviour of the circuit at the first harmonic: $-\frac{3V_q^3}{4}|H_3(\omega, \omega, -\omega)| \sin(\omega t) \sin(\phi_{3,1})$. This term is a phase-shifted, amplitude dependent version of the cosine term and is summed to it. The summation is shown, in phasor representation, in Figure 2.5. This means that the phase of the output signal with respect to the input is dependent on the signal amplitude. This leads to undesirable effects since

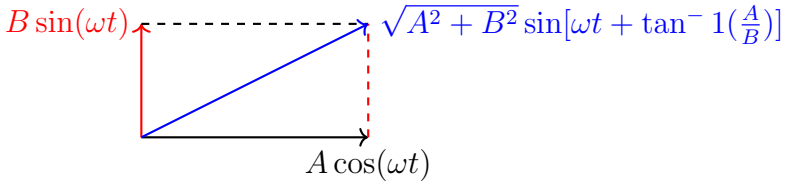


Figure 2.5: Phasor representation of the AM-PM distortion summation. The first-harmonic term is the black vector and the effect of the third harmonic is represented in red. The blue vector is the resulting output signal.

amplitude modulation may be converted into phase modulation, altering the information carried by the modulated signal. This phenomenon is called amplitude-to-phase (AM-PM) distortion.

Two-tone Excitation

If two sinusoidal signals at frequencies ω_1 and ω_2 are applied to a nonlinear system, the output exhibits, alongside the harmonics of these frequencies, also new frequencies that arise from products of the two components as their sum is raised to a power greater than unity. Furthermore, the amplitude of each of those new frequency components is proportional to the product of the amplitudes of all the contributing excitations. Some of the lowest-order terms ($n \leq 3$) are usually of most concern to system designers, as they allow to reveal nonlinear effects that may not manifest themselves in a single-tone test.

It is important in the following analysis to distinguish between the concepts of degree and order. The degree of the non linearity refers simply to the power of $v(t)$ in the nonlinear transfer characteristic (2.26). In (2.27), an nth-order mixing frequency is defined as one that arises from the sum of n excitation frequencies. In general it is not possible to determine the order of a mixing product from its frequency; for example, the frequency $2\omega_1 - \omega_2$ appears at first to be of third order, that is, $2\omega_1 - \omega_2 = \omega_1 + \omega_1 - \omega_2$, but in reality it could be the fifth-order mixing product, $\omega_1 + \omega_1 + \omega_1 - \omega_1 - \omega_2$ [22]. In the following discussion, our circuit contains only a single, ideal, transfer non linearity and no feedback, so an nth-degree non linearity generates mixing products up to only nth order.

We will now consider a non linear system, modeled by Equation (2.27) to which it is applied a signal described by (2.24) with $Q = 2$:

$$\begin{aligned} s(t) &= \frac{V_1}{2}\left(e^{j\omega_1 t} + e^{-j\omega_1 t}\right) + \frac{V_2}{2}\left(e^{j\omega_2 t} + e^{-j\omega_2 t}\right) \\ &= V_1\cos(\omega_1 t) + V_2\cos(\omega_2 t)\ . \end{aligned} \tag{2.34}$$

The system's first degree output component is given by the formula:

$$w_1(t) = \frac{1}{2}\left[V_1 H_1(\omega_{q1}) e^{j\omega_{q1}t} + V_2 H_1(\omega_{q2}) e^{j\omega_{q2}t}\right] \tag{2.35}$$

where, for compactness of notation, $\omega_{q1} = \pm\omega_1$ and $\omega_{q2} = \pm\omega_2$. Thus we get two sinusoidal components at the input frequencies multiplied and phase shifted according to the circuit linear response. If we now consider the second degree component of the circuit output:

$$w_2(t) = \frac{1}{4}\sum_{q1=-2}^{2}\sum_{q2=-2}^{2} V_{q1} V_{q2} H_2(\omega_{q1}, \omega_{q2}) e^{j(\omega_{q1}+\omega_{q2})t} \ , \tag{2.36}$$

the summation generates $(2Q)^n = 16$ terms, since $Q = 2$. Of those 16 terms half of them appear in complex-conjugate pairs (which is expected since they represent time waveforms in $\mathbb{R}$) and some of them are repeated. From (2.36) we get a DC term, two terms at twice the input frequencies and two intermodulation (IM) components at $\omega_1 + \omega_2$ and $\omega_1 - \omega_2$. The output voltage component generated by the third-degree term can be found in a similar manner. From (2.27), with $n = 3$, we have:

$$w_3(t) = \frac{1}{8}\sum_{q1=-2}^{2}\sum_{q2=-2}^{2}\sum_{q3=-2}^{2} V_{q1} V_{q2} V_{q3} H_3(\omega_{q1}, \omega_{q2}, \omega_{q3}) e^{j(\omega_{q1}+\omega_{q2}+\omega_{q3})t} \ . \tag{2.37}$$

This summation gives 64 terms, half of which complex-conjugate. Some, but not all of them, are summarized in Table 2.3.2. For a more detailed enumeration of the distortion terms and their coefficients please refer to Chapter 9 in [24]. The first two of these mixing frequencies are important because they often appear at frequencies close to ω_1 and ω_2 and thus are difficult to filter. In the summation above there are three identical terms at $2\omega_2 - \omega_1$ and three at $2\omega_1 - \omega_2$, so the coefficient 3 is used in the expression for such components. For example, expressing the term at $2\omega_2 - \omega_1$ in cosine form we get: $w_3'(t) = \frac{3}{4} V_1 V_2^2 |H_3(-\omega_1, \omega_2, \omega_2)| \cos[(2\omega_2 - \omega_1)t + \phi_3]$. Where ϕ_3 represents the combined phases of the complex coefficients in (2.37). Since the purpose of intermodulation analysis is usually to determine the output power at the mixing frequency, the phase component is rarely of interest and for the sake of clarity and compactness of notation will be neglected in the following discussion.

A two-tone test is a common method for determining the intermodulation properties of a nonlinear or quasilinear circuit. In such test, two excitations of equal amplitude and separated only slightly in frequency are applied to the circuit, and the powers of the resulting IM components are measured. Figure 2.6

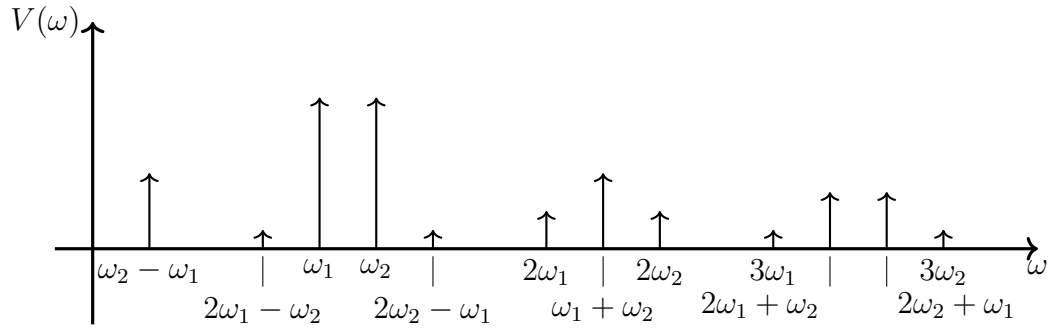


Figure 2.6: Spectrum of intermodulation frequencies resulting from two-tone excitation at frequency ω_1 and ω_2.

shows some of the lowest-order terms that are usually of most concern to system designers [12, 22].

Expressed in dBm, at low levels the second- and third-order intermodulation powers vary respectively 2 dB and 3 dB for each dB with the input power level. The linear output power varies instead at the expected 1 dB per dB rate. Further analysis [22] shows that nth-degree intermodulation products always vary by n dB with each dB of the input power level. As shown in Figure 2.7, at some point the linear output power and the intermodulation characteristics saturate, however below this saturation level the curves are straight lines. This straight-line behaviour can be used to predict the IM levels at any input power level. Since the angular coefficients of the straight line interpolating the low-level intermodulation curves are known, it is necessary to know only the output level at one point in order to define the entire curve. A convenient point is the extrapolated point at which the nth-order intermodulation and linear

ω_{q1}	ω_{q2}	ω_{q3}	Output Frequency
$+\omega_2$	$+\omega_2$	$-\omega_1$	$2\,\omega_2 - \omega_1$
$+\omega_1$	$+\omega_1$	$-\omega_2$	$2\,\omega_1 - \omega_2$
$+\omega_1$	$+\omega_1$	$-\omega_1$	ω_1
$+\omega_2$	$+\omega_2$	$-\omega_2$	ω_2
$+\omega_1$	$+\omega_1$	$+\omega_1$	$3\,\omega_1$
$+\omega_2$	$+\omega_2$	$+\omega_2$	$3\,\omega_2$

Table 2.2: Third-degree frequency terms of the two-tone Volterra series.

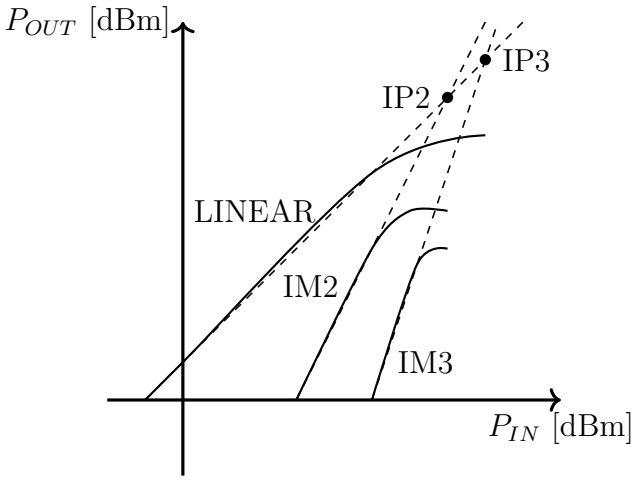


Figure 2.7: Input/output power curves for linear and intermodulation components higliting the second- and third-order intercept points.

output power are equal. This point is different for each order and is called the nth-order intercept point (IPn). This point is used to find not only the intermodulation output power, but the ratio of linear to intermodulation power level, often a more important quantity.

An adverse effect arising in the presence of two (or more) tones occurs if a large interferer accompanies the received signal. The effect is a reduction in the gain at the desired signal due to the large excursion of the signal produced by the interferer. This phenomenon, more relevant in the RX chain than in the TX chain, is called *desensitization* and lowers the signal-to-noise ratio (SNR) at the receiver. Assuming only real coefficients for the Volterra series in (2.35) and (2.37), the circuit response at the fundamental frequency ω_1 can be recast as follows:

$$w_f(t) = \left(\alpha_1 + \frac{3}{4}\alpha_3 V_{q1}^2 + \frac{3}{2}\alpha_3 V_{q2}^2\right) V_{q1}\cos(\omega_1 t)\ . \tag{2.38}$$

The first term, α_1, is the usual small-signal gain of the circuit. The second term, $\frac{3}{4}\alpha_3 V_{q1}^2$, is again responsible for the $\mathrm{P_{1dB}}$, while the last term (assuming $\alpha_1\alpha_3 < 0$ which is often the case) is responsible for the desensitization. In fact, for sufficiently large values of V_{q2} (the interferer amplitude) the gain drops to zero and no signal is output at the frequency of interest [12].

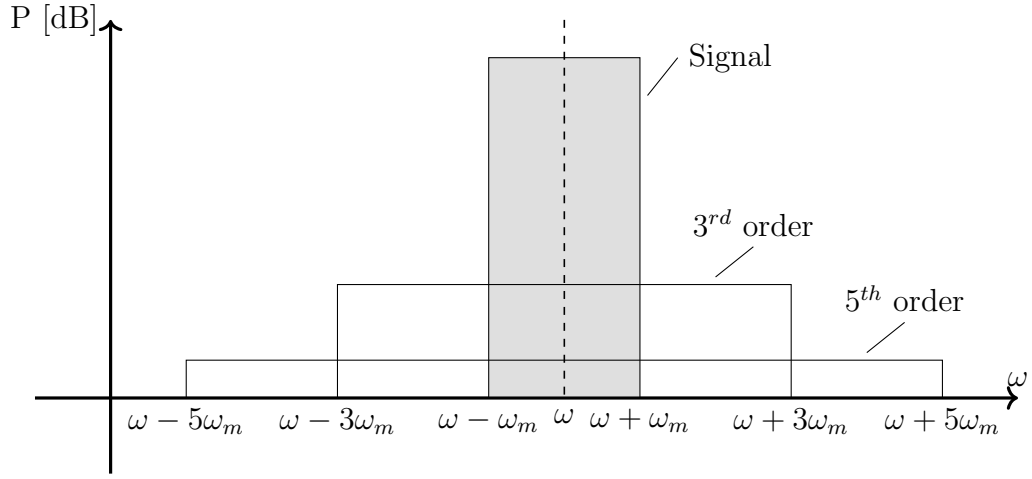


Figure 2.8: Intermodulation spectrum for a typical band-limited digitally modulated signal.

Modulated Signals Analysis

When dealing with PAs operating into regions of strong nonlinearity, the validity of the power series or Volterra series approach becomes questionable, especially if the goal is to have a useful tool to be used in the early stages of design. The issue is how many polynomial terms are required in a specific case to model the PA characteristic to the required degree of precision. The model has to be able to handle substantial amounts of gain compression, and the corresponding AM-PM distortion. Handling a large number of coefficients in a Volterra series is not an issue for modern computers. However, when modulated signals are fed into the model, many RF cycles have to be simulated in order to obtain an output suitable for spectral and modulation distortion prediction. This is still a time consuming task, even with modern hardware. Traditional algorithms are extremely inefficient because they are forced to follow the fast (orders of magnitude higher in frequency) varying carrier for a length of time sufficient to study the behaviour of the slow information signal [25]. This section tries to explain briefly the PA behaviour with modulated signals and discuss the methods of *envelope simulation*.

The methods of envelope simulation are used, as a means of predicting the spectral and modulation distortion under specific signal conditions, having derived a suitable model for the PA characteristic. As explained in the previous section, if two separate carriers with fixed spacing are applied to the PA, many new frequencies will be generated as a effect of distortion. Usually, in communications problems, only the first-zone spectral components of the

output, those that lie in or surround the input spectrum at the carrier frequency, are considered. Higher harmonics of the output spectrum are effectively filtered out and may be neglected. The products of most interest, in terms of their possible detrimental effects, are the third- and fifth-order IM products. The third order products appear at frequencies $2\omega_2 - \omega_1$ and $2\omega_1 - \omega_2$, while the fifth order products appear at $3\omega_2 - 2\omega_1$ and $3\omega_1 - 2\omega_2$. Please note that the fifth degree terms also add a contribution at the third order IM products. These higher degree contributions can be ignored when operating well below the compression level, but can become dominant in the compression and saturation regimes.

Let us now suppose that a signal with bandwidth $B = 2\omega_m$ and carrier frequency ω is applied to a nonlinear PA. The resulting output spectrum is depicted in Figure 2.8. In the two-tone analysis the intermodulation sidebands appear either side of each carrier at a frequency spacing equal to that of the two carriers (Figure 2.6). With modulated signals, the intermodulation bands stretch out to three (in the case of third order distortion) or five times (in the case of fifth order distortion) the original signal bandwidth. So the spectrum resulting from nonlinear amplification has a stepped appearance, with each step corresponding to a higher order of distortion. These steps are known as *spectral regrowth* sidebands [24] and their effect is quantified by the adjacent channel power ratio (ACPR) metric: the ratio between the total power adjacent channel (intermodulation signal) to the main channel's power (useful signal).

Starting once again with the to-carrier signal (2.34), this can be rearranged [24] as:

$$s(t) = 2V_q \cdot \cos(\omega_m t)\cos(\omega t) \tag{2.39}$$

with $\omega = (\omega_1 + \omega_2)/2$ and $\omega_m = (\omega_1 - \omega_2)/2$. This is now recognizable as a double sideband, suppressed carrier amplitude modulated signal with carrier frequency ω and a sinusoidal baseband modulation of frequency ω_M. This confirms the usefulness of IM analysis in giving insights about PA behaviour with modulated signals. More generally, a modulated signal is defined as

$$s_m(t) = V_m \cdot f(\omega_m t)\cos(\omega t) \tag{2.40}$$

and the modulating function $f(\omega_m t)$ is a scalar function of periodicity ω_m. A fundamental assumption of envelope analysis is that the modulation frequency is sufficiently slow compared to the RF signal carrier such that the conditions at any instant can be considered quasi-static and can be determined from a static, continuous-wave measurement at the same input power. Moreover the amplifier has to have sufficient bandwidth that the performance characteristics do not change over the bandwidth of the modulated signal and that the nonlinear action is independent of the frequency of the modulating signal [26].

The RF signal described by Equation (2.40) sweeps between an amplitude of zero and V_{pk}, dependent on $f(\omega_m t)$. Assuming, for convenience a $1\,\Omega$ resistive load we can define the peak envelope power (PEP) as the average power supplied to the load by a transmitter during one RF cycle at the crest of the modulation envelope:

$$P_{pk} = \left(\frac{V_{pk}}{\sqrt{2}}\right)^2 \ . \tag{2.41}$$

The overall mean power is given by integration of the square of the RMS RF amplitude over a complete modulation cycle:

$$P_m = \frac{\omega_m}{2\pi} \int_0^{\frac{2\pi}{\omega_m}} \frac{\left[V_m \cdot f(\omega_m t)\right]^2}{2} dt \ . \tag{2.42}$$

A very important parameter in envelope analysis is the ratio of P_{pk} over P_m, this ratio is called peak-to-average power ratio (PAPR). This is an useful metric, in fact if the mean power level of the variable envelope signal is set to be equal to the conventional, single-carrier $\mathrm{P_{1dB}}$ power, the peaks of the envelope will incur much greater than 1 dB of compression and will saturate the amplifier for a significant portion of the modulation cycle. Compared to the single carrier scenario, the modulated signals require an higher amount of backoff, proportional to the PAPR, in order to reach the same compression and IM3 level for the same amount of undistorted mean power level. The key issue is that waveforms with high PAPR have more power locked up in the high peaks, so if the peaks are clipped the effect is substantial [24].

So far AM-PM distortion has been neglected. It has been shown by Cripps [24] that the AM-AM and AM-PM components combine to produce sidebands which have a higher amplitude than the single contribution of either of these individual parts. It is worthy of note that if amplitude distortion effects are ignored completely, even one degree of AM-PM distortion can cause IM3 at a level of $-53\,\mathrm{dBc}$, and this will rise according to a law of 6 dB per doubling of the phase distortion [24].

When making the step from analog to digital modulation, it is usually necessary to make a conceptual step from mathematical functionality and analytical certainty to random sequences and statistical probabilities to estimate the distortion level in RF power amplifiers. The sequence of symbols and the path from one symbol to the following influences the amount of distortion produced. Signals resulting from both analog and digital modulation schemes can be represented as so called complex envelopes. A complex envelope is a complex time function where the real part represents the in-phase component and the imaginary component represents the quadrature component of a modulated carrier. The in-phase component is usually called I, and the quadrature

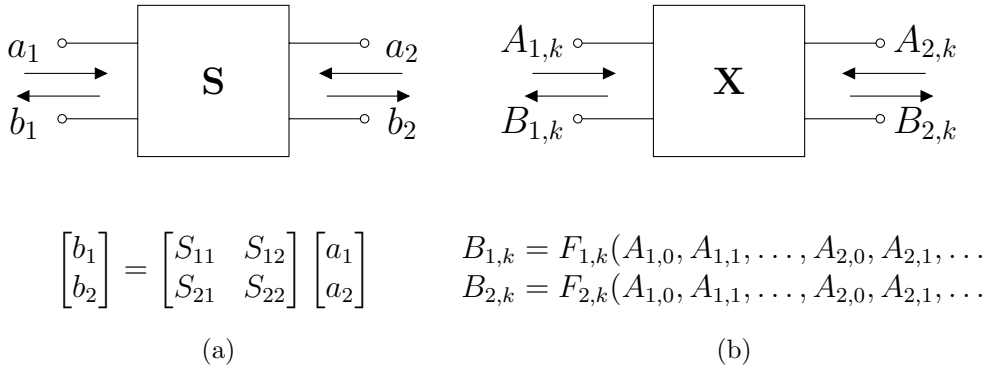
component is usually called Q. A constellation diagram is a representation of the complex envelope in the I-Q plane at symbol sampling instants. In this case the distortion performance of a radio transmitter is characterized by means of the error vector magnitude (EVM) metric. Transmitter imperfection, noise and distortion cause the the actual constellation points to deviate from the ideal location. An error vector is a vector in the I-Q plane between the ideal constellation point and the received point, in other words it is the difference between the actual received symbols and the ideal symbols. The EVM is equal to the ratio of the amplitude of the error vector to the amplitude of the reference [27]. It can be defined either in dB or as a percentage:

$$\begin{aligned} EVM(dB) &= 10\log_{10}\left(\frac{P_{error}}{P_{reference}}\right) \\ EVM(\%) &= 100\cdot\sqrt{\frac{P_{error}}{P_{reference}}}\ . \end{aligned} \tag{2.43}$$

Statistical evaluation of digitally modulated signals is a realm where computer-aided design (CAD) really shines. Commercially available CAD packages oftentimes offer envelope simulation methods based on non-linear behavioural circuit models. Those algorithms numerically compute the envelope dynamics in the presence of a carrier signal at a much higher frequency, they proceed at the rate of the slow modulating signal and the computation time is insensitive to the frequency of the fast carrier signals. The efficiency of this method is the result of using the most appropriate method for each of the circuit modes: harmonic balance for the fast behaviour and time-domain integration for the slow behaviour in order to capture transient phenomena and memory effects [25]. To further reduce the computation required to extract the envelope of the output signal, nonlinear models for the circuit behaviour are employed. The most widely used is the polyharmonic distortion (PHD) modeling [28]. The PHD modeling (also called X-parameter [1] modeling) is a black-box, frequency-domain modeling technique. All information needed to construct a PHD model is acquired through externally stimulating the signal ports of a device under test (DUT) and measuring the response signals. The PHD model is identified from the responses of a DUT stimulated by a set of harmonically related discrete tones, where the fundamental tone is dominant and the harmonically related tones are relatively small.

X-parameters can be thought as an extension of the S-parameters to non-linear circuits. A visual comparison of the models and their equation is given in Figure 2.9(a) and 2.9(b). Conventional S-parameters are defined only for linear systems, or systems behaving linearly with respect to a small signal

[1] "X-parameters" is a registered trademark of Agilent Technologies.



$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad \begin{aligned} B_{1,k} &= F_{1,k}(A_{1,0}, A_{1,1}, \ldots, A_{2,0}, A_{2,1}, \ldots) \\ B_{2,k} &= F_{2,k}(A_{1,0}, A_{1,1}, \ldots, A_{2,0}, A_{2,1}, \ldots) \end{aligned}$$

(a) (b)

Figure 2.9: Representation of S-parameters (a) and X-parameters (b) models for a given circuit and their equations. The index k in $B_{1,k}$ and $B_{2,k}$ denotes the kth-harmonic response.

applied around a static operating point (e.g., fixed bias condition of a transistor). As previously discussed, virtually all real systems are non linear: they generate harmonics and show intermodulation distortion and spectral regrowth. S-parameter theory doesn't apply to such systems. It may be a good approximation over some range of input, but it is incapable of even estimating the nonlinear response of real systems. The PHD approach assumes the presence of discrete tone signals (multisines) for the incident as well as for the scattered waves. As a result, the reflected waves at port n and harmonic index k, B_{nk}, are a function of the amplitude of each incident signal. In general, these discrete tones may appear at arbitrary frequencies, as explained in [29].

The PHD model can be linked to harmonic balance and envelope simulators that are capable of implementing black-box frequency-domain models. In fact, the mathematical structure of the equations fits these simulators like a glove. This results in reduced memory requirements and fast simulations. This model can also be applied to modulated signals to simulate the spectrum and envelope of modulated signals [28]. Moreover the PHD model is very accurate for a wide variety of nonlinear characteristics, including compression, AM-PM, harmonics, load-pull, and time-domain waveforms.

2.4 From System-level to Circuit-level Specifications

The analysis in [3, 30] shows that, when highly directional steerable antennas and beam combining techniques are used, the most favourable 5G band in

terms of power consumption and propagation losses is the 28 GHz band. In this band transmitter and receiver antenna gains are sufficient to offset the negative effects of increased path loss and reduced efficiency due to technology limitations. In this section a simplified transmitter model will be used to find a ballpark value for the minimum average PA output power, as a function of the modulation scheme, for a given distance between transmitter and receiver in a typical 5G line of sight scenario.

With reference to Figure 2.10, by rewriting the Friis transmission equation [19] in order to find the minimum transmit power required for reliable signal detection we get:

$$P_{TX,min} = P_{RX,min} + 2 \cdot L_S + L_{TX} + L_P + L_{RX} - G_{TX} - G_{RX} \tag{2.44}$$

where $P_{RX,min}$ is the minimum power at the receiver for reliable detection, L_S represents the losses due to the TX/RX switch of the MMIC, L_{TX} is the sum of all the losses from the output pad to the antenna, L_P is the path loss at the carrier frequency, L_{RX} is the sum of all the losses from the receiving antenna to the input pad and G_{TX}, G_{RX} are the antenna gains for the transmitter and receiver respectively. The minimum received power is expressed as follows [30] and takes into account the signal bandwidth BW, the noise figure of the receiver NF_{RX} and the target SNR of the modulated signal SNR_{sig} for a BER of 10^{-3}

$$P_{RX,min} = 10 \log_{10}(BW \cdot k_B T \cdot 10^3) + NF_{RX} + SNR_{sig} \ . \tag{2.45}$$

Table 2.4 summarizes the SNR needed to reach the target BER for various modulation formats, data is calculated from [31].

In order to compute the minimum output power for a given line of sight range for a typical 5G transmitter, it has been assumed a 16-element array

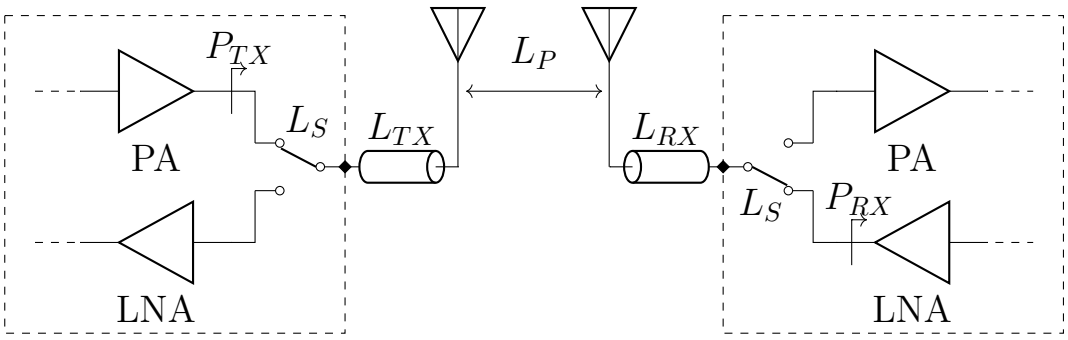


Figure 2.10: Illustration of link budget analysis scenario for a single TX/RX element in a 5G phased array.

as in [32]. This way for both the TX and RX antennas, with N_{ant} radiating elements, the gain can be approximated applying the formula from [30]

$$G_{TX,RX} = 10\log_{10}(N_{ant}) + G_{elem} \tag{2.46}$$

were G_{elem} is the gain of a single element. Using the same parameters for the reference system in [30], the resulting gain is 16 dB. The general criterion for the parameter choice is to represent the highest proven capabilities for system components from published literature. According to data in [30], assuming a carrier frequency $f_c = 28\,GHz$, the total losses due to the connection between the antenna and PA and LNA is $L_{tot} = 2 \cdot L_S + L_{TX} + L_{RX} \approx 20\,dB$. Finally the path loss [19] is calculated with the following formula:

$$L_P = 20\log_{10}\left(\frac{4\pi f_c}{c_0}D\right) \tag{2.47}$$

where c_0 is the speed of light and D the distance between TX and RX units.

By combining the previous relationships in order to find $P_{TX,min}(D)$ with data from Table 2.4 we obtain the plots in Figure 2.11. As expected, the most demanding modulation scheme is a 250 MHz wide 256-QAM. In order to obtain about 50 m line of sight range the PA is required to output at least 12 dBm on average. The $P_{TX,min}$ (in dBm!) is roughly halved to 7 dBm if a 250 MHz 64-QAM modulation is employed over the same distance. Low-power 5G use cases requiring longer range can employ lower modulation orders, down to QPSK, and also lower bandwidth. In fact, according to Equation (2.45), if the bandwidth is halved then the $P_{TX,min}$ is reduced by 3 dB. A point worth noting is that, in this analysis, amplifier distortion has been completely neglected. If it were to be considered then the SNR is reduced, and thus also the range, for the same amount of output power. Moreover, EVM is the main linearity specification to be considered. Thanks to the high transmission directivity at mmWave frequencies, the ACPR is less of an issue [30]. AM-PM and AM-AM

Modulation	SNR
QPSK	7 dB
16-QAM	11 dB
64-QAM	14 dB
256-QAM	18 dB

Table 2.3: Minimum SNR required by some sample modulation format in order to obtain a BER of 10^{-3} [31].

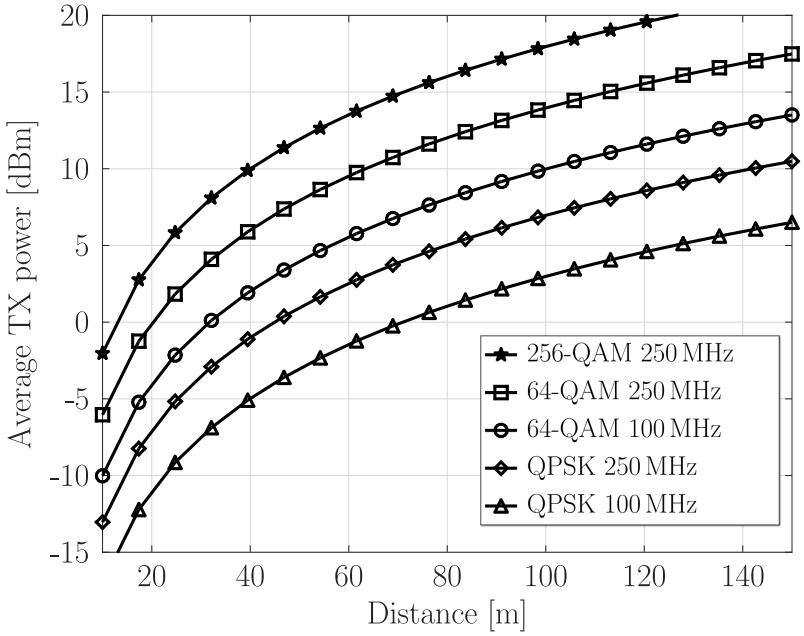


Figure 2.11: Minimum average PA output power as a function of distance for some sample modulation formats to obtain a BER of 10^{-3}.

distortion degrade the signal quality, increasing the EVM, and cause out of band spectral regrowth, degrading the ACPR. When a 64-QAM modulation is employed, the PA should ensure an EVM better than -25 dB to guarantee 3 dB margin over the SNR required to achieve 10^{-3} bit error rate on the received signal [30].

Digital predistortion based on look-up tables (LUTs) is an advanced yet relatively simple linearization technique widely used [33] to compensate for nonlinear behaviour in RF PAs. The most important issue with predistortion is that the estimation error should be minimized and the error correction has to be insensitive to process, voltage and temperature (PVT) variations. In a high-volume production setting, cost and complexity preclude the use of calibration [30]. Moreover hardware requirements explode if predistortion is applied to each of the RF chains in a phased array. Moreover, in 5G phased arrays the antenna elements operating at full power will exhibit a different phase shift than their attenuated counterparts. This undesired deviation leads to errors in the array's radiation pattern. Thus, 5G radios require PA having inherent circuit-level linearity.

2.5 Amplifier Classes

With the term operating class of a PA several different features can be referred to, ranging from the traditional bias point selection (Class A, AB, B or C), to the selection of matching network topologies (Class F, J, etc.) or to the operating conditions of the active device (Class D, G, E, S, etc.). Moreover, in the case of class A, AB, B and C, the identification of the operating class may be performed in terms of the conduction angle, i.e. the fraction of the RF signal period where a non-zero current is flowing in the active device. This definition is misleading since the conduction angle varies with the amplitude of the driving signal. In a class AB PA for example the active device is conducting for the whole period if the input signal is sufficiently small. A better definition is based on the quiescent bias point and will be used in this section, the conduction angle will be used to compare the different classes when the maximum output swing is reached.

All the classic power amplifier classes may be understood by studying the same simplified model sketched in Figure 2.13 and 2.15. In this model, the resistor R_L represents the load in which the output power is delivered, The inductance L_B feeds DC power to the collector and is assumed large enough that the current through it is constant and the collector is connected to the load via the capacitor C_B to prevent any DC dissipation in the load. Finally only the first harmonic of the collector voltage and current are considered, all the other harmonics are supposed to be short-circuited. The effect of the higher-order harmonics will be examined in Section 2.6.

2.5.1 Class A

In the class A power amplifier the bias levels are chosen so that the transistor is always conducting and it operates linearly. For a bipolar realization, this condition is satisfied by avoiding cutoff and saturation regions; for MOS implementations, the transistor has to be kept into the saturation region of operation. A typical bias point (labelled as Q) and load line for this kind of amplifiers is shown in Figure 2.12. Although class A is the most linear class [16], this linearity is provided at the expense of efficiency because there is always dissipation due to the bias current, even when there is no signal.

A simplified schematic and the resulting waveforms for class A operation are reported in Figure 2.13. Given all the previous assumptions about harmonic termination, the collector current can reasonably approximated by

$$I_{C,A}(t) = I_Q + i_c \cos(\omega t) \tag{2.48}$$

where I_Q is the quiescent bias current, i_c is the amplitude of the signal component of the drain current and ω is the operating frequency. The output voltage is simply the product of the current and the load resistance. From Kirkhoff voltages law (KVL) we get:

$$V_O = -R_L i_c \cos(\omega t) \tag{2.49}$$

Finally the inductor L_B presents a DC short, so the collector voltage swings symmetrically about V_{CC}. The drain voltage and currents are therefore offset sinusoids 180° out of phase with each other. As shown by the waveforms the transistor is always dissipating power because the product $V_{CE} \cdot I_C$ is always greater than 0.

To evaluate the theoretical efficiency of class A PAs the signal power delivered to R_L is calculated as

$$P_{out,A} = \frac{i_c^2 \cdot R_L}{2} \tag{2.50}$$

and the DC power, assuming that the quiescent drain current I_Q is made large enough to guarantee that the transistor does not ever cut off, is then:

$$P_{DC} = I_Q \cdot V_{CC} = i_{c,MAX} \cdot V_{CC} \ . \tag{2.51}$$

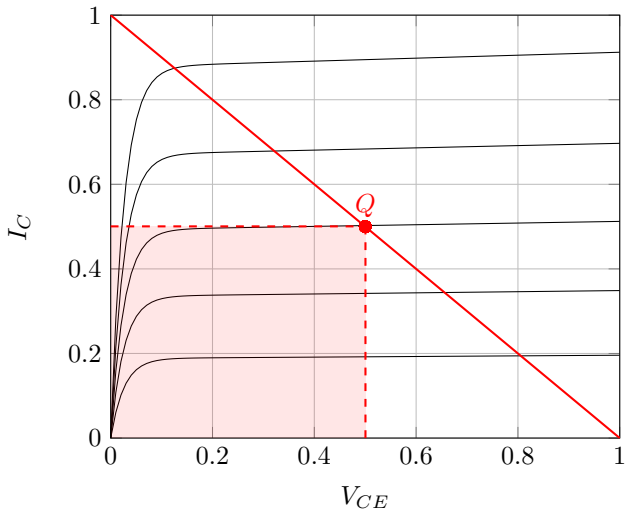


Figure 2.12: Load line for a typical class A amplifier. The point labelled as Q is the quiescent operating point.

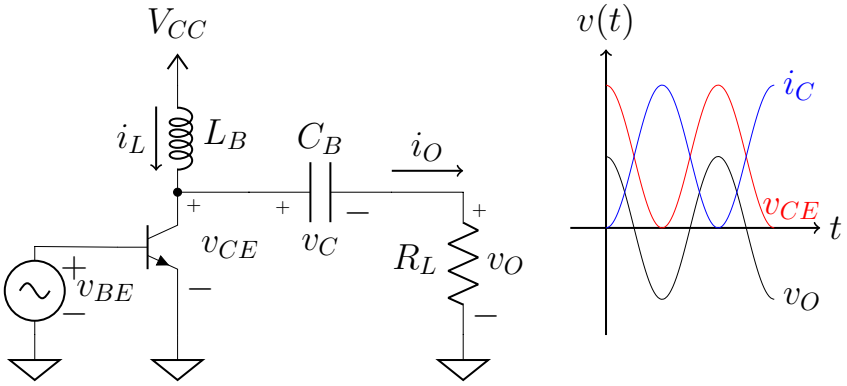


Figure 2.13: Simplified class A amplifier schematic and current and voltage waveforms.

By substituting Equation (2.50) and (2.51) into (2.15) we get that the collector efficiency of a class A amplifier is:

$$\eta_A = \frac{1}{2} \cdot \frac{i_c^2 \cdot R_L}{i_{c,MAX} \cdot V_{CC}} \ . \tag{2.52}$$

Since the absolute maximum value that i_c can have is $i_{c,MAX} = V_{CC}/R_L$, the maximum theoretical collector efficiency is 50 %.

2.5.2 Class B

In the class B amplifier, the bias is arranged in order to shut off the active device for half of the cycle. The PA load line is depicted in Figure 2.14 and simplified schematic and circuit waveforms are shown in figure 2.15. With intermittent conduction a significant number of harmonics are generated, since the collector current waveform is heavily interacting with the non linear cutoff region of the transistor.

The collector current is a half-wave rectified sinusoid and assuming that the output tank filters out all the harmonics of the current then a sinusoidal collector voltage waveform is left. Also in this case, the maximum voltage swing remains V_{CC} so the maximum output power is

$$P_{out,B} = \frac{(V_{CC})^2}{2 \cdot R_L} \ . \tag{2.53}$$

The DC input power is computed by calculating the mean value of $I_C(t)$ over a period of the waveform [16]. The resulting maximum theoretical efficiency is:

$$\eta_B = \frac{\pi}{4} \approx 0.785 \tag{2.54}$$

which is considerably higher than class A. With the class B amplifier we have accepted distortion in exchange for a significant efficiency improvement. In class A, the power consumption is maximum at zero output power, in class B when the output power is zero the transistor is not dissipating any power. The advantage of class B is that the DC collector current naturally scales with output power and so efficiency drops more gracefully as the power is backed off from peak output power. A comparison between the efficiency of class A and class B amplifiers as a function of the drive level is given in Figure 2.16.

2.5.3 Class AB

The bias of class AB amplifiers is just above the conduction region, such that the transistors conduct somewhere between 50 % and 100 % of the cycle, depending on the bias level chosen. As a result, its efficiency and linearity lie somewhere between those of a class B and class A amplifier. This compromise between efficiency and linearity and its higher power capacity (for a definition of power capacity refer to the next section) compared to class A and class B make it a popular choice for PA designers [16]. Moreover the class B operating point is an ideal mathematical point and most class B amplifiers are implemented as class AB PAs, as a trickle current is allowed to flow through the active devices to avoid cutting off the transistors during amplifier operation.

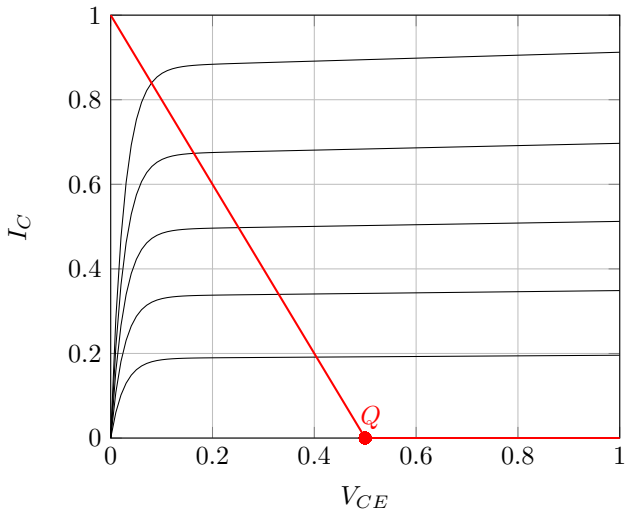


Figure 2.14: Load line for a typical class B amplifier. The point labelled as Q is the quiescent operating point.

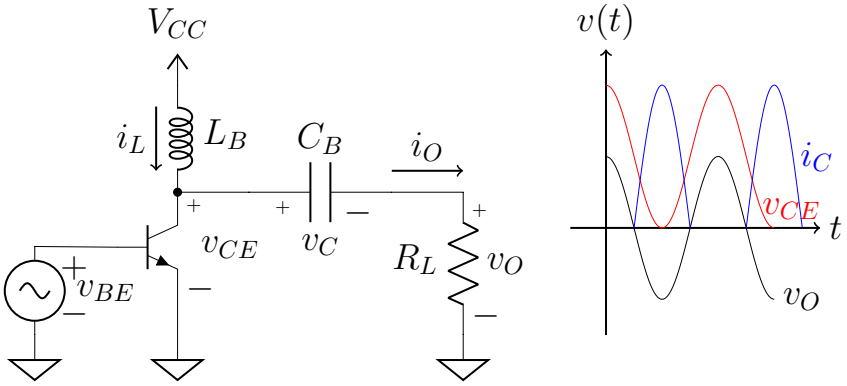


Figure 2.15: Simplified class B amplifier schematic and current and voltage waveforms.

2.5.4 Class C

The circuit of class C amplifiers looks no different from the class B amplifier or the class A amplifier. But in a class C PA, the bias is arranged such that the quiescent point is below device cut-off thus the transistor conducts less than half the time. The collector current consists of a periodic train of pulses

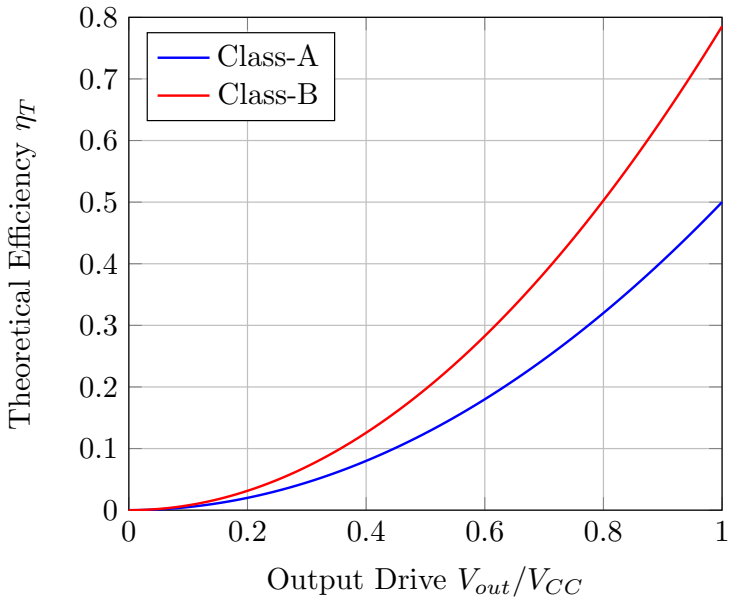


Figure 2.16: Efficiency comparison of class A and class B amplifiers versus output drive level [15].

Class	Conduction Angle	Bias Point (MOS)	Bias Point (BJT)
A	$\Phi = 2\pi$	Always in saturation	Always in active region
AB	$\pi < \Phi < 2\pi$	Above cut-off	Above cut-off
B	$\Phi = \pi$	At device cut-off	At device cut-off
C	$\Phi < \pi$	Below device cut-off	Below device cut-off

Table 2.4: Summary of PA classification in terms of conduction angle Φ and bias point.

which are approximated by top pieces of sinusoids [16]. Specifically the collector current is in the form:

$$I_C(t) = \begin{cases} \frac{I_{MAX}}{1-\cos\left(\frac{\Phi}{2}\right)} \left[\cos(\omega t) - \cos\left(\frac{\Phi}{2}\right)\right] & \text{if } \omega t \leq \frac{\Phi}{2} \\ 0 & \text{otherwise} \end{cases} \tag{2.55}$$

where ω is the operating frequency and Φ is the conduction angle at peak voltage swing [16]. We continue to assume that the transistor behaves all the time as an ideal current source and that all the harmonics of the collector voltage are filtered out by the output matching network (OMN) such that the output voltage is still sinusoidal. This waveform can be considered a generalization on the collector current waveforms of the aforementioned PA classes, depending on the choice of Φ. Operating class, conduction angle and bias point are summarized in Table 2.4.

We are interested in the DC term and first harmonic term of the Fourier series expansion of (2.55) $I_C(t) = I_0 + I_1\cos(\omega t) + \ldots$ which are [15]:

$$\begin{aligned} I_0 &= \frac{I_{MAX}}{2\pi} \cdot \frac{2\sin(\Phi/2) - \Phi\cos(\Phi/2)}{1-\cos(\Phi/2)} \\ I_1 &= \frac{I_{MAX}}{2\pi} \cdot \frac{\Phi - \sin(\Phi)}{1-\cos(\Phi/2)} \ . \end{aligned} \tag{2.56}$$

From the coefficients in (2.56) the optimum first harmonic load as a function of the conduction angle can be calculated. The optimum load is the load allowing for maximum voltage swing at the collector which, in the case of an ideal device with no knee voltage, corresponds to V_{DC}. So

$$R_{opt}(\Phi) = \frac{V_{DC}}{I_1(\Phi)} = \frac{2V_{DC}}{I_{MAX}} \cdot \pi \cdot \frac{1-\cos(\Phi/2)}{\Phi - \sin(\Phi)} \ . \tag{2.57}$$

In the same way we can obtain the RF power delivered to the load and the DC power absorbed from the supply as a function of Φ:

$$P_{DC}(\Phi) = V_{DC} I_0(\Phi) \tag{2.58}$$

$$P_{out}(\Phi) = \frac{V_{DC} I_1(\Phi)}{2} \tag{2.59}$$

from which we can calculate the maximum theoretical efficiency using Equation (2.15):

$$\eta_T(\Phi) = \frac{1}{2} \cdot \frac{\Phi - \sin(\Phi)}{2\sin(\Phi/2) - \Phi\cos(\Phi/2)} \tag{2.60}$$

According to (2.59) an increase in the output power over class A or class B can be obtained if class AB design is used. Since maximum swing is assumed this result does not account for gain performance and is independent of the PA drive voltage. The blue curve in Figure 2.17 plots the maximum theoretical efficiency as a function of conduction angle according to Equation (2.60). The efficiency performance exhibits a constant increase moving towards class C, with a limit value of 100 % when the conduction angle is zero. This is true, however, only to a first approximation, since the simplifying assumptions performed on the device behaviour would imply that, when the conduction angle is zero the transistor is always off and the current waveform approaches the Dirac delta function. Moreover as the conduction angle approaches zero also gain and output power tend toward zero.

One common way to quantify the relative stress on the devices is to define the *power capacity* or *normalized power output capability* [16], which is a dimensionless figure of merit expressed as the ratio of the actual output power to the product of the maximum voltage and current stress imposed on the device. Since the maximum collector voltage is $2 \cdot V_{DC}$ the power capacity is:

$$P_C(\Phi) = \frac{P_{out}}{V_{CE,MAX} \cdot I_{C,MAX}} = \frac{1}{8\pi} \cdot \frac{\Phi - \sin(\Phi)}{1 - \cos(\Phi/2)} \ . \tag{2.61}$$

The power capacity (red curve in Figure 2.17) is low for class C PAs at low conduction angles, while there is a maximum in class AB mode. In order to provide an output power comparable to that of a class A design, in a class C PA, the small conduction angle dictates that the output transistor be very wide so as to deliver a high current for a short amount of time [12]. The class A amplifier ($\Phi = 2\pi$) provides linearity at the cost of low efficiency and relatively large device stresses, while class B provides higher efficiency for the same power capacity. Class AB sits in between, offering higher linearity compared to class B and higher efficiency than class A. Moreover its power capacity is the highest among the classical amplifier classes, requiring lower chip area for the same amount of power [16].

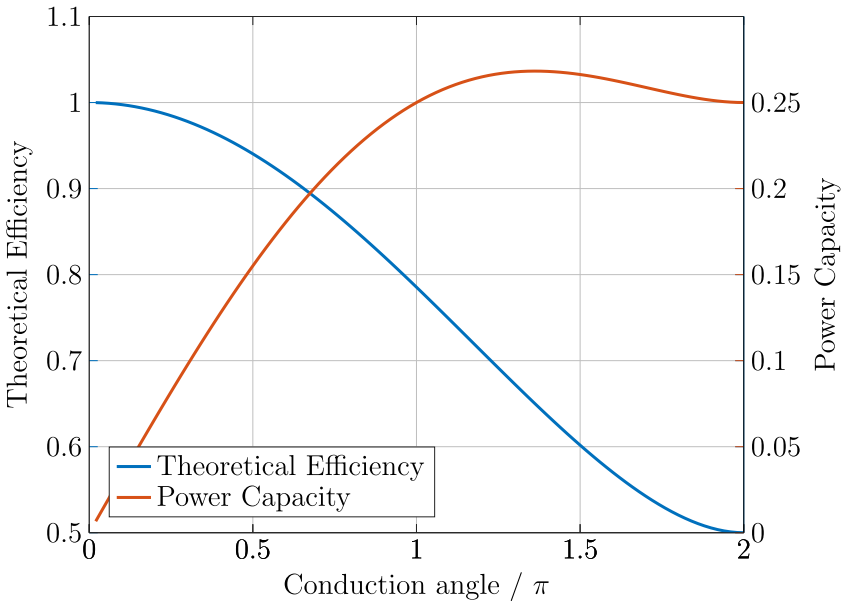


Figure 2.17: Theoretical efficiency and power capacity as a function of the conduction angle.

2.6 The Class J Power Amplifier

Contrary to what one's intuition might suggest, the maximum power transfer theorem is largely useless in the design of power amplifiers. One minor reason is that it isn't entirely clear how to define impedances in a large-signal nonlinear system. One more important reason is that even if we were able to do so and subsequently arrange for a conjugate match, the maximum efficiency would only be 50 % because equal amounts of power are dissipated in the source and load [16]. We have already discussed how maximizing efficiency is of primary importance in PA design, so the goal is to deliver a specified amount of power into a load with the highest possible efficiency while meeting the specifications on gain and linearity.

The main premise in the previous analysis on class A, B and C amplifier has been that the output transistor collector-emitter voltage waveform is sinusoidal, thanks to the filtering effect of the OMN. Parasitic capacitances, passive resonator losses and the turn-on characteristic of the active device modify the classical results in a substantial matter and the theoretical efficiency is reduced [24]. If the requirement of short-circuit harmonic termination is relaxed, higher harmonics can be exploited to improve the performance. The OMN can be employed to shape the waveforms, minimizing the time during

which the output transistor carries a large current and sustains a large voltage. This approach reduces the power consumed by the transistor and improves efficiency [12]. Moreover the harmonics can be used to shape the collector-emitter voltage in order not to interact with the nonlinear saturation region of the transistor. At the same time we can obtain the same behaviour and efficiency of a class B design with a more feasible matching network with no harmonic traps. This is what happens in class J power amplifiers [24].

The starting point for class J PAs is the class B amplifier in Figure 2.15. Let us suppose for a moment that the matching network between the active device and the load has no specific harmonic termination network. If we take into account the parasitic output capacitance of the active device, the ratio of the resulting capacitive reactance X_{Co} to the load seen by the device at the fundamental frequency

$$\rho = \frac{X_{Co}}{R_L} \tag{2.62}$$

becomes an important parameter in defining the PA operating mode. If $\rho \leq 1$ then the device output capacitance is large enough that for the harmonics greater than the fundamental it behaves as a short circuit and a good approximation of class B behaviour is obtained. On the other hand, if, depending on device technology and operating frequency, $\rho > 1$ then the circuit waveforms will deviate substantially from the classical analysis. Especially problematic are devices that run at low supply voltages and/or high frequency (such as CMOS and SiGe devices). The introduction of a substantial reactive component in the fundamental load can help in restoring the power and efficiency values close to the corresponding classical values. The voltage and current waveforms will be, however, far from classical [24].

In the presence of harmonics the voltage waveform on the active device is defined as follows [34]:

$$V(\theta) = V_{DC} - V_{1r}\cos(\theta) + V_{1q}\sin(\theta) + \sum_n V_{nq}\sin(n\theta) \tag{2.63}$$

where V_{DC} represents the DC supply voltage and $\theta = \omega t$ the angular phase of the signal. In this expression it is assumed that, since the current waveform contains only terms in cosine, the only dissipative voltage component is the fundamental which delivers power to the load. For convenience the voltage can be normalized such that $V_{DC} = 1$ so

$$v(\theta) = 1 - v_{1r}\cos(\theta) + v_{1q}\sin(\theta) + \sum_n v_{nq}\sin(n\theta)\ . \tag{2.64}$$

The concept of class B operation can be generalized by noting that, in order to maintain linear behaviour, the following conditions on (2.64) must hold in

at least one value of θ:

$$v(\theta) = 0, \quad v'(\theta) = 0 \ . \tag{2.65}$$

This means that the voltage waveform "grazes" zero with derivative equal to zero [34]. There exists a family of waveforms that satisfy this condition having the form:

$$v(\theta) = (1 - \beta\cos(\theta))(1 - \alpha\sin(\theta)), \quad (-1 \leq \alpha \leq 1,\ 0 \leq \beta \leq 1) \tag{2.66}$$

for which the generalized class B conditions expressed by (2.65) will be met at $\theta = 2k\pi,\ k \in \mathbb{N}$. The usual class B mode is obtained for $\alpha = 0$ and $\beta = 1$ which correspond in (2.64) to:

$$v_{1r} = 1; \quad v_{1q} = 0; \quad v_{nq} = 0 \ . \tag{2.67}$$

Since $\beta = 1$ corresponds to a unity value of the v_{1r} parameter, for each choice of α, the class B standard for efficiency is maintained. In practice, to avoid knee clipping, the value of β will usually be slightly lower than unity, resulting in a corresponding reduction in efficiency. The voltage expression in (2.66), along with the assumed class B-type current waveform, defines a continuous set of tuning conditions that lie between the limiting cases of class J* ($\alpha = -1$), thru conventional class B ($\alpha = 0$), to class J ($\alpha = 1$).

Assuming $\beta = 1$, all cases result in PAs having the same output power and efficiency as a conventional class B design, but with reactive, rather than short-circuited higher harmonics [34]. The waveform set, with $-1 \leq \alpha \leq 1$ and $\beta = 1$, is plotted in Figure 2.18. The higher cases of $|\alpha|$ cause higher peak voltages than are typically encountered in conventional harmonic-shorted PA modes. There is however a range of potential applications where higher peak voltages can be sustained. These include handset type PAs that run off a low voltage supply, and high power designs using Gallium Nitride devices whose limiting conditions are mainly driven by heat dissipation, rather than voltage breakdown, considerations [34].

The family of voltage waveforms in (2.66) can be generated, starting from the intrinsic collector current, by an appropriate choice of termination impedances for each harmonic. The intrinsic collector current in Equation (2.55), when the PA is biased in class B ($\Phi = \pi$), can be approximated by [35]:

$$I_C(\theta) = \frac{I_{MAX}}{\pi} + \frac{I_{MAX}}{2}\cos(\theta) + \frac{2I_{MAX}}{3\pi}\cos(2\theta) \tag{2.68}$$

where I_{MAX} is the maximum drain current.

The optimal load resistance at the fundamental frequency for a class B PA is obtained from Equation (2.57) with $\Phi = \pi$ and it results in $R_{opt} = (2V_{DC})/I_{MAX}$.

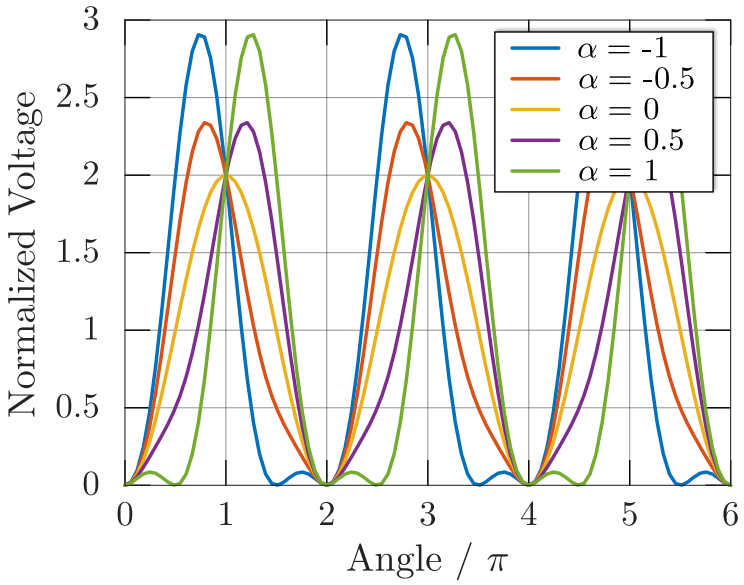


Figure 2.18: Generalized class B voltage waveforms as a function of the parameter α.

Then the optimal impedances seen by the active device at the fundamental ($Z_{L,1}$) and second-harmonic ($Z_{L,2}$) frequencies are [35]:

$$Z_{L,1} = \frac{V_1}{I_1} = R_{opt}(\beta + j\alpha) \tag{2.69}$$

$$Z_{L,2} = \frac{V_2}{I_2} = -j\alpha\beta\frac{3\pi}{8}R_{opt} \tag{2.70}$$

To realize an ideal class J (class J^{-1}) PA the optimal impedances for (2.69) and (2.70) must be presented to the transistor by the OMN. Thus, for ideal class J operation ($\beta = 1$ and $\alpha = 1$) the impedance has to be:

$$Z_{L,1} = R_{opt}(1 + j) \tag{2.71}$$

$$Z_{L,2} = -j\frac{3\pi}{8}R_{opt} \tag{2.72}$$

and for class J^{-1} ($\beta = 1$ and $\alpha = -1$):

$$Z_{L,1} = R_{opt}(1 - j) \tag{2.73}$$

$$Z_{L,2} = j\frac{3\pi}{8}R_{opt}\ . \tag{2.74}$$

All the other higher-order harmonic terminations are short-circuited. This ideal impedances are plotted on the smith chart in Figure 2.19.

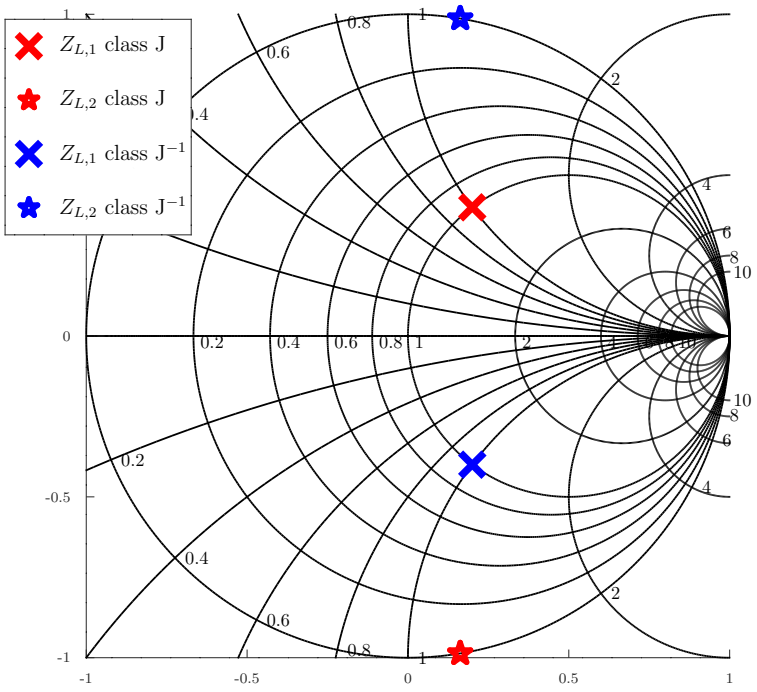


Figure 2.19: Ideal class J and class J^{-1} first and second harmonic impedances on the smith chart.

Chapter 3

Class J Power Amplifier Design

3.1 Class AB vs Class J: 10 GHz Radar

In this section, a class AB and a class J PAs for X-band phased array radar applications are presented. The class AB design features the cascade of a 8-bit programmable gain amplifier (PGA) and a conventional class AB PA core, leading to a gain variation range of over 50 dB with a phase shift deviation of $<4°$ over a 25 dB attenuation range. The performance of the class AB design is compared against a class J PA for the same target application to verify the effectiveness of the class J harmonic tuning approach in improving the efficiency. In the case of class J, integrated transformers are used to implement the input matching network and to synthesize the output class J load, while providing single-ended to differential conversion.

Recent advances in SiGe technologies enable the implementation of cost-effective active electronically-scanned phased-arrays (AESAs) in silicon. As it is the case for 5G, these arrays are typically built using hundreds or even thousands of transmit-receive (T/R) modules like in Figure 2.1). In typical T/R implementations, the phase and amplitude control blocks also affect, respectively, the attenuation and phase shift in the signal path, which is an undesired behavior. Hence, a two-dimensional calibration table is typically required. The proposed PA implementations target the X-band and are tailored for radar applications. The implemented PGA shows quasi perfect phase invariant amplitude control in order to reduce calibration efforts down to a one dimensional table. An additional programmable RF signal phase inversion furthermore eases the implementation of the phase control reducing the range the phase shifter is required to display from 360° to 180°. Complete PGA and PA biasing is monolithically integrated as well as the digital-to-analog converter (DAC) and a serial peripheral interface (SPI).

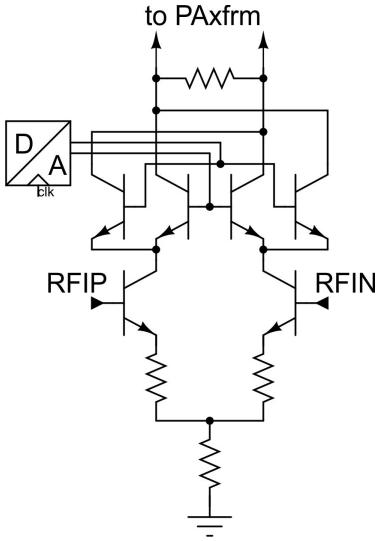


Figure 3.1: Class-A PGA with cross-coupled current steering schematic.

3.1.1 Class AB PA Design

The class AB PA has been designed by Infineon technologies Villach [36]. It is a two-stage design, the simplified schematic of the PGA that drives the PA is shown in Figure 3.1. The gain control is implemented through current steering. The RF current is usually steered to the supply, resulting into a large phase error [37]. In this work, cross steering (or canceling steering) of the RF currents is preferred as it inherently features a very low phase variation versus gain control due to the symmetric operating points of the cross-coupling NPN transistors. The highly sensitive control of the steering base voltages is solved by using accurate 8 bit on-chip DACs, easily implemented in BiCMOS technology. No analog linear-to-dB amplitude control is used, this functionality being shifted to the digital domain. The cross-coupled steering also elegantly implements a signal inversion capability: zero attenuation is provided for the DAC input code set to the lower (0) or upper (255) values, with opposite signal phase. Maximal attenuation, limited by finite layout symmetry and device matching, is achieved for an input code set at mid scale (127). The PGA operates in class A and is supplied from a standard 3.3 V supply voltage with a nominal supply current of 25 mA, chosen sufficiently high not to limit the PGA-PA output compression point and saturated power.

The schematic of the push-pull class AB PA core is shown in Figure 3.1. The PA uses a separate supply for best efficiency and improved PGA-PA isolation. The PA supply voltage was chosen to 1.8 V as the best compromise between output power and bipolar device reliability. The input transformer

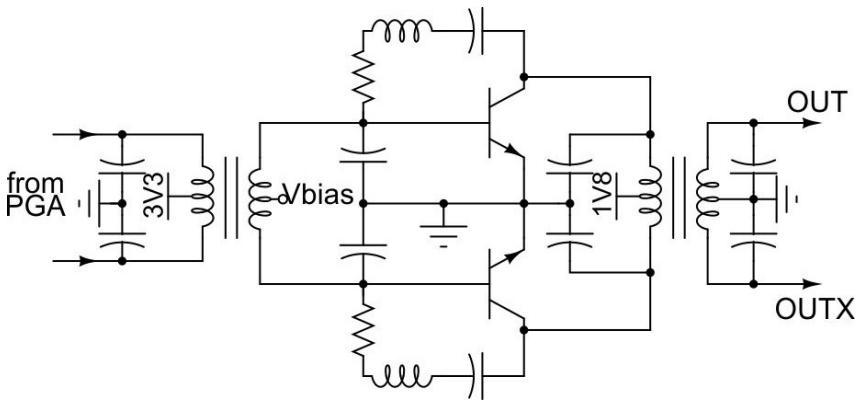


Figure 3.2: Class-B PA simplified schematic.

is part of the PGA load, making up a parallel resonant tank. Its middle tap is used to bias the PA. The biasing voltage generation is realized completely on-chip with low output impedance, such that no external biasing is needed. The intrinsic feedback of the bipolar transistors through the base collector capacitance is one of the most important sources of circuit instability. To avoid this, a passive frequency selective feedback in parallel to the base collector capacitance was inserted as proposed in [38]. The PA is loaded by an integrated transformer providing impedance transformation and electrostatic discharge (ESD) protection through its inherent galvanic isolation.

3.1.2 Class J PA Design

The schematic of the designed class J PA is shown in Figure 3.3. As described in Section 2.6, Class J operation leverages harmonic tuning to engineer the (single-ended) voltage waveform at the collector nodes of the amplifying transistors [24]. The presence of a strong second-harmonic component introduces an asymmetry in the waveform such that the corresponding voltage waveforms gracefully graze the bipolar transistors saturation region when approaching their minimum value. By eliminating the necessity of harmonic shorts or harmonic opens, compared to class E or class F, the realization of the output matching network is more practical. As a result the class J behaviour is maintained over a wider bandwidth [24, 39–41].

The starting point in a class J design is a class B PA where the load impedance Z_L shows an inductive component at the first harmonic and a capacitive termination at the second harmonic. The impedance values for the first and second harmonic are defined respectively according to Equation (2.71) and (2.72). In order to synthesize the required Z_L and, at the same time, cope

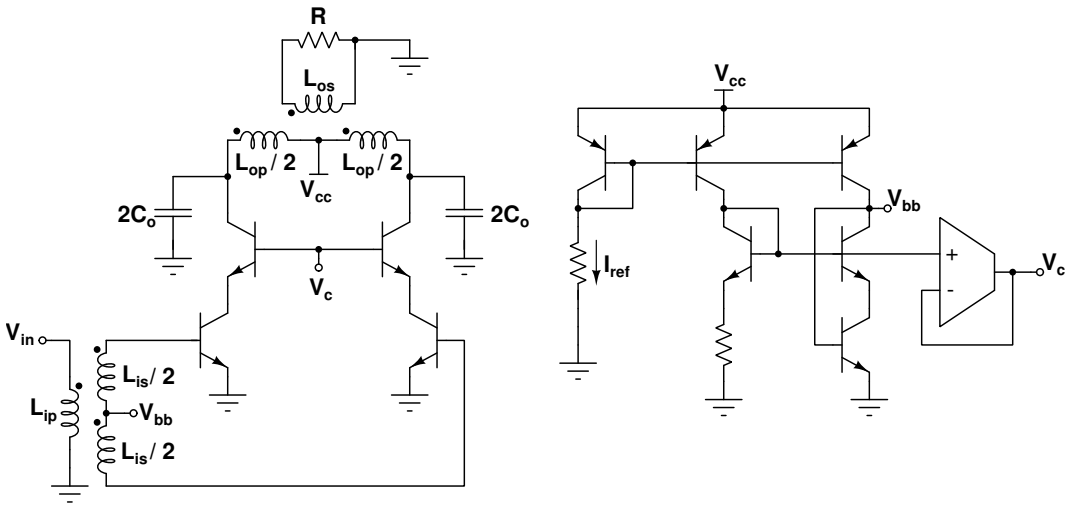


Figure 3.3: Class J PA simplified schematic, including bias circuit.

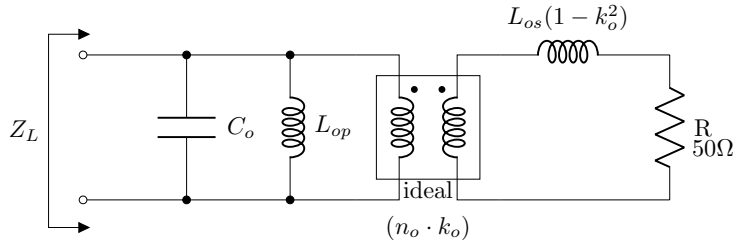


Figure 3.4: Equivalent differential Class J load network.

with the parasitic capacitances of the transistors, an integrated transformer has been used. An effective way to physically realize a proper class J harmonic termination is to embed the parasitic output capacitance into the load matching network so as to resonate it at the first harmonic and exploit its relatively low impedance at higher harmonics [36, 42].

The equivalent differential load network of the amplifier is depicted in Figure 3.4. The integrated transformer has been represented with a simple equivalent lossless model including an ideal transformer where L_{op} is the primary self-inductance and $L_{os}(1-k_o^2)$ is the leakage inductance at the secondary side. The transformer equivalent turns ratio is $n_o = \sqrt{L_{os}/L_{op}}$ and k_o is the mutual coupling coefficient. C_o is the total capacitance at the PA core output nodes. The load impedance seen by the PA core is then Z_L. The elements of the matching network should be sized to bring the values of Z_L at the fundamental frequency and at its second harmonic as close as possible to those needed

for class J operation. In this respect, the use of a transformer brings several benefits.

First, the capacitance C_o, which is in part made of the active devices parasitics and in part of an explicit capacitor, can be resonated with L_{op} at ω_0. Thanks to the resonance, the resulting value of $Z_L(\omega_0)$ is given by the transformer leakage inductance ($(1-k_o^2)L_{os}$) reflected to the primary side in series with the equivalent load resistance. Thus, as a second benefit, the required load reactance at ω_0 can be obtained, without additional waste of silicon area, by properly tuning the leakage inductance value. Third, the equivalent output transformer turns ratio, $n_o \cdot k_o$ can be set to step-down the $R = 50\Omega$ termination resistor into $R_L = R/(n_o \cdot k_o)^2$, the load resistance needed to achieve the desired output power. As a result, $Z_L(\omega_0)$ can be synthesized to match exactly the ideal class-J first harmonic impedance. Finally, the transformer can be configured as a balun, allowing a differential to single-ended transformation. This allows to have a differential PA core, which is beneficial in terms of maximum voltage swing, while having a single output pad.

Class J theory dictates that there is no other harmonic component in the voltage apart from the first two and hence for the higher-order harmonics the ideal load impedance must behave like a short. In this respect, the parasitic capacitance at the PA core output nodes comes in handy as it has the tendency to provide a short to all of the higher-order harmonics. There is however a price to be paid for the efficiency improvement: the capacitive second harmonic termination increases the peak voltage of the waveform compared to the sinusoidal case [24]. This can lead to an increased stress on the devices if the supply voltage is not scaled accordingly. To address this issue and to improve reverse isolation and stability, the amplifier uses a cascode configuration. The PA is supplied by a single 2 V supply. The active devices are biased in class AB by means of a high-swing cascode current mirror. The low impedance biasing scheme is key, since class J operation involves a strong voltage (common-mode) second-harmonic so the cascode bias voltage is buffered. At the PA input, a network based on an integrated transformer matches the transistor input impedance to a single-ended 50 Ω source.

The load synthesized by the proposed matching network has two impairments that must be taken care of. One is due to the fact that, if C_o is dominated by transistor output parasitic capacitances, its dependence on the amplitude of the voltage signal at the PA core output detunes the $L_{op} - C_o$ resonance at high output power, thus contributing to AM-PM distortion and leading the PA to non ideal class J operation. In order to limit this undesired effects, the fraction of C_o contributed to by transistor nonlinear capacitances should be made as small as possible. This target can be aimed at by reducing the size of

the output transistors (with a lower limit set by the fact that the maximum current density should be chosen so as not to drive the transistor too far into the high injection regime), and by making the value of C_o as large as allowed by the class J constraints, as discussed in the rest of the section, so that a large fraction of its value can be realized through external capacitors.

A second issue is that, as shown on the Smith chart in Figure 3.5, reporting a plot of the equivalent load impedance $Z_L(\omega)$ normalized to the first harmonic load resistance $R_L = 20\,\Omega$ and computed assuming $k_o = 0.7$, while the first harmonic perfectly matches the theory, there is a certain amount of mismatch between $Z_L(2\omega_0)$ and the ideal value $Z_{L,2}$ given by Equation (2.72). Luckily, having a second harmonic impedance that exactly matches the ideal value is not critical. As discussed in [41], trading-off some efficiency allows the second harmonic impedance value to deviate from the optimal value yet still

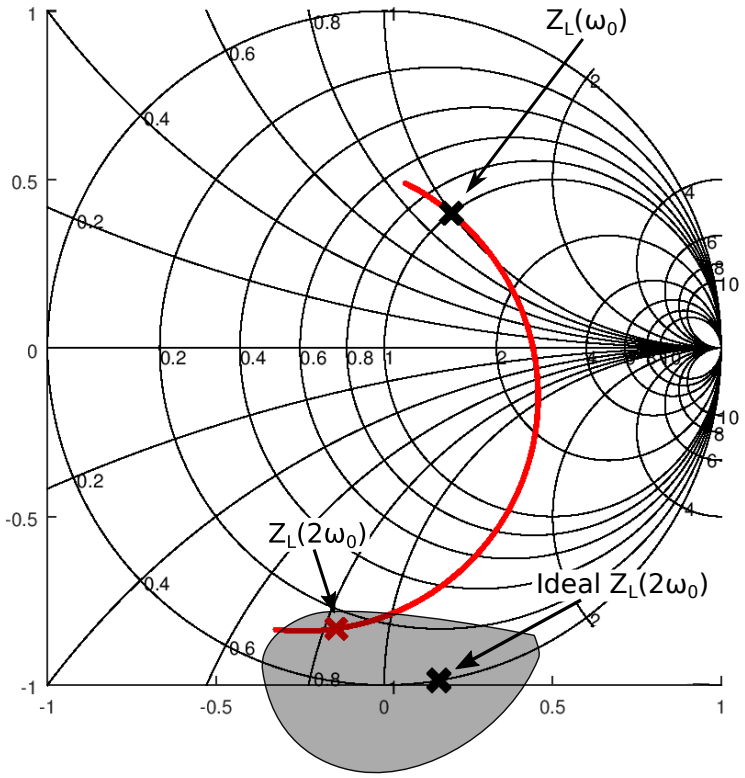


Figure 3.5: Load impedance (normalized to $R_L = 20\,\Omega$) versus frequency on the Smith chart. Annotated are the ideal and effective load impedance at first and second harmonic (the synthesized first harmonic perfectly matches the theory). The shaded area represents the clipping contour for $z_L(\omega_0) = 0.9 + j0.9$.

having class J amplifier operation. The theory in [41] demonstrates that, if the fundamental impedance is reduced with respect to the value yielding the maximum efficiency, a space of second harmonic impedance values, surrounding the optimal value, is generated such that the class-J requirements defined above are still satisfied. The boundary of this space is called *clipping contour*.

Values of $Z_L(2\omega_o)$ laying outside of the region defined by the clipping contour generate collector voltage waveforms that bring the bipolar transistors deep into the saturation region and the PA is not operating in class J any more. At the boundary we have perfect class J operation while inside the contour the collector-emitter voltage stays above the clipping region but still approaches it with derivative equal to zero so the PA is still showing class J waveforms but with lower efficiency. In this design the fundamental impedance has been reduced by 10 % with respect to the optimal value R_{Lopt}, yielding a maximum theoretical efficiency $\eta_{MAX} \approx 70\,\%$. By calculating the closed form expression for the impedance in Figure 3.4 for $\omega = 2\omega_0$ and by substituting the fundamental load condition defined in Equation (2.71) into the formula we get the following relation:

$$Z_L(2\omega_0) = \frac{(2-j)\frac{2}{3}\sqrt{\frac{L_{op}}{C_o}}}{1+j\left(\,2-\frac{2}{3}\frac{1}{R_L}\sqrt{\frac{L_{op}}{C_o}}\,\right)}\ . \tag{3.1}$$

We note that $\frac{1}{R_L}\sqrt{\frac{L_{op}}{C_o}}$ is in the form of a Q factor of a series RLC resonant circuit. As such it will be denoted by q_s.

Numerical analysis on the equations outlined in [41] has been used to compute the clipping contour for the normalized first harmonic load impedance $z_{\omega_0} = 0.9 + j0.9$. The impedance range that satisfies the class-J condition on the voltage waveform has been then converted into a requirement on the value of q_s:

$$0.82 \leq q_s \leq 1.15\ . \tag{3.2}$$

By noting that, at the fundamental frequency:

$$L_{op}\frac{1-k_o^2}{k_o^2} = \frac{R_L}{\omega_0} \tag{3.3}$$

and $\omega_0 = \frac{1}{\sqrt{C_o L_{op}}}$ we get the following formula that can be used to express the output transformer coupling factor k_o as a function of q_s:

$$k_o = \sqrt{\frac{q_s}{1+q_s}}\ . \tag{3.4}$$

Figure 3.6 plots the above equation. The shaded region shows the acceptable values of q_s, and thus the coupling factor for the output transformer that still

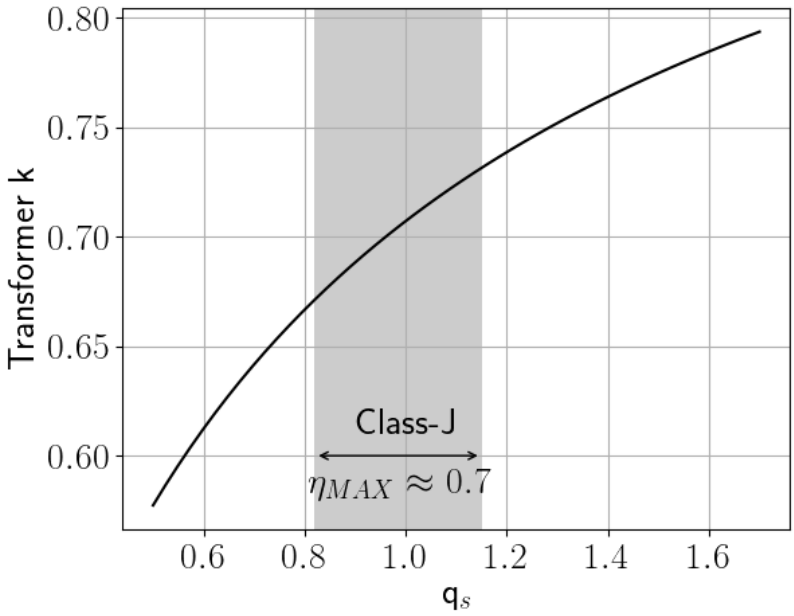


Figure 3.6: Range of q_s versus transformer k factor. The shaded region highlights the acceptable range for q_s that still enables class J operation in the presence of suboptimal second harmonic termination.

ensure class J operation with suboptimal second harmonic impedance. The range of admissible k_o values can be exploited to reduce the fraction of C_o due to the nonlinear output capacitance of the active devices, by noting that L_{op}, as given by Equation (3.3), monotonically increases with k_o. Then, lower values of k_o result in lower L_{op} and thus higher C_o, allowing to realize a larger fraction of it with external capacitors.

Taking all the previous considerations into account we fix a target output power of 200 mW, twice the desired maximum, in order to compensate for the losses in the devices and in the output network. The peak voltage swing at the collector node of the BJTs is limited by the collector-emitter breakdown voltage, which in this technology, is around 5 V. As mentioned before, in a class J amplifier the peak voltage is higher than a pure class B design. As such the voltage amplitude of the first harmonic on the collectors is set to 2 V. The single-ended 50 Ω termination resistor has to be transformed into a 20 Ω differential resistor in order to get the desired output power. This value takes into account the effect of the inductive termination at the first harmonic which reduces the voltage amplitude on the resistor by a factor $\sqrt{2}$. Once R_L has been chosen all the other circuit parameters can be calculated for any given choice of the output transformer coupling factor k_o. As discussed before lower

R_L	k_o	C_o	L_{op}	L_{os}
20 Ω	0.7	828.3 fF	305.8 pH	1.56 nH

Table 3.1: Output network component values for 10 GHz operation.

k_0 values would help to reduce the effect of the nonlinear output capacitance of the active devices. On the other hand, satisfaction of the clipping contour constraint with some margin, in order to safely accommodate the possible effect of device parameter spread, would suggest to pick a k_0 value in the middle of the shaded region in Figure 3.6. As a result a value of $k_0 = 0.7$ was chosen. The resulting component values for the output network are outlined in Table 3.1.

Figure 3.7 shows the ideal normalized current and voltage waveforms of a class J design, whereas the simulated waveforms are reported for comparison in Figure 3.8. The simulated voltage and current waveforms are obtained by plotting voltage and current at the collector nodes of the cascode devices with the designed load network. As those two figures show, the waveforms are in good agreement with class J theory and the devices are operating inside their safe operating area (SOA).

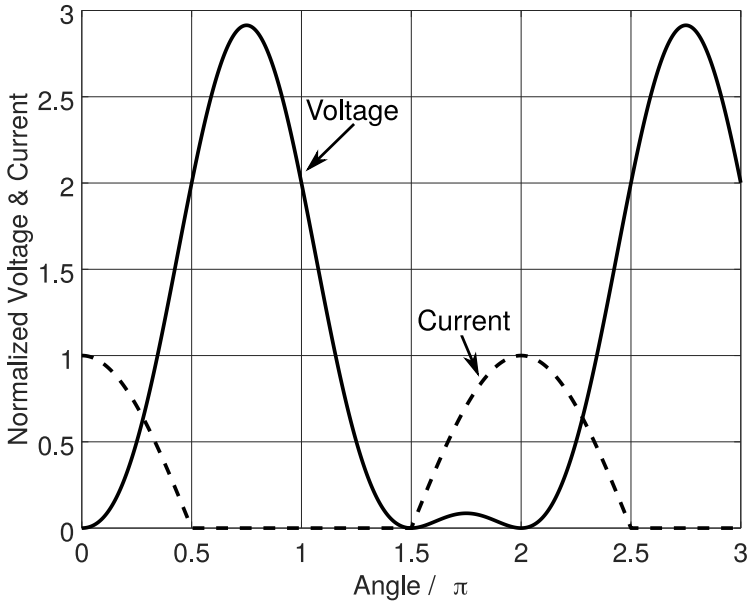


Figure 3.7: Ideal class-J normalized voltage and current waveforms.

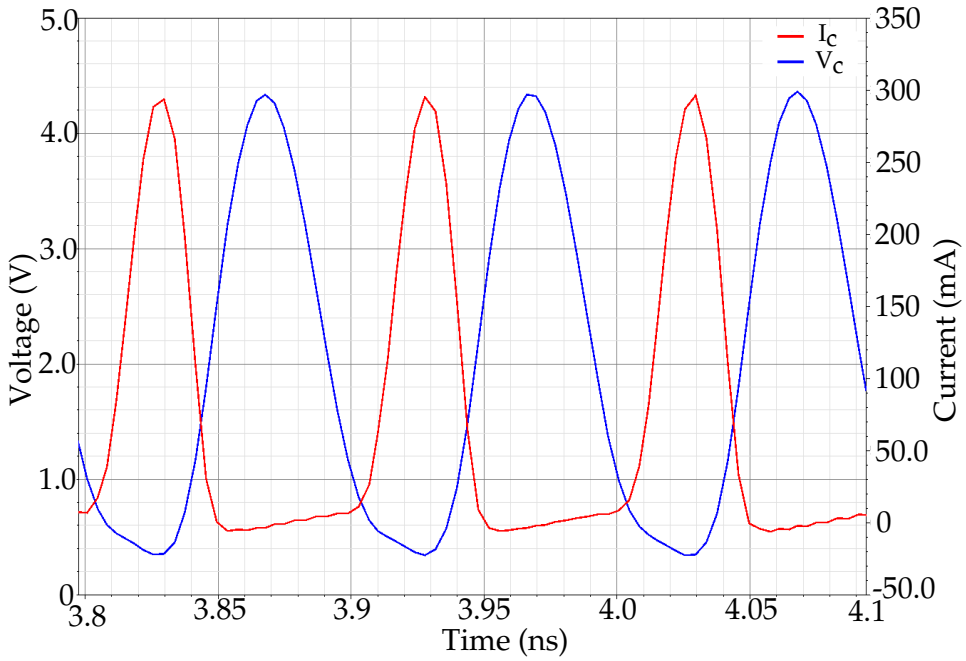


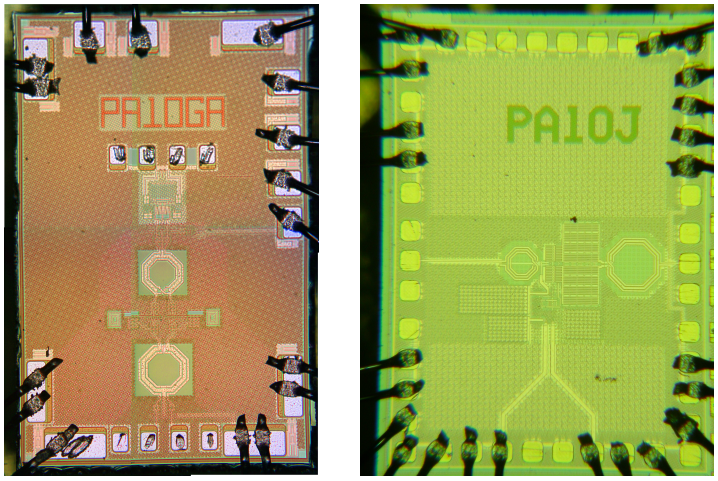
Figure 3.8: Simulated voltage and current waveforms at the collector nodes of the cascode BJTs, for $P_{in} = P_{in,1dB}$, with the load network outlined in Figure 3.4.

3.1.3 Measurements

The class AB PGA-PA combination including DAC and SPI digital control is implemented in Infineon 130 nm SiGe BiCMOS process featuring an $f_{\max}$ of 400 GHz [43]. The chip photograph is shown in Figure 3.9(a). The die area is 930 µm × 1400 µm.

All the following measurements report the performance of the cascade of the PGA and PA circuits. The small signal S-parameter measurements (with reference to 100 Ω differential input and output ports) are shown in Figure 3.10, and compared to simulation results. There is a substantially good agreement between measurement and simulations. The amplifier is input matched ($S_{11} < -10$ dB) up to 12 GHz, while the gain peaks at 23 dB at about 10 GHz. The measured 3 dB pass-band is 3 GHz.

The large signal experimental characterization of the class AB PGA-PA cascade, performed both at 27 °C and 85 °C, is reported in Figure 3.11 and 3.12. Figure 3.11 shows the power gain and output power of the amplifier, measured at 10 GHz. The measured saturated output power (P_{sat}) is 22 dBm at ambient temperature, with a minimal 1 dB decrease as the temperature is raised to 85 °C. On the other hand, there is a 3 dB decrease in the amplifier gain at



(a) (b)

Figure 3.9: Chip microphotographs for class AB and class J PAs. The class AB PA (a) has an area of 930 µm × 1400 µm while the class J PA (b) has an area of 1050 µm × 1450 µm.

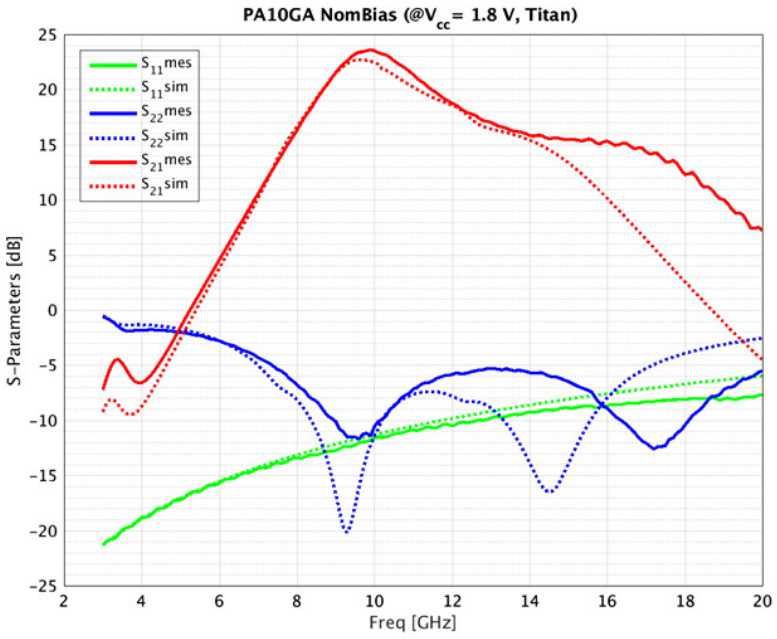


Figure 3.10: Measured versus simulated S-parameters of the class-AB PGA-PA.

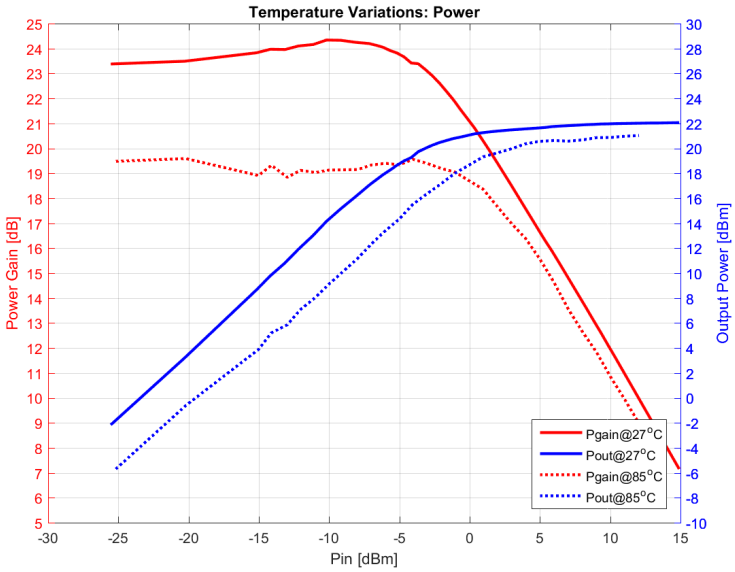


Figure 3.11: Measured G_P and P_{out} of the class AB PA at 27°C and 85°C.

85 °C, that results in a decrease of the PAE from 32 % to 27 % in the same conditions, as illustrated in Figure 3.12.

The class J PA is implemented in Infineon 0.35 µm SiGe bipolar technology [44]. The die, shown in Figure 3.9(b), has an area of 1050 µm × 1450 µm, of which only 730 µm × 430 µm are occupied by the PA, the rest being decoupling capacitors and pads.

The measured small signal S-parameters of the class J PA are shown in Figure 3.13, and compared to simulations (dashed lines). The peak gain is 20 dB, achieved around 9 GHz. The 3 dB bandwidth is 2.5 GHz. The effectiveness of the cascode configuration is proved by the reverse isolation, which is >40 dB making the amplifier unconditionally stable.

Figure 3.14 shows the small signal S_{22} versus frequency on Smith chart, both measured (solid line) and simulated (dashed line). The impedance at the first and second harmonic is emphasized by a thicker point. There is good agreement between the designed and resultant measured output impedance which confirms effective class J operation.

The power gain and the output power, measured at 9 GHz, are shown in Figure 3.15. The P_{sat} is 22 dBm, the input-referred P_{1dB} is −0.6 dBm. The PAE of the amplifier, measured at 9 GHz, is reported in Figure 3.16. It peaks at 36 %, showing the effectiveness of the class J approach in improving the efficiency of the PA.

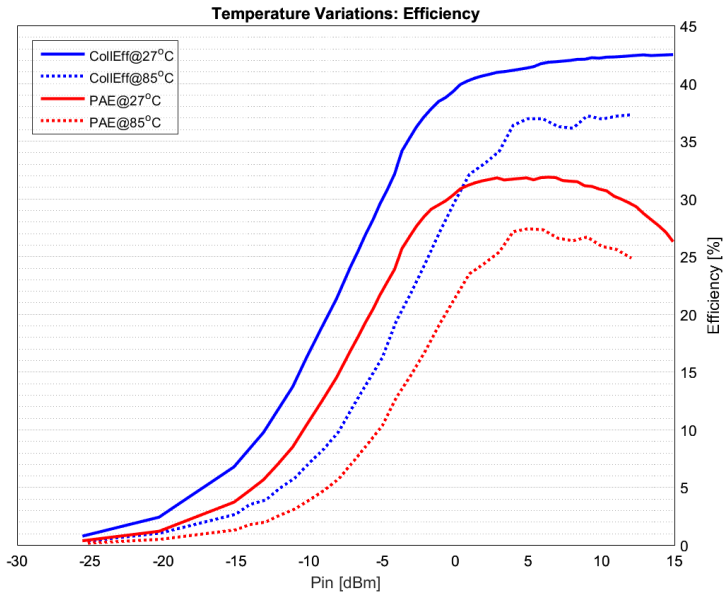


Figure 3.12: Measured collector efficiency and PAE at 27°C and 85°C.

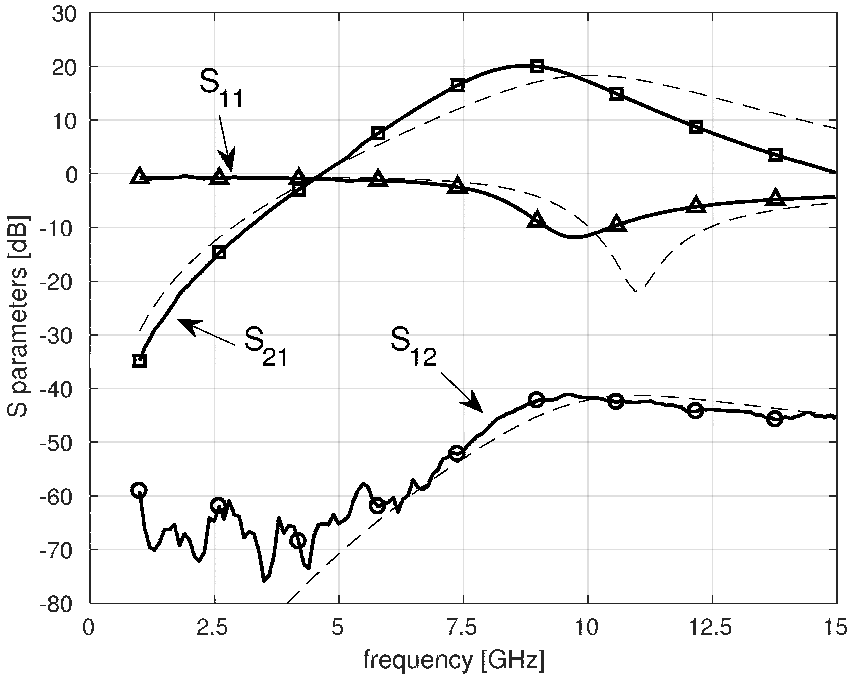


Figure 3.13: Measured versus simulated S-parameters of the class-J PA.

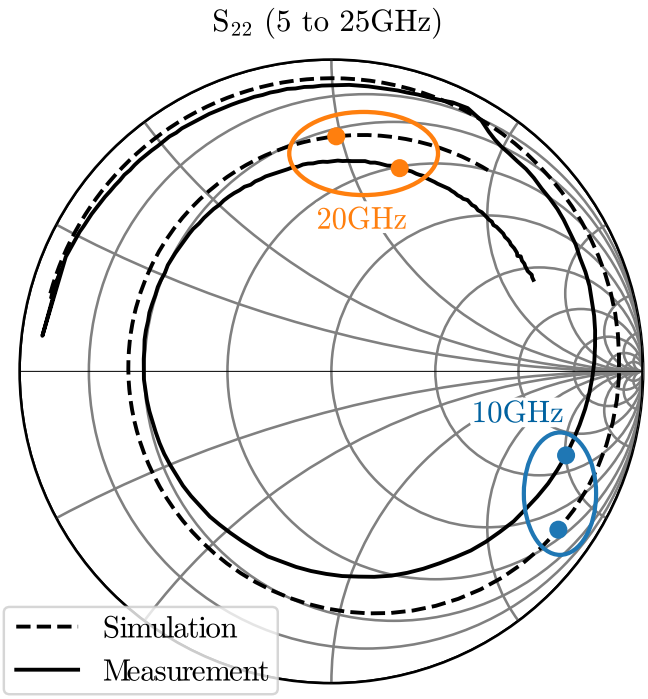


Figure 3.14: Smith chart plot of the measured (solid line) and simulated (dashed line) S_{22}.

3.1.4 Conclusion

In conclusion two PAs for X-band phased array radar applications that deliver 22 dBm of P_{sat} have been propoded and compared. The class AB PGA-PA combination features a digitally controlled gain variation range of over 50 dB. The phase error is <4° over a gain range of 25 dB. The overall PGA-PA cascade shows a PAE of 31 %. As a way to improve the peak PA efficiency, class J operation has been explored. The result is a PAE of 36 %. The performance of this work compares well to the state of the art [36], featuring an adequate bandwidth, an output power well above 20 dBm with a high efficiency and is additionally addressing crucial phased array features as amplitude control with lowest phase error enabling one-dimensional calibrations. All measured results are summarized and compared to the state of the artin Table 3.2.

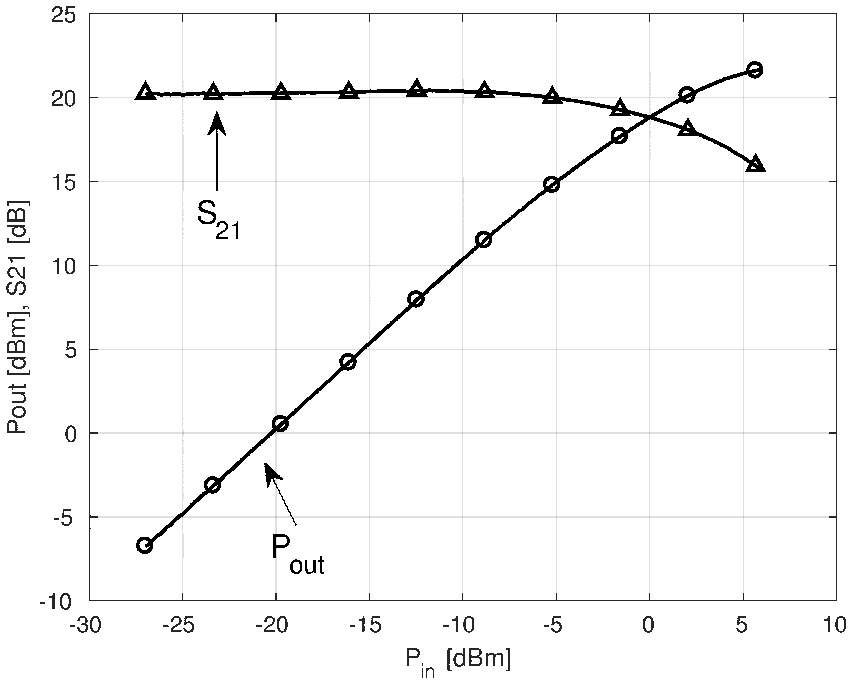


Figure 3.15: Measured power gain and output power of the class-J PA.

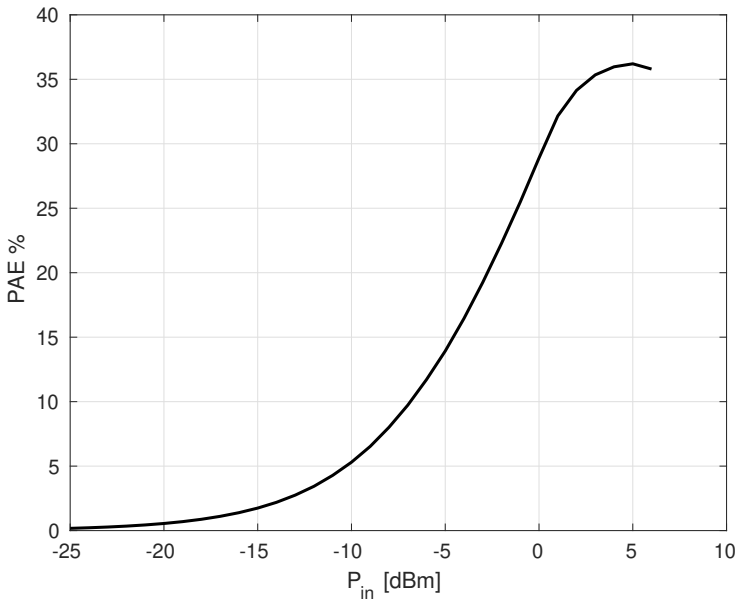


Figure 3.16: Measured efficiency of the class-J PA.

	Class-AB	Class-J	[45]	[46]	[38]	[47]	[48]
Freq. [GHz]	10	9	14	9	12.1	10	8.8
B_{3dB} [GHz]	3	2.5	–	3	2	4	3
Gain [dB]	23	20	16	25.5	21.1	27.7	21
P_{sat} [dBm]	22	22	24.4	23.3	23.4	29.5	27
PAE [%]	31	36	29.1	28	37.3	17.8	36
V_{CC} [V]	3.3/1.8	2	4	4	1.8	4.5/7.5	3.5
Area [mm^2]	1.3	1.4	0.4	0.6	1.7	2.7	1.0

Table 3.2: Measurement summary and comparison of the X-band PAs discussed in the present section with other state-of-the-art SiGe works.

3.2 28 GHz Class J 5G PA Design

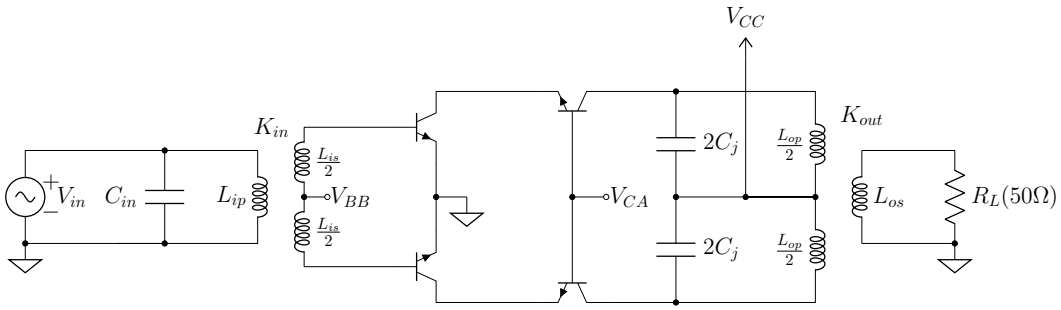


Figure 3.17: Simplified 28 GHz PA schematic, excluding bias.

To further investigate the benefits of class J operation another version of the PA presented in the previous section and in [36, 42] has been designed. The only difference with the previous design is the center frequency which is now 28 GHz. Its schematic, excluding the bias circuit, is shown in Figure 3.17. Once again, a cascode topology has been used for its higher output voltage swing, gain and reverse isolation compared to a single stage solution. Given its high efficiency and relatively high output power one possible application for such PA is base station phased array drivers. Taking into account PAPR, antenna gain and typical 5G link margin, it has been shown in [49] and in Section 2.4 that for an eight-element phased array the 1-dB compressed output power per antenna element should be greater than or equal to 15 dBm. As a safety margin, to compensate for the losses due to the additional elements connecting the amplifier to the antenna, it has been decided to target a P_{sat} of 23 dBm for the current design. The output matching network has been designed as before for a center frequency of 28 GHz. After solving the network in Figure 3.4 in order to satisfy the conditions for class J operation and for the required output power the component values outlined in Table 3.3 are obtained.

The IC has been fabricated using Infineon 130 nm SiGe technology. The chip photograph is shown in Figure 3.18. Die area is 930 µm × 930 µm of which 390 µm × 340 µm are used by the PA core, including integrated inductors.

R_L	k_o	C_o	L_{op}	L_{os}
20 Ω	0.7	296 fF	109 pH	557 pH

Table 3.3: Output network component values for 28 GHz operation.

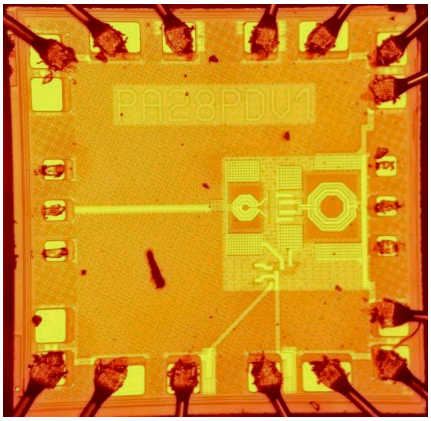


Figure 3.18: Chip photograph for the 28 GHz class J PA. Die area is 930 µm × 930 µm, active area is 390 µm × 340 µm.

The measured small-signal S-parameters are plotted in Figure 3.19 (solid lines) alongside their simulated values (dashed lines). The design shows a slightly lower center frequency than the simulated one due to circuit parasitics. The peak gain is 16 dB at 26 GHz and good input return loss is achieved from 25 GHz to 30 GHz. The −1 dB bandwidth goes from 22 GHz to 30 GHz easily covering the whole n257 and n258 5G bands [50]. The measured stability factor K is plotted in Figure 3.20. The minimum value is around 1.5 at 25 GHz which confirms that the circuit is unconditionally stable.

When evaluating amplifier performance, gain expansion by 1 dB has the same effect on linearity as 1 dB compression. The class J 28 GHz amplifier shows 1 dB gain expansion at an output power of 18 dBm, after which it starts compressing. The saturated output power is 20 dBm. Measured large signal gain and output power versus input power are reported as solid lines in Figure 3.21 while the dashed lines on the same figure represent the simulations. At low input power levels, there is good agreement between simulations and measurements. The difference at high input (output) powers is due to device self-heating within the amplifier core.

Figure 3.22 plots the measured PAE versus output power (solid line) compared with the simulation (dashed line). The peak PAE is 36 % at 19 dBm output power, in line with the state of the art and with previous results at 10 GHz and in good agreement with simulations.

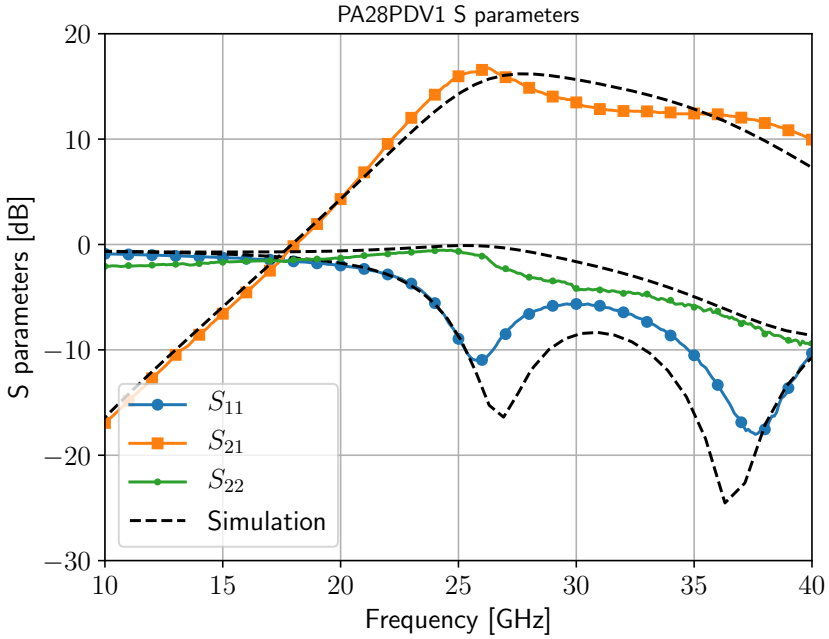


Figure 3.19: S_{11}, S_{21} and S_{22} measured (solid lines) and simulated (dashed lines) for the 28 GHz class J PA.

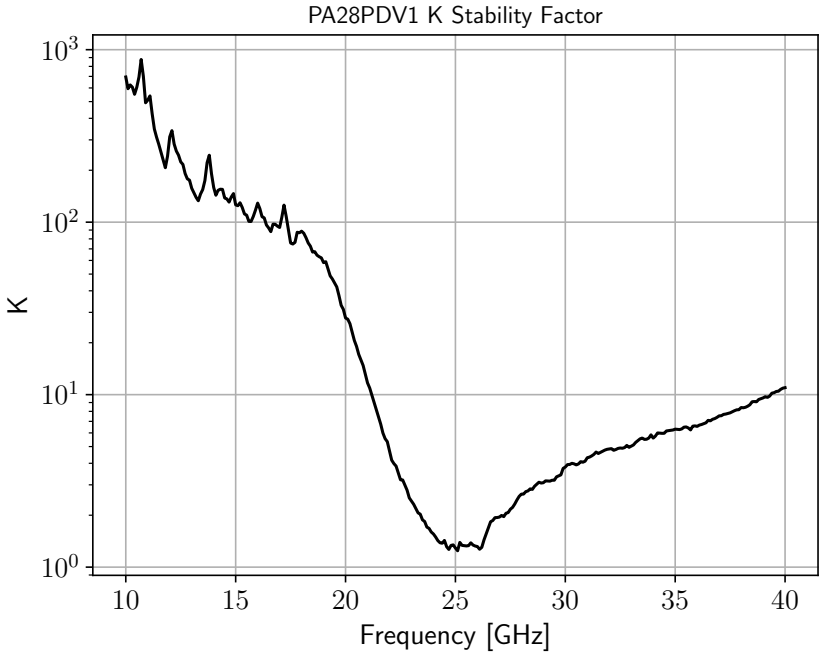


Figure 3.20: Measured stability K factor for the 28 GHz class J PA.

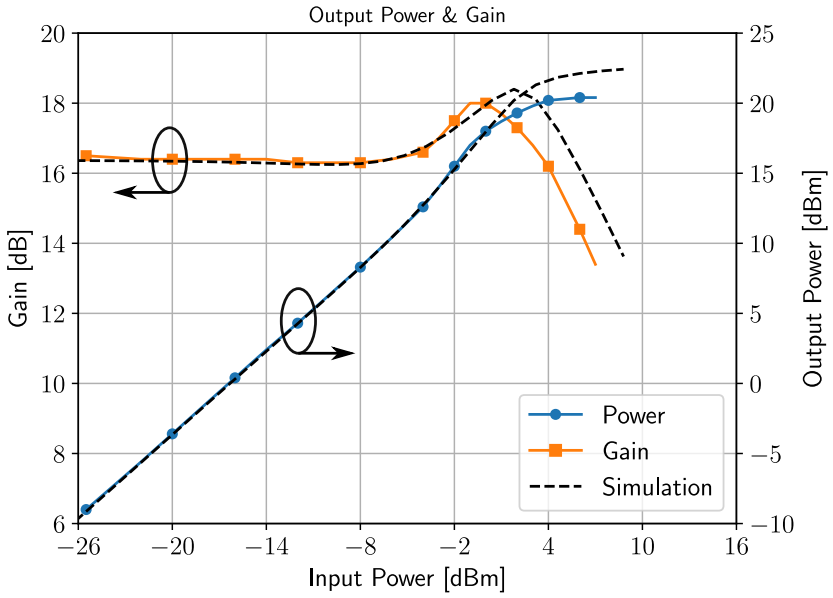


Figure 3.21: Measured output power and gain versus input power of the class J 28 GHz PA. Dashed lines represent simulations.

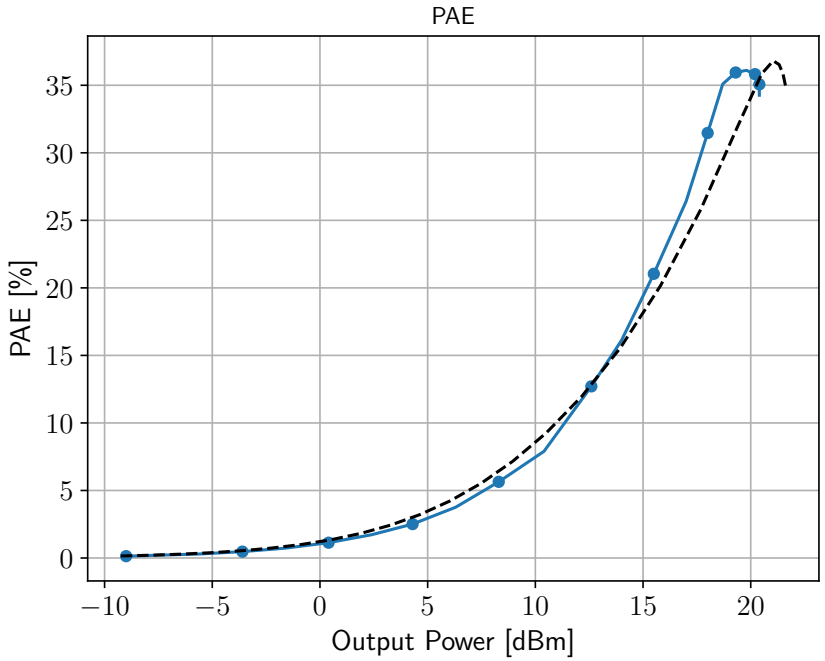


Figure 3.22: Measured PAE versus input power of the class J 28 GHz PA (solid line) compared with the simulation (dashed line).

	This PA	[53]	[30]	[49]	[51]	[52]
Technology	130 nm SiGe	180 nm SiGe	28 nm CMOS	130 nm SiGe	65 nm CMOS	45 nm SOI CMOS
Freq. [GHz]	26	28	30	28	24	28
B_{3dB} [GHz]	8	4	3.85	16	6	–
Gain [dB]	16	28.6	16	15.3	9	10
P_{sat} [dBm]	20	27.3	14	18.6	14.7	22.4
P_{1dB} [dBm]	18	23.2	13.2	15.5	14	21.5
PAE [%]	36	32.7	35.5	35	42.6	40
Supply [V]	2	2.8/3.8	1	3.6	1.1	2.4
Area [mm^2]	0.133	0.713	0.16	0.445	0.11	0.63

Table 3.4: Performance summary and comparison of the class J PA currently presented with the state of the art.

3.2.1 Conclusion

To further investigate the benefits on efficiency due to class J operation another PAs operating at a center frequency of 28 GHz has been designed, measured and discussed. The PA delivers a P_{sat} 20 dBm. The maximum achieved PAE of this work is 36 % which compares favourably with the state of the art summarized in Table 3.4. Other works achieving higher efficiencies report a lower output power [51] or resort to more refined and expensive technologies such as SOI CMOS [52].

Chapter 4

Improving Linearity

In this chapter a class J PA for operation in the X-band realized in SiGe bipolar technology is presented. The proposed design combines the high efficiency of class J operation, outlined in the previous chapter, with solutions to mitigate AM-PM distortion down to a level compatible with high spectral efficiency modulation schemes. The main sources of AM-PM distortion are identified in the base-emitter and collector-base BJT capacitance variation with power level and solutions that make the design less sensitive to these impairments are proposed. Linear metal-insulator-metal (MIM) capacitors are used at the PA core output to realize the proper class J second harmonic termination, while an input matching network based on a Bessel ladder filter is adopted to make the signal phase at the PA core input less sensitive to base-emitter capacitance variation. The 10 GHz class J PA outlined in Section 3.1 is used as a reference to highlight the trade offs entailed by AM-PM distortion reduction. The reference PA [36], is designed for radar applications and thus for maximum PAE with no concern on the AM-PM, the solutions adopted to mitigate AM-PM distortion and make it compatible with high spectral efficiency modulation schemes will be discussed.

With the advance of silicon technology, the trend is moving towards higher frequencies which offer larger bandwidths such as K, Ku or even Ka-bands. However, especially in satellite communications, frequencies above 12 GHz are less resilient to rain fade compared to the X-band [54,55]. To avoid outages that compromise availability and quality of service (QOS) due to the fluctuation of received signal level, many techniques have been proposed [56]. One of the most effective is frequency diversity which allows for almost complete fade restoration. Frequency diversity uses an alternate frequency band to avoid fade when the upper ones are not available. In this scenario, the X-band provides a useful diversity alternative to Ku, K and Ka-band [56].

4.1 Distortion Sources

As already discussed, the goal of the design in [36] was to maximize the PAE. In order to fulfil such goal the output class J capacitors are realized with back-to-back pn-junction varactors connected between the cascode BJTs collector node and V_{CC}. This configuration prevents forward-biasing of the diodes and partially compensates C_{BC} and C_{CS} variation when the collector voltage waveform is close to its maximum. This has been done in order to compensate the BJTs output capacitance variation with output power. This yields better class J operation at peak power but results in poor linearity. In the current design the output load employs MIM capacitors of the same nominal value as the reference. The current design also keeps the same PA core, bias circuit and bias decoupling capacitance as the reference design.

Class J PAs feature the same collector current waveform as their class B counterparts. As such the average current across the devices increases with increasing output power. This is a major source of non-linearity that can limit the amplifier performance with modulated signals. Figure 4.1 shows a simplified amplifier model where circuit elements whose values strongly depend on the collector current are highlighted.

The change in large-signal impedance at the input and output ports of the amplifier causes phase shift in the IMN and OMN, especially if the quality factor (Q) is high at the frequency of interest [57–59]. This phase shift is a main source of AM-PM distortion. Various compensation techniques exist to avoid this inconvenience, the most widely used of which is input signal predistortion [60]. Predistortion techniques may be complex and inconvenient, especially if the amount of distortion to be corrected is high. One approach to reduce, the amount of predistortion is making the matching networks less sensitive to the impedance variation of the active devices.

In this design, and in PAs in general, the OMN is not conceived for power match but instead for maximum efficiency. This results in a lower Q factor compared to the IMN. Thus the latter is to blame for the majority of AM-PM distortion. In fact, at the fundamental frequency, the output network behaves like a series of a resistor and an inductor whose reactance is equal to the resistance. Thus the output quality factor is: $Q_o = 1$. On the other hand the IMN is designed for power matching in the whole X-band (8 GHz to 12 GHz). Given that $Q_i = \frac{f_c}{\Delta f} = 2.5$ the circuit sensitivity to impedance variation is roughly twice as high at the input than at the output.

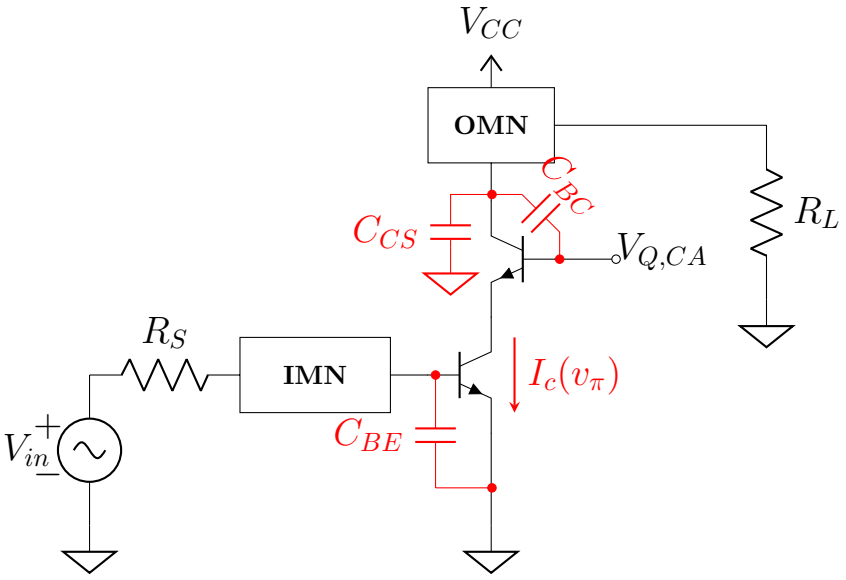


Figure 4.1: Simplified model of the power amplifier. The parasitic components (BJT input capacitance C_{BE}, cascode collector-junction capacitance C_{CS} and cascode base-collector capacitance C_{BC}) and the non-linear collector current are marked in red. Such elements contribute the most to AM-AM and AM-PM distortion.

4.2 AM-PM Distortion in Class J SiGe PAs

As discussed in Chapter 2, the Volterra series is able to model the AM-PM and AM-AM distortion of a typical PA well into its compression region. An important issue is how many polynomial terms are required in a typical case. In [61], a comprehensive analysis up to the third-order coefficient has been carried out. However as discussed by [24] when the output power approaches the P_{1dB}, higher-order harmonics come into play and cannot be neglected. As such the Volterra series has to to include their effect, further complicating the model.

In this analysis an approach based on [21], where trigonometric equations are solved in the time domain to obtain the phase of the signals, is presented. The effects of both the input and output impedance are taken into account and the contribution of each of them to the overall AM-PM are discussed. The models are derived under the quasistatic assumption: the amplitude and phase of the signals in the circuit are the same for a given input RF carrier amplitude, regardless of how quickly the signal envelope changes and are independent of previous history. Comparison against measured and simulated output phase

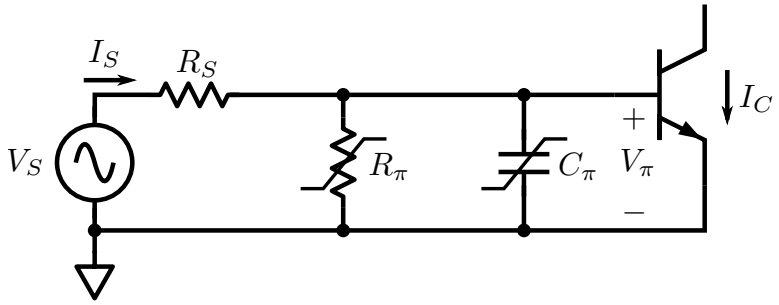


Figure 4.2: Equivalent schematic used to model the effects of BJT input impedance variation. Nonlinear elements have been de-embedded from the transistor.

variation versus input power on the PA prototype in Section 3.2 is provided to verify the effectiveness of the model. Simulations and measurements show good agreement up to P_{1dB}. Moreover the model has the advantage of providing formulas which are easy to reason about and can be used to make informed design choices to improve the PA linearity.

4.2.1 Input Impedance Contribution

The input impedance has been modeled as shown in Figure 4.2. The nonlinear elements (R_π and C_π) have been de-embedded from the active device which is considered to be linear ($i_C = g_m \cdot v_\pi$). The only contribution to the phase of the current is due to the interaction of C_π and R_π with the source resistance R_S. As a result the phase of the base-emitter voltage V_π is the same as the phase of the collector current I_C.

In active mode the diffusion capacitance is dominant over the junction capacitance, so C_π is considered as a function of the collector current according to the formula:

$$C_\pi(t) = C_{\pi,Q}\frac{I_C(t)}{I_{C,Q}} = \frac{C_{\pi,Q}}{I_{C,Q}}\, e^{v_\pi(t)/V_T} \tag{4.1}$$

where $C_{\pi,Q}$ is the capacitor value at the steady-state operating point.

If we ignore higher-order harmonics and assume the base-emitter voltage sinusoidal with an amplitude-dependent phase shift ϕ_i relative to the input sine wave, we get $v_\pi(t) = V_\pi \cos(\omega_0 t + \phi_i)$ and also that $C_\pi(t)$ is periodic and can be represented by a Fourier series in *capacitance*:

$$C_\pi(t) = C_{\pi,0} + C_{\pi,1}\cos(\omega_0 t + \phi_i) + C_{\pi,2}\cos(2\omega_0 t + 2\phi_i) + \cdots \tag{4.2}$$

where $C_{\pi,n}$ is the n-th harmonic Fourier coefficient of $C_\pi(t)$.

Considering the input loop in Figure 4.2, current and voltage must obey Kirchhoff's laws independently at every harmonic frequency. Therefore

$$V_s(t) = V_S \cos(\omega_0 t) = R_S \cdot I_s(t) + V_\pi(t) \tag{4.3}$$

$$I_s(t) = i_{C_\pi}(t) + i_{R_\pi}(t). \tag{4.4}$$

The capacitor C_π is specified in terms of its incremental capacitance versus base-emitter voltage: $C_\pi(v_\pi) = dQ_B/dv_\pi$ where Q_B is the base charge in the bipolar transistor. As a result $i_{C_\pi}(t) = C_\pi(v_\pi)\, dv_\pi/dt$. We combine (4.3) with (4.4), use (4.2) for $C_\pi(v_\pi)$ and note that $R_S R_\pi \gg 1$. Then the phase shift between $v_S(t)$ and $v_\pi(t)$ is given by:

$$\phi_i(V_\pi) \approx \arctan\left(\frac{R_\pi(V_\pi)}{\omega_0\left(C_{\pi,0}(V_\pi) - \frac{1}{2}C_{\pi,2}(V_\pi)\right)}\right) \tag{4.5}$$

The Fourier coefficients of $C_\pi(v_\pi)$ are determined from (4.1), while the base resistance can be expressed by the formula:

$$R_\pi(v_\pi) = \frac{\beta_0}{G_m(v_\pi)} = \frac{\beta_0 V_T}{I_{c,1}(v_\pi)} = R_{\pi,Q}\frac{I_{C,Q}}{I_{c,1}(v_\pi)} \tag{4.6}$$

where $I_{c,1}(v_\pi)$ is the first-harmonic of the BJT collector current and $G_m(v_\pi)$ is the large-signal transconductance of the active devices. By using the method outlined in [62], the following relationships are obtained:

$$C_{\pi,0}(V_\pi) = C_{\pi,Q}\, \mathbb{I}_0(V_\pi/V_T) \tag{4.7}$$

$$C_{\pi,2}(V_\pi) = C_{\pi,Q}\, \mathbb{I}_2(V_\pi/V_T) \tag{4.8}$$

$$R_\pi(V_\pi) = R_{\pi,Q}\, \mathbb{I}_1(V_\pi/V_T) \tag{4.9}$$

where $\mathbb{I}_\alpha$ is the modified Bessel function of the first kind and order α, $C_{\pi,Q}$ is the quiescent value of the base-emitter diffusion capacitance and $R_{\pi,Q}$ is the small-signal base-emitter resistance of the devices.

4.2.2 Output Impedance Contribution

The schematic for modeling the AM-PM distortion due to the output impedance is shown in Figure 4.3 where the output transformers steps down the antenna impedance into the resistance R_L. The collector current $i_C = I_C \cos(\omega_0 t)$ is

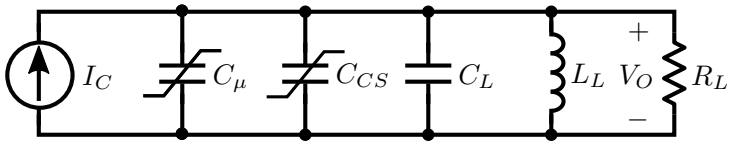


Figure 4.3: Output impedance equivalent model. The collector current is considered to be linear. The only phase variation from I_C to V_o is due to the output capacitance variation vs output voltage.

considered linear and the only phase non-linearity is due to the collector-substrate capacitance C_{CS} ad the collector-base capacitance C_μ. The Miller effect is neglected since the PA on which this model is based employs a cascode configuration (see Figure 3.17) and it is supposed that the common-base stage acts as an ideal current buffer.

Assuming abrupt junctions, the capacitances are given by:

$$C_\mu = \frac{C_{j\mu,0}}{\sqrt{1+\frac{V_{CB}}{\Phi_{jBC}}}} = \frac{C_{\mu,Q}}{\sqrt{1+\frac{v_o}{\Phi_{jBC}+V_{CB,Q}}}}, \tag{4.10}$$

$$C_{CS} = \frac{C_{jCS,0}}{\sqrt{1+\frac{V_{CS}}{\Phi_{jCS}}}} = \frac{C_{CS,Q}}{\sqrt{1+\frac{v_o}{\Phi_{jCS}+V_{CC}}}}. \tag{4.11}$$

For the sake of analysis we suppose: $V_{CB,Q} \approx V_{CC}$ and $\Phi_{jBC} \approx \Phi_{jCS}$. The parallel between C_μ and C_{CS} becomes:

$$C_o(v_o) = \frac{C_{o,Q}}{\sqrt{1+\frac{v_o}{\Phi_j+V_{CC}}}} \tag{4.12}$$

where $C_{o,Q} = C_{\mu,Q} + C_{CS,Q}$. If we now expand C_o using the Taylor series around $v_o \to 0$ we get: $C_o(v_o) = C_{o,Q} + C'_o v_o + C''_o v_o^2 + \cdots$, with $C_{o,Q}$ quiescent value of the BJT output capacitance and

$$C'_o = -\frac{C_{o,Q}}{2\left(\Phi_j + V_{CC}\right)}, \tag{4.13}$$

$$C''_o = \frac{3\,C_{o,Q}}{8\left(\Phi_j + V_{CC}\right)^2}. \tag{4.14}$$

Compared to Section 4.2.1, here we resort to the Taylor series instead of the Fourier series because, albeit more accurate, the closed-form Fourier series of (4.12) is too convoluted to give any design insights. Moreover at the output

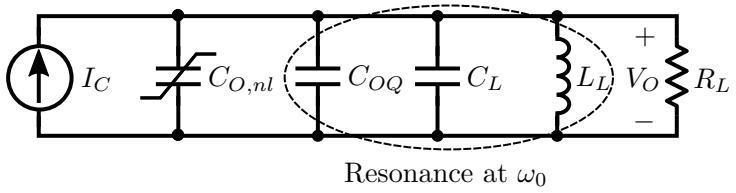


Figure 4.4: Simplified output model where C_o has been represented according to (4.15) as the sum of a linear capacitor $C_{o,Q}$ and a non-linear one $C_{o,nl}$.

there are less harmonics than at the input, thanks to the filtering action of the parallel resonant tank formed by $C_L + C_{o,Q}$ and L_L, so the approximation does not affect the final result significantly.

Once again $C_o(v_o) = \frac{dQ_{C_o}}{dv_o}$ so $dQ_{C_o} = C_o(v_o)\, dv_o$, then the current in the capacitor C_o is given by:

$$i_{C_o} = C_o(v_o)\frac{dv_o}{dt} = C_{o,Q}\frac{dv_o}{dt} + C_o' v_o \frac{dv_o}{dt} + C_o'' v_o^2 \frac{dv_o}{dt}. \tag{4.15}$$

This current can be divided into a linear part due to $C_{o,Q}$ and a non-linear part depending on the output voltage v_o, represented by $C_{o,nl}$ in Figure 4.4. By design, at the operating frequency ω_0, the small-signal BJT output capacitance $C_{o,Q}$ in parallel with the tuning capacitance C_L is resonated by the inductor L_L and appear as an open circuit.

Following the same approach as the input network analysis, we suppose $i_c(t) = I_C \cos(\omega_0 t)$ and $v_o(t) = V_o \cos(\omega_0 t + \phi_o)$. By applying Kirchhoff's laws to Figure 4.4 we get:

$$v_o(t) = R_L \left(i_c(t) - C_{o,nl}(v_o)\, \frac{dv_o}{dt} \right). \tag{4.16}$$

If we substitute the expressions for $v_o(t)$, $i_c(t)$ and $C_{o,nl}(v_o)$ from (4.15) and solve for the phase of $\cos(\omega_o t)$, the phase shift between $i_c(t)$ and $v_o(t)$ is:

$$\phi_o(V_o) = \arctan\left(\frac{4}{R_L \omega_0 C_o'' V_o^2} \right). \tag{4.17}$$

4.2.3 Model Comparison

The model is compared against the class J PA described in Section 3.2. According to (4.5) and (4.17) the phase shifts depend on the peak base-emitter and output voltages (respectively V_π and V_o) of the PA. Model parameters are reported in Table 4.1. They have been determined by means of an AC simulation on the circuit. The peak first-harmonic voltages V_π and V_o are obtained

ω_0	$R_{\pi,Q}$	$C_{\pi,Q}$	R_L	$C_{o,Q}$	Φ_j	V_{CC}
$2\pi 28\,\mathrm{GHz}$	$208\,\Omega$	$239\,\mathrm{fF}$	$20\,\Omega$	$209\,\mathrm{fF}$	$0.7\,\mathrm{V}$	$2\,\mathrm{V}$

Table 4.1: Model parameters values extracted from simulation.

from a swept-power simulation of the complete PA. The resulting variation from the small-signal value of ϕ_i and ϕ_o versus input power are reported in Figure 4.5. The figure shows that, according to this model, the dominant effect on the AM-PM distortion of a cascode SiGe PA at the onset of compression is due to the BJT input impedance variation with input (output) power.

Figure 4.6 shows the total phase shift $\phi = \phi_i + \phi_o$ from input to output. Up to $\mathrm{P_{1dB}}$ (corresponding to an input power of 2 dBm) there is good agreement between the predicted AM-PM distortion and the measurement which confirms the validity of the model. For larger values of the input (output) power the model, the simulation and the measurements begin to diverge. This is due to the fact that higher-order effects which have been neglected are beginning to dominate the phase behaviour of the PA.

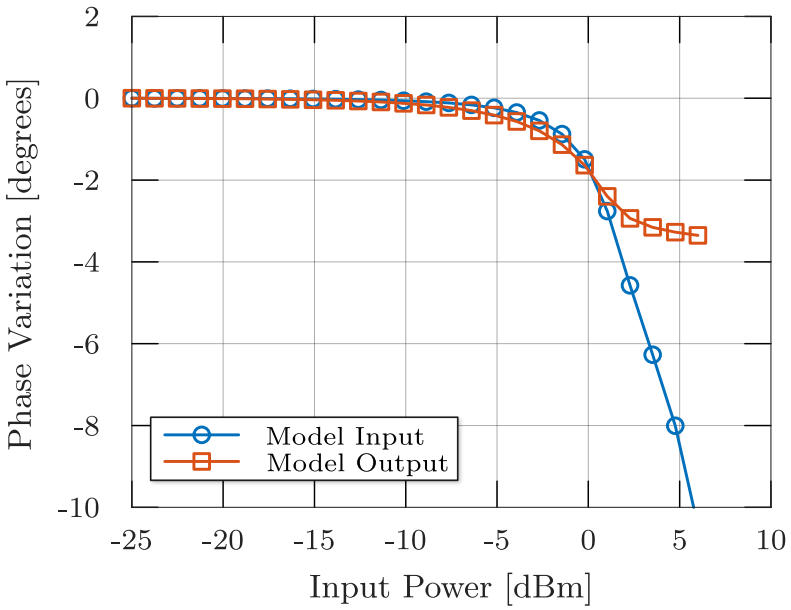


Figure 4.5: Phase variation ϕ_i (blue curve) and ϕ_o (red curve) versus PA input power. The dominant effect is due to the input impedance variation with P_{in}.

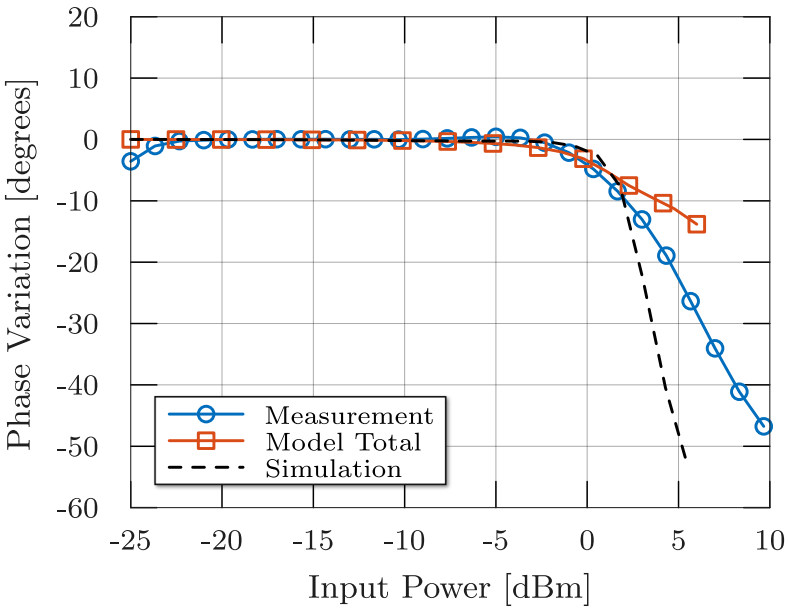


Figure 4.6: Total phase variation ϕ predicted by the model, compared with measurements and simulation. There is good agreement between model and measurement.

4.3 Ladder-Filter Input Matching Network

To desensitize the IMN from device impedance variations degrading AM-PM performance, this network has been designed using a doubly terminated LC ladder filter as a prototype [42]. Doubly terminated LC ladder filter topologies are highly desirable as they have very low sensitivities to component values: non-exact component values have a minimal effect on the realised transfer function [63]. Furthermore, high data rate digital communication schemes require accurate suppression of group delay variation within the filter passband. To satisfy this constraint a Bessel filter prototype has been used for the present design.

Bessel filters are able to pass wideband signals with a minimum of distortion [64]. They are optimized to obtain a maximally flat group delay or linear phase characteristic in the filter's passband. Selectivity or stop band attenuation is not a primary concern when dealing with the Bessel filter. Other filter prototypes, such as the Butterworth or Chebyschev filters, show a phase response which is extremely non linear over the filter's passband. This phase non-linearity results in distortion of wideband signals due to the varying time delays associated with the different spectral components of the signal.

The single-ended small-signal AC equivalent of the PA differential input network is shown in Figure 4.7. By transforming the parallel connection of $c_\pi/2$ and $2 \cdot r_\pi$ into its series equivalent, a two-section ladder filter topology is obtained with a shunt branch and a series branch. The series branch is formed by the input transformer leakage inductance $L_{is} \cdot (1 - k_{in}^2)$, the series-equivalent BJT input impedance, including the BJT base resistance R_B, and the external resistor R_A. This small resistor has been added to realize the correct resistive termination for the filter. The values of the series-equivalent of c_π and r_π have been estimated by transistor-level simulation yielding $c_{\pi,s} = 1.79\,pF$, $r_{\pi,s} = 4.35\,\Omega$ and $R_B = 1\,\Omega$.

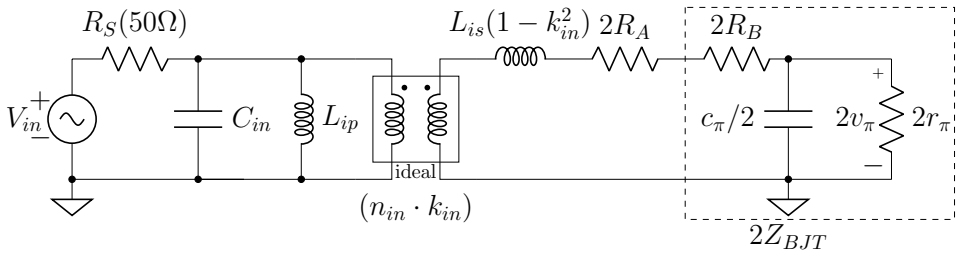


Figure 4.7: Input ladder matching network single-ended small-signal AC equivalent circuit. The equivalent small-signal BJT input impedance is shown inside the dashed box.

The transformer equivalent turns ratio helps in realizing the doubly terminated filter by transferring the series branch impedance to the primary side divided by $(n_{in} \cdot k_{in})^2$, where $n_{in} = \sqrt{L_{is}/L_{ip}}$. The transformer magnetizing inductance L_{ip}, together with the capacitor C_{in}, forms the parallel branch of the filter. The capacitance C_{in} also includes the parasitic capacitance of the RF input pads.

Starting from the usual low pass ladder filter prototype, center frequency and bandwidth have been chosen in order to obtain suitable component values. The goal is to minimize the number of additional passive components for the network and obtain good power match at the input within the desired operating band. Component values are shown in Table 4.2. Since input matching bandwidth is not a fixed design constraint (obviously the wider the better), such parameter can be tweaked to obtain a capacitance for the series branch which is the same as the value given by the transistor input impedance at the operating frequency.

In order to assess the effectiveness of the ladder-filter based IMN compared to the resonant IMN adopted in the reference design in reducing AM-PM distortion, small-signal ac and large-signal transient simulation have been performed on the IMN equivalent circuits and on the complete PA post-layout

C_{in}	L_{ip}	k_{in}	L_{is}	R_A
855 fF	296 pH	0.665	507 pH	7 Ω

Table 4.2: Ladder input matching network component values.

schematics, respectively, of the two PA's. First, small-signal ac simulations have been executed on the equivalent circuits of the ladder-filter based IMN, shown in Figure 4.7, and of the resonant IMN of the reference design, shown in Figure 4.8, to estimate the sensitivity of the signal phase to C_{BE} variation. A series of simulations with increasing values of c_π (i. e. , the small-signal value of C_{BE}) have been executed and the phase difference $\Phi_{in,1(2)}$ between $2v_\pi$ and V_{in} (see Figure 4.7 and 4.8) has been measured. Sub-index 1 and 2 refer to the present design and to the reference design, respectively. For better accuracy, the value of r_π was varied alongside that of c_π using the relationship $\omega_t = \beta/(r_\pi c_\pi)$. The resulting phase difference variation $\Delta\Phi_{in,1(2)}$ vs c_π is reported in Figure 4.9, showing that the ladder-filter (solid line) reduces the signal phase sensitivity to base-emitter capacitance variation with respect to the reference design (dashed line).

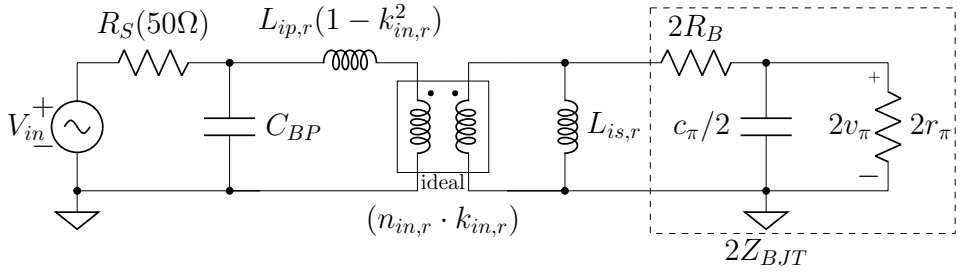


Figure 4.8: Single-ended small-signal AC equivalent input network for the reference design [36]. The small-signal BJT input impedance model is highlighted by the dashed box.

Then, large-signal transient simulations of the complete PA schematics (see Figure 3.3 and Figure 3 in [36]) with post-layout parasitic back-annotation have been executed at increasing input power levels. Considering the fundamental component of the voltage waveforms, in this case $\Phi_{in,1(2)}$ is re-defined as the phase difference between the common-emitter (CE) BJTs differential base voltage and V_{in}, and $\Phi_{tot,1(2)}$ is introduced as the phase difference between the load voltage V_{out} and V_{in}. The resulting phase difference variations $\Delta\Phi_{in,1(2)}$ and $\Delta\Phi_{tot,1(2)}$ vs P_{in} are reported in Figure 4.10. First, it should be noted that $\Delta\Phi_{in,1}$ is consistently lower than $\Delta\Phi_{in,1}$. Based on the results shown

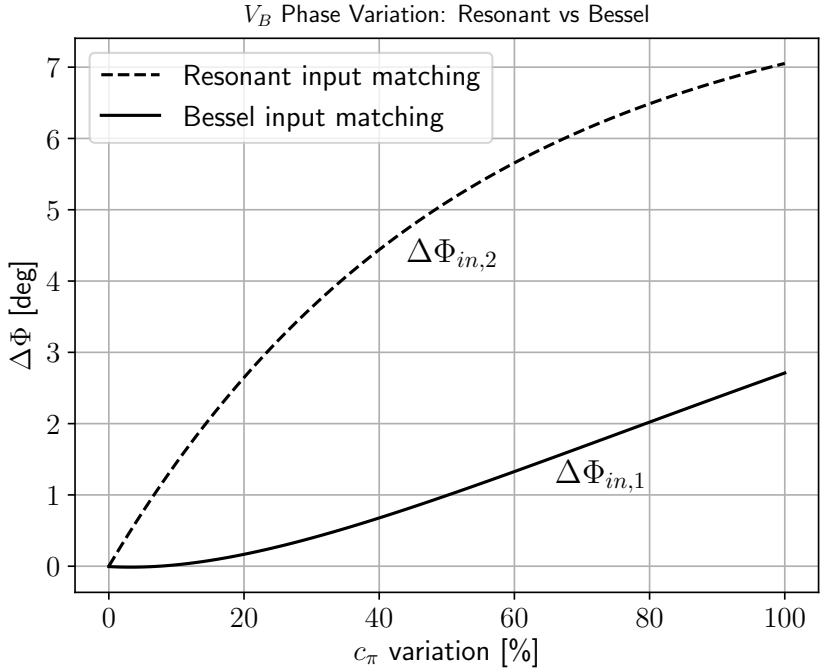


Figure 4.9: Theoretical phase difference variation at the input node for the old design employing a resonant matching network (index 2) and the new design with Bessel filter (index 1).

before in Figure 4.9, this improvement can be attributed to the ladder-filter based IMN introduced in the present design. Second, the present design is also expected to feature a lower AM-PM distortion than the reference design as $\Delta\Phi_{tot,1} < \Delta\Phi_{tot,2}$ when $P_{in} > -2$ dBm. Finally, it may also be noticed that the phase shift $\Delta\Phi_{tot,1(2)} - \Delta\Phi_{in,1(2)}$ between the common-emitter BJTs differential base voltage and V_{out} is positive in the present design and lower in absolute terms than in the reference design. This is mainly a consequence of the usage MIM capacitors vs pn-junction varactors in the OMN of the present design and of the reference design, respectively.

4.3.1 Measurement Results

Figure 4.11 shows the chip microphotograph. The complete MMIC measures 1050 µm × 1450 µm (1.4 mm^2) and its active area is roughly 600 µm × 450 µm (0.27 mm^2) including the transformers. The PA is implemented in Infineon 0.35 µm SiGe technology. This technology is optimized for RF applications and features bipolar transistors with $f_T = 200\,GHz$ [44].

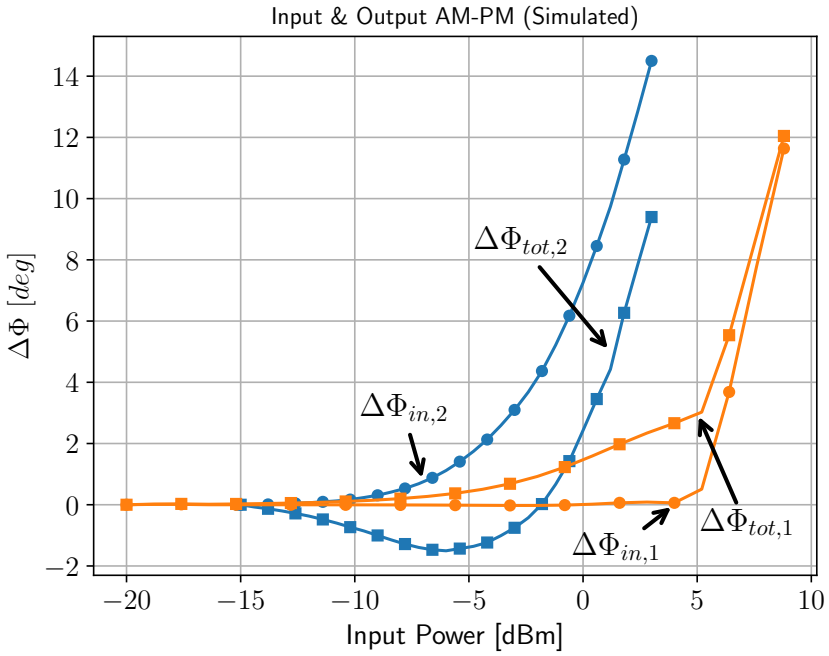


Figure 4.10: Post layout simulation of first harmonic phase difference variation after the matching network (transistor base) $\Delta\Phi_{in,1(2)}$ and at the output node of the PA $\Delta\Phi_{tot,1(2)}$ with respect to the input voltage V_{in}. The index 1 and 2 refer to the current design and the reference design respectively.

The measured small signal S-parameters are shown in Figure 4.12. The solid line is the measurement whereas the dashed line is the simulation. The implementation shows slightly higher gain and bandwidth than simulation due to overestimation of circuit parasitics. Peak gain is 15 dB at 10 GHz and the −3 dB bandwidth spans the entire X-Band (8 GHz to 12 GHz). Moreover the PA achieves good input return loss in the operating band.

The measured stability factor K is plotted in Figure 4.13. The minimum value is 3.8 at 7.5 GHz which confirms that the amplifier is unconditionally stable.

In figure 4.14 the group delay versus frequency is shown. Due to the Bessel filter topology employed in-band phase variation and thus group delay is small. This work has shown a measured group delay of 101 ps ± 2.5 % in the whole X-band.

Using a ladder filter based input matching network improves also the large signal performance of the PA. Figure 4.15 shows a comparison between the reference class J design [36] presented in Section 3.1 and the new design [42].

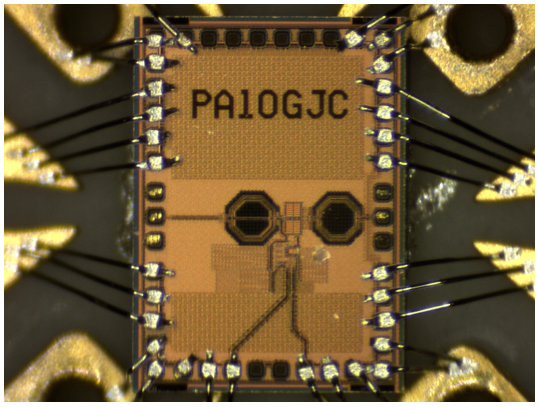


Figure 4.11: IC photograph.

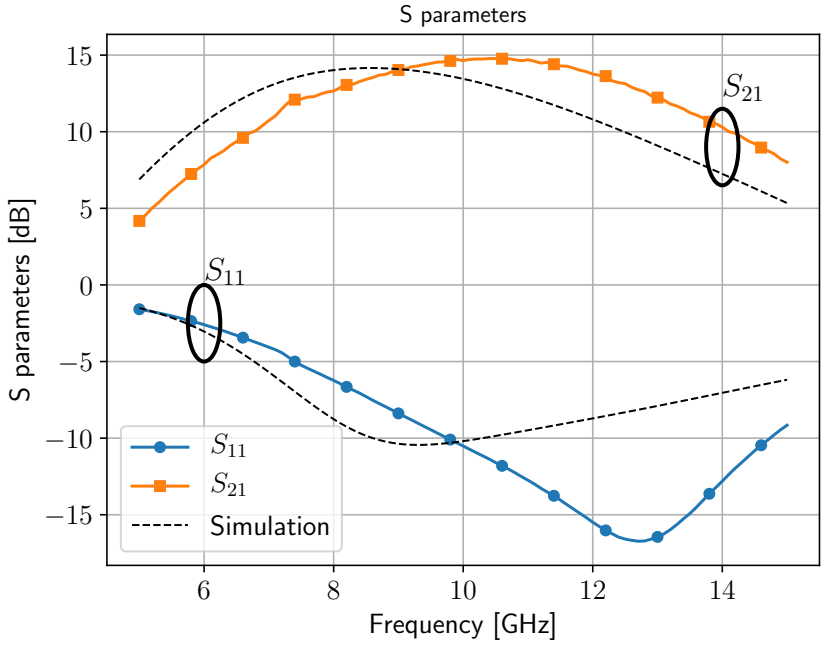


Figure 4.12: Measured (solid lines) and simulated (dashed lines) S_{11} and S_{21}.

Albeit the reduction in gain, which is due to the input filter insertion loss, P_{sat} is not affected and the output P_{1dB} is brought closer to it.

Both amplifiers have P_{sat} 22 dBm. The reference amplifier had an input P_{1dB} of −2 dBm which resulted in an output power of 16 dBm. On the other hand the new design has an input P_{1dB} of 5 dBm and output P_{1dB} of 19 dBm, a 3 dB improvement on the previous solution.

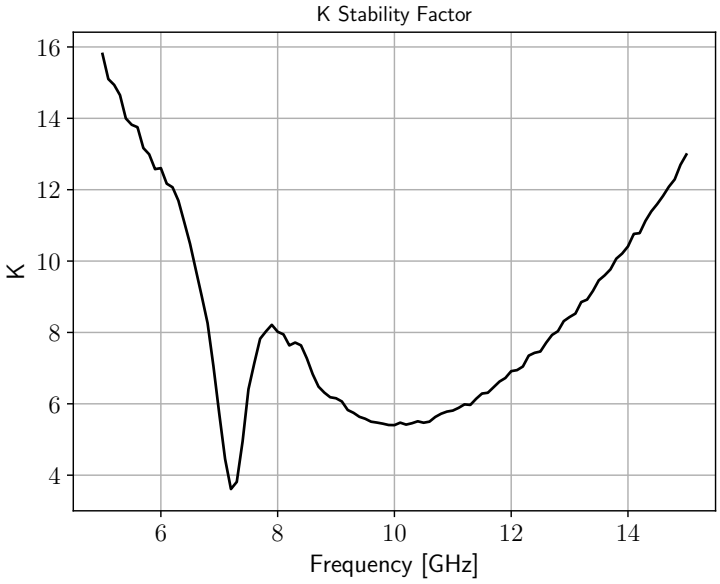


Figure 4.13: Measured stability K factor.

Power added efficiency versus output power is shown in Figure 4.16. Despite the small reduction of peak PAE in saturation, which in the current version is 33 % and in the previous one was 36 %, having the P_{1dB} and P_{sat} closer together reduces the amount of back off needed to obtain the same performance. This results in better efficiency with modulated signals, especially when the PAPR is high.

Figure 4.17 compares the AM-PM distortion of the current and previous solutions. On the x-axis the output power, normalized to the compression point of each amplifier has been used. This has been done in order to show the amount of back off needed by each amplifier in order to obtain a certain maximum phase variation. Thanks to the usage of MIM capacitors at the output node and a Bessel ladder filter matching at the input, a five fold decrease of phase variation at compression point, compared to the previous design, has been obtained.

4.3.2 Conclusion

The design of an efficient, distortion-aware, class J power amplifier suitable for high spectral efficiency communications applications in the X-band was presented. Taking as a reference a class J PA originally designed for radar applications, the work singled-out the main sources of AM-PM distortion in the sensitivity of the input and output matching networks to the active devices

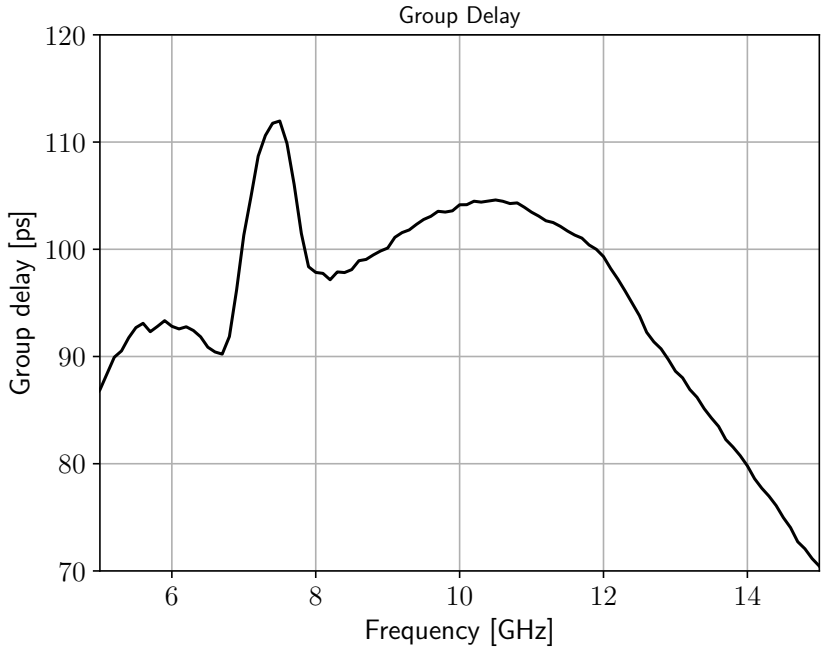


Figure 4.14: Measured group delay versus frequency.

parasitic capacitance variation at high power levels. The trade-off between efficiency and precision of the second harmonics termination offered by class J was used to reduce the fraction of output capacitance due to nonlinear transistor parasitics. A Bessel bandpass ladder filter was chosen to realize an IMN that simultaneously achieves low sensitivity to BJT input capacitance variation and almost constant group delay vs frequency.

The resulting design has been fabricated using the 0.35 µm SiGe process from Infineon technologies and results in an active area of 0.27 mm^2. The new PA shares the same P_{sat} as the previous design (22 dBm). The output P_{1dB} is brought closer to saturation (19 dBm instead of 16 dBm). Moreover the current work shows group delay and AM-PM distortion performance which are better suited to high data rate communication applications which employ modulation schemes with high spectral efficiency. The price to pay for such improvement is a small reduction in the peak PAE which is now 33 % instead of 36 %. The gain is also reduced:15 dB instead of 20 dB in the reference design.

All measured result are summarized in Table 4.3. In such table the current PA is compared to the previous one and with the state of the art. All measurements show good agreement with simulations and compete well with other works on the same topic, especially in terms of efficiency, output power and AM-PM.

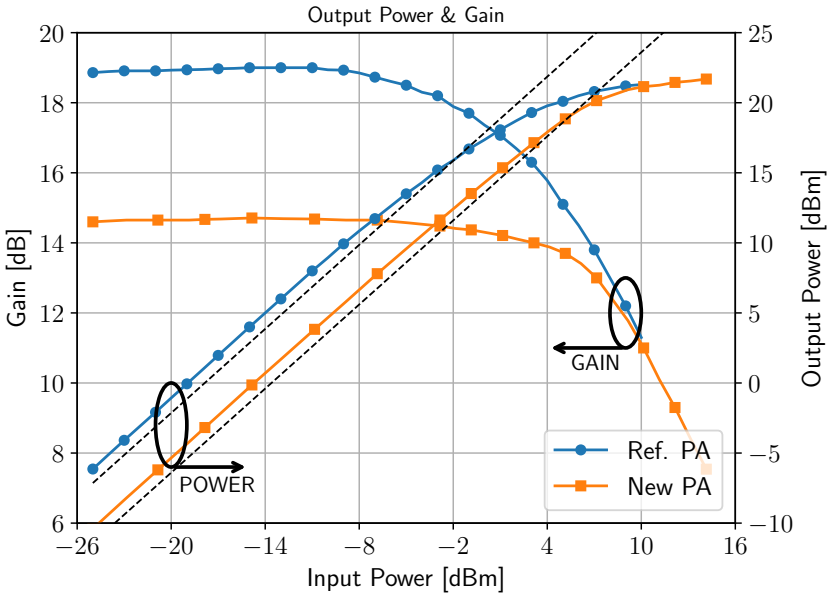


Figure 4.15: Measured output power and gain of the reference PA (circles) and of the new PA (squares).

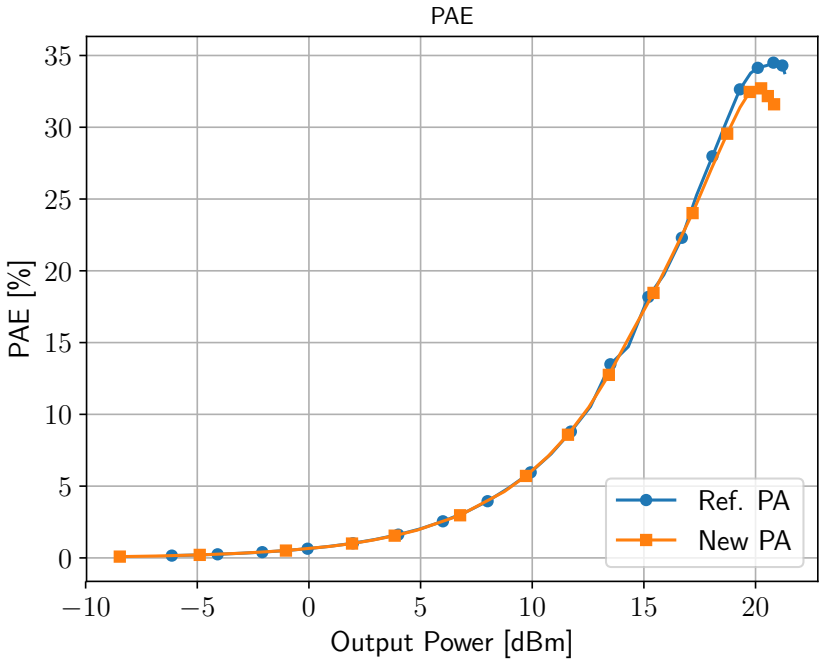


Figure 4.16: Measured PAE of the reference PA (circles) and of the new PA (squares).

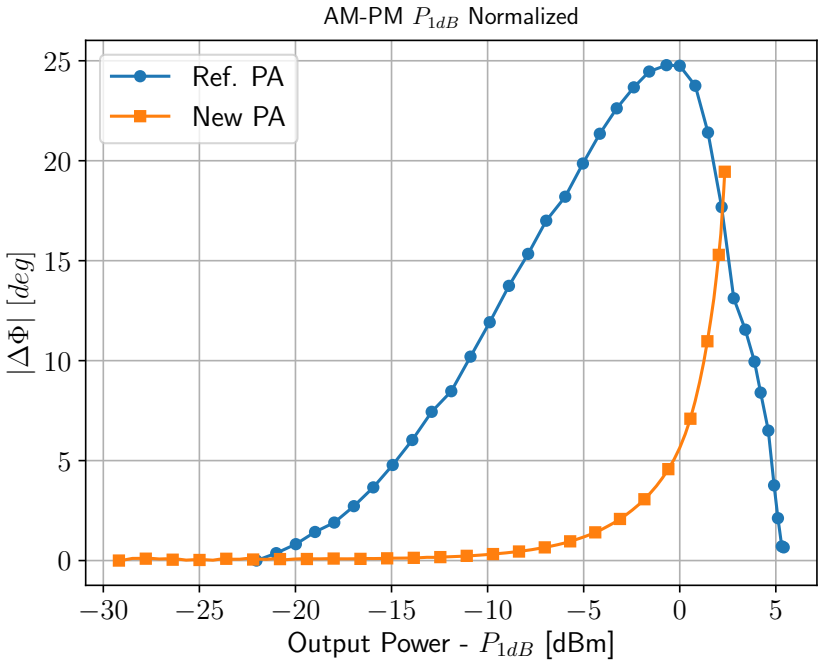


Figure 4.17: AM-PM distortion obtained by measuring the phase of S_{21}. On the x-axis the output power is normalized to the P_{1dB}.

	This work	[38]	[65] (PA only)	[48]	[66]
Technology	$0.35\mu m$ SiGe	$0.35\mu m$ SiGe	$130nm$ CMOS	$180nm$ SiGe	$180nm$ CMOS
Freq. [GHz]	10	12.1	9.5	8.8	9.5
B_{3dB} [GHz]	4	2	3	3	6.5
Gain [dB]	15	21.1	17	21	25
P_{sat} [dBm]	22	23.4	15.5	27	21.5
P_{1dB} [dBm]	19	22	11	25	20
P_{1dB} AM-PM [deg]	5	–	5	–	–
PAE [%]	33	37.3	19	36	20
V_{CC} [V]	2	1.8	3	3.5	3.6
Area [mm^2]	1.4	1.7	–	1.0	0.63

Table 4.3: Summary and comparison of the current work with the state of the art.

4.4 Two-stage CMOS-SiGe PA

As already discussed in the previous section, one of the main AM-PM distortion sources in PAs is the input impedance variation with input power [42, 57, 67]. This issue can be mitigated by exploiting the complementary nature of MOS transistors. As first suggested in [57], by combining pMOS and nMOS devices in the input stage this variation can be minimized. In the design discussed in this section, to reduce AM-PM distortion a hybrid CMOS-BJT two-stage topology with an interstage matching network implemented as a doubly-tuned, magnetic transformer. A class A, CMOS predriver reduces the contribution to AM-PM distortion of the nonlinear gate capacitance of the devices at the PA input by exploiting the complementary behavior of nMOS and pMOS transistors, while a class J, common-base (CB) second stage guarantees the desired output power over a large bandwidth with high drain efficiency.

The interstage matching network can be designed to add current gain between the first and the second stage mitigating the impact of the predriver power consumption on the PAE, reducing at the same time the size of the MOS devices with an additional beneficial effect on AM-PM distortion thanks to lower parasitic capacitances. Starting from [68], the network is designed to feature a single resonance in order to obtain a good trade-off between current gain and power losses due to the finite quality factor of the transformer coils. The validity of the approach is assessed through the design of a PA for mmWave 5G applications in the operating band n257 of the 5G standard (from 26.5 GHz to 29.5 GHz) [50]. The proposed circuit is designed using Infineon's 130 nm BiCMOS SiGe process [69].

4.4.1 Output Stage Design

With reference to Figure 4.18 the output stage is implemented by a CB topology which, compared with the CE solution, shows an higher breakdown voltage [70]. The circuit behaves, in the current domain, as a diode voltage clamper. This way the bias current in the output BJTs varies with the envelope of the input, similar to an ideal class B CE stage, but without compromising gain [71]. Moreover the output matching network is designed to obtain class J operation, as the other PAs presented in this thesis, following the same methodology outlined in [36, 42] and in Section 3.1.2 of this thesis. Given that the target operating frequency is the same, the OMN is the same as the 28 GHz class J PA reported in Section 3.2.

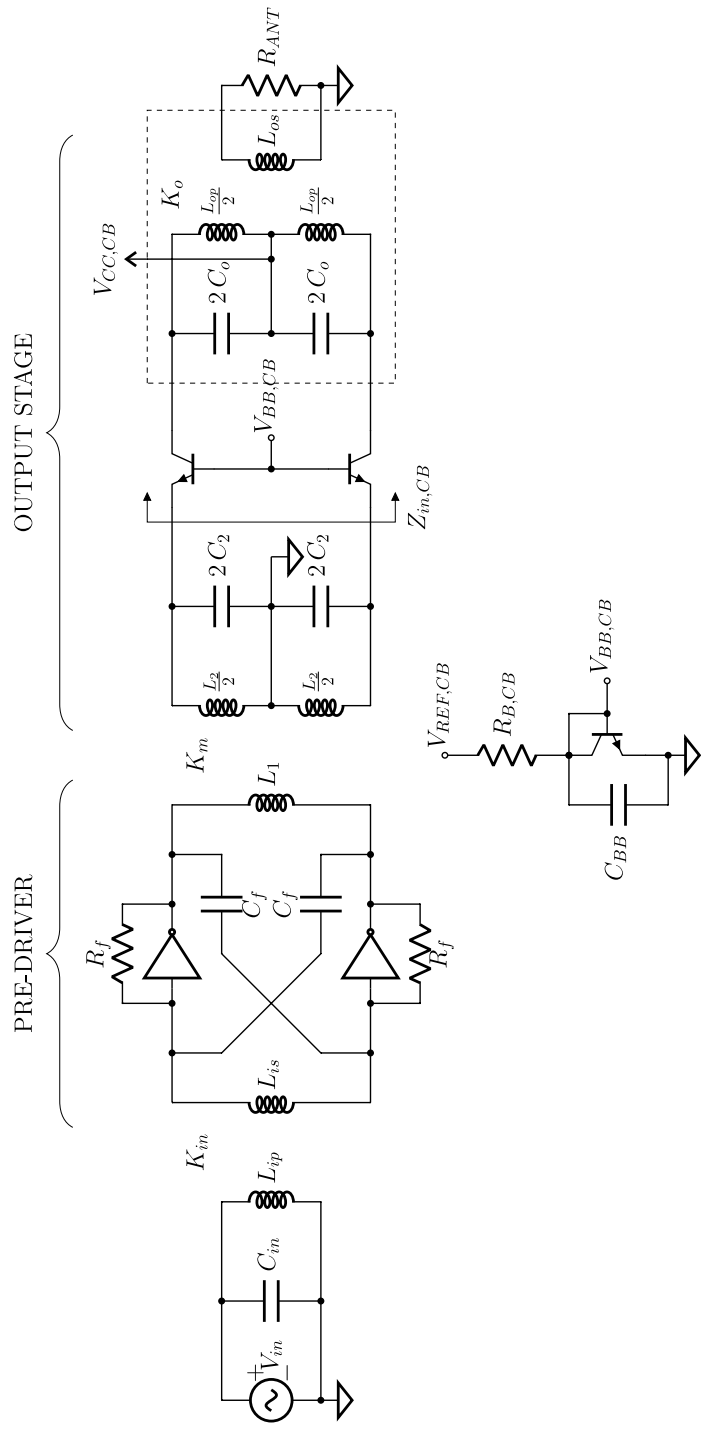


Figure 4.18: Simplified schematic of the two-stage hybrid BiCMOS PA.

4.4.2 Predriver and Interstage Matching Design

In the PA described in Section 3.2, a CE stage was coupled to a CB stage in a cascode fashion and the main contribution to the AM-PM distortion was due to the driver transistors. In this design (Figure 4.18), in order to minimize the AM-PM distortion, the input stage is realized with CMOS inverters, where the complementary dependence of pMOS and nMOS gate capacitance on input voltage lowers the contribution of the predriver to overall AM-PM distortion [57]. Furthermore, the predriver inverters are self-biased in class A by means of the resistors R_f, thus trading PAE for increased linearity. In order to achieve an acceptable trade-off between linearity and PAE, the interstage matching network is then designed to provide current gain.

The predriver IMN is designed with an input transformer that works as a balun for the input signal and provides the required impedance transformation to match the PA to the source in the operating band. Explicit MIM neutralization capacitors C_f improve the stability of the circuit [72]. Transistor sizing is dictated by the maximum current required to drive the CB output stage in order to achieve the desired P_{sat} value. Since the CB output stage acts as a current buffer, then, designing an interstage matching network to step-up the input impedance $Z_{in,CB}$ of the CB stage, reduces the predriver current, with a beneficial effect on PAE and, consequently, on the size of the pMOS and nMOS transistors in the inverters, thus lowering layout parasitics.

To meet this goal, the interstage matching network has been designed using a doubly-tuned, magnetic transformer [68]. The schematic of the network is shown in Figure 4.19, where R_1 and R_2 are the equivalent loss resistances of the transformer coils, and k is the transformer magnetic coupling coefficient. $Z_{in,CB} = R_{in,CB} + jX_{in,CB}$ is the CB input impedance, extracted from simulation, C_1 and C_2 are the shunt capacitors for the transformer primary and secondary inductances L_1 and L_2, respectively. The impedance $Z_{in,CB}$ is transformed by the network into Z_{in}.

As discussed in [68], under proper assumptions, it can be shown that Z_{in} peaks at $\omega_{S_{II}} = 1/\sqrt{C_1 L_1 (1-k^2)}$ and that the secondary side of the interstage matching network can be approximated as an equivalent series tank, whose loss resistance is

$$R_{eq,S_{II}} = R_2 \frac{k^2 + Q_2/Q_1}{k^2}. \tag{4.18}$$

Then, the peak value of Z_{in} can be written as

$$Z_{in}(\omega_{S_{II}}) = \frac{Z_{II}^2}{Z_{in,CB} + R_{eq,S_{II}}} \tag{4.19}$$

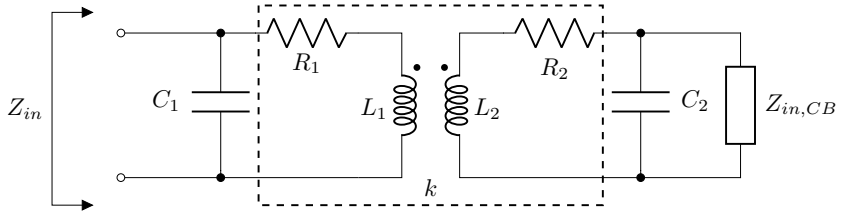


Figure 4.19: Schematic of the doubly-tuned interstage matching network. The equivalent model of the integrated transformer is enclosed in the dashed square, turns ratio is $n = \sqrt{L_2/L_1}$.

where Z_{II} (corresponding to K_{II} in [68]) is given by

$$Z_{II} = \omega_{S_{II}} L_2 \cdot \frac{(1-k^2)}{n \cdot k} \tag{4.20}$$

showing that, around $\omega_{S_{II}}$, the doubly-tuned transformer can be modeled as an impedance inverter with a scaling factor given by Z_{II}. The value of Z_{II} can then be set to achieve the desired interstage matching network current gain:

$$G_i = \sqrt{\frac{Z_{in}}{Z_{in,CB} + R_{eq,S_{II}}}} = \frac{Z_{II}}{Z_{in,CB} + R_{eq,S_{II}}}. \tag{4.21}$$

Based on the equations above, and considering that the loss resistance $R_{eq,S_{II}}$ is proportional to the transformer turns ratio $n = \sqrt{L_2/L_1}$ and decreases with k [68], $\omega_{S_{II}}$ is set to 28 GHz by realizing C_1 only through the parasitic capacitance at the interstage matching network primary port (466 fF as extracted from the layout), thus maximizing the value of L_1 (93 pH).

The effect of the interstage matching network current gain G_i on PAE, output power and AM-PM distortion has been estimated by harmonic balance, large-signal simulation of the transistor-level PA schematic with a lumped model of the interstage matching network transformer, assuming a constant quality factor $Q = 15$ for both inductors L_1 and L_2. The quiescent current of the predriver and of the second stage are set to 14 mA and 22.2 mA, respectively.

The value of L_2 has been varied from 13 pH to 108 pH, while the coupling factor was kept fixed at $k = 0.68$, the value extracted from EM simulations of the transformer with $L_2 = 54$ pH. Correspondingly, the value of G_i derived from (4.18), (4.20) and (4.21) ranges from about 1 to 1.7. Figure 4.20 reports the simulated PAE at P_{sat}, P_{1dB} and AM-PM distortion against G_i. The analysis of the voltage and current waveforms at the interstage matching network input port (not shown) demonstrates that the onset of PA gain compression occurs in the predriver and that, close to the P_{1dB}, the predriver moves from class

k_o	C_1	L_1	C_2	L_2
0.5	466 fF	93 pH	180 fF	54 pH

Table 4.4: Interstage matching network component values.

A towards class AB operation. Then, the almost constant value of P_{1dB} and the slight increase of PAE when G_i is increased from 1 to roughly 1.6, can be explained by the growth of Z_{in}, reducing the predriver output current value required to reach P_{1dB}, while the second stage input current, thanks to the increasing value of G_i, is roughly constant.

When G_i exceeds 1.6, Z_{in} becomes comparable to the predriver output impedance, causing the fraction of predriver current coupled into the interstage matching network primary port to decreases significantly, resulting in a drop of the output P_{1dB} and PAE. The AM-PM distortion at P_{1dB}, as discussed in Section 4.4.3, is mainly due to the nonlinear capacitance at the predriver input and, thus, it is not significantly affected by G_i. Based on these results, L_2 was set to 54 pH, corresponding to a nominal $G_i = 1.64$. The value of the matching network components is summarized in Table 4.4.

To further assess the effects of the interstage matching network on the linearity performance of the amplifier, an EVM simulation on the PA X-parameters, extracted by simulating the extracted view of the IC, has been performed. As a typical 5G modulation scheme, 256-QAM 400 MHz bandwidth test signal has been used. The results are reported in Figure 4.21, showing EVM as a percentage versus average output power which is less than 3 % up to 6 dB backoff from P_{1dB}.

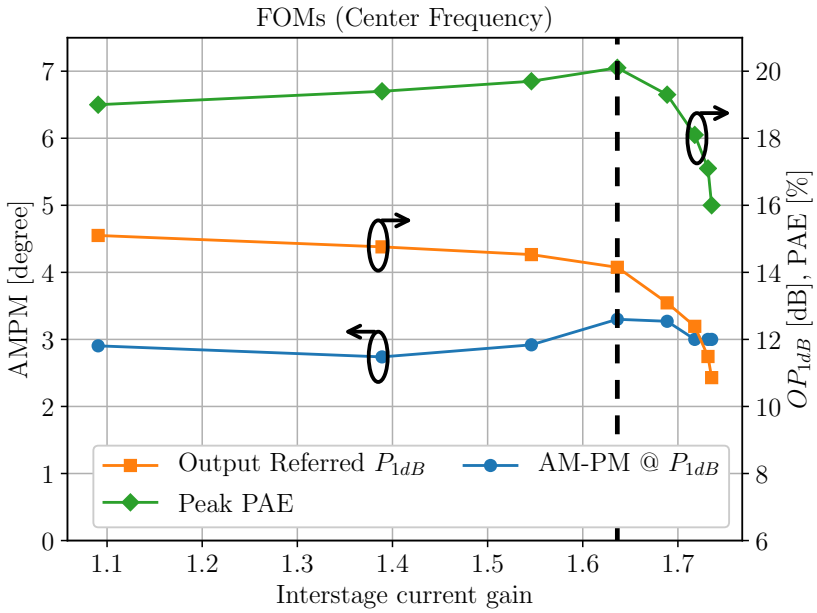


Figure 4.20: Effect of different interstage current gain values on PAE, AM-PM distortion and output P_{1dB}. The dashed line marks the chosen design value, granting maximum PAE.

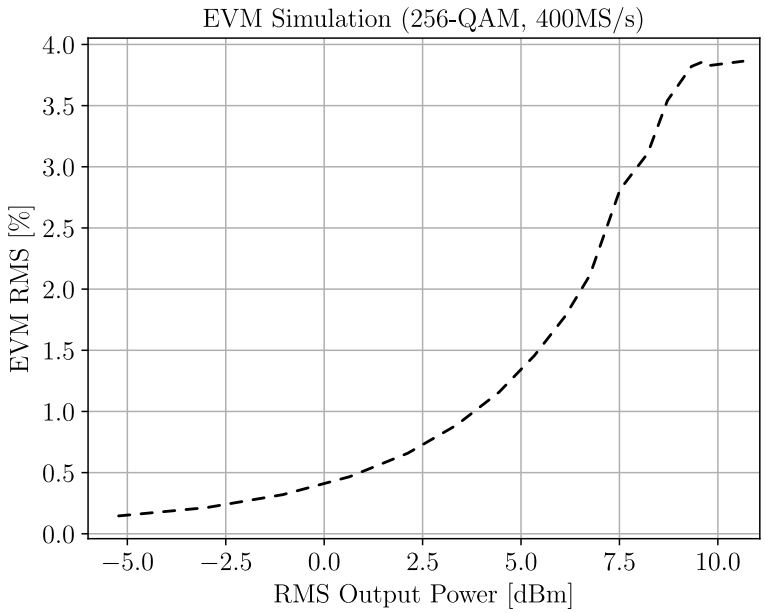


Figure 4.21: Simulated EVM versus average output power for the hybrid BiCMOS PA, obtained by extracting the PA X-parameters.

4.4.3 Measurement Results

Figure 4.22 shows the chip microphotograph of the PA. The design is implemented in Infineon's 130 nm SiGe technology. The complete IC measures 930 µm × 930 µm (0.864 mm^2) with an active area of 390 µm × 340 µm (0.133 mm^2), including the transformers. The chip has been measured by means of on-wafer microwave probing.

The measured (solid line) and simulated (dashed line) small signal S-parameters are reported in Fig. 4.23. The peak gain (S_{21}) is 11 dB as predicted by simulation, though at 26 GHz instead of 28 GHz. This shift towards lower frequency is due to the underestimation of layout parasitics and causes the −1 dB bandwidth (from 24 GHz to 28.5 GHz) to cover the 5G standard operating range n258 (from 24.25 GHz to 27.5 GHz) instead of n257 [50]. The −3 dB bandwidth goes from 22 GHz to 32 GHz and the input return loss is good in the whole operating band. The stability factor K, resulting from the S-parameters, is always greater than one and the minimum value is around 10 at 25 GHz (see Figure 4.24) so the circuit is unconditionally stable for any source or load impedance.

Figure 4.25 plots the measured and simulated output power (dashed line and blue curve respectively), gain (orange curve) and PAE (green curve) versus input power. The proposed PA features a saturated output power of 16 dBm, it shows no sign of gain expansion and has an input P_{1dB} of 4 dBm and output P_{1dB} of 14 dBm. When the output power is saturated the PA shows 20 % peak PAE, at P_{1dB} the PAE is still near the peak at 19 %. At 6 dB back-off (P_{OUT} = 8 dBm) the PAE is 7.5 %.

Figure 4.26 plots the simulated and measured phase difference from the small signal value versus input power. The plot shows a phase variation as low as $\leq 1.5°$ with the input power varying from small signal up to saturation. The simulation shows that the AM-PM contribution of the CMOS predriver is significantly smaller than that of a CE BJT pair [42] and comparable in magnitude but opposite in sign with respect to that due to the CB output stage.

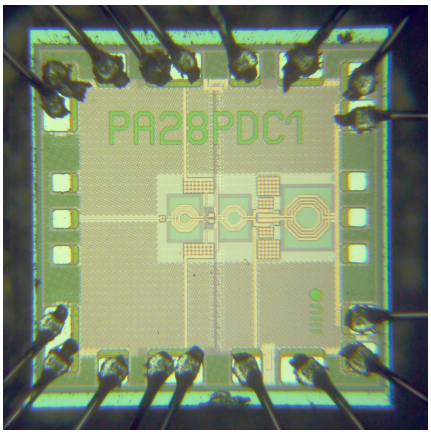


Figure 4.22: IC photograph. Die area is 930 µm × 930 µm, active area is 390 µm × 340 µm.

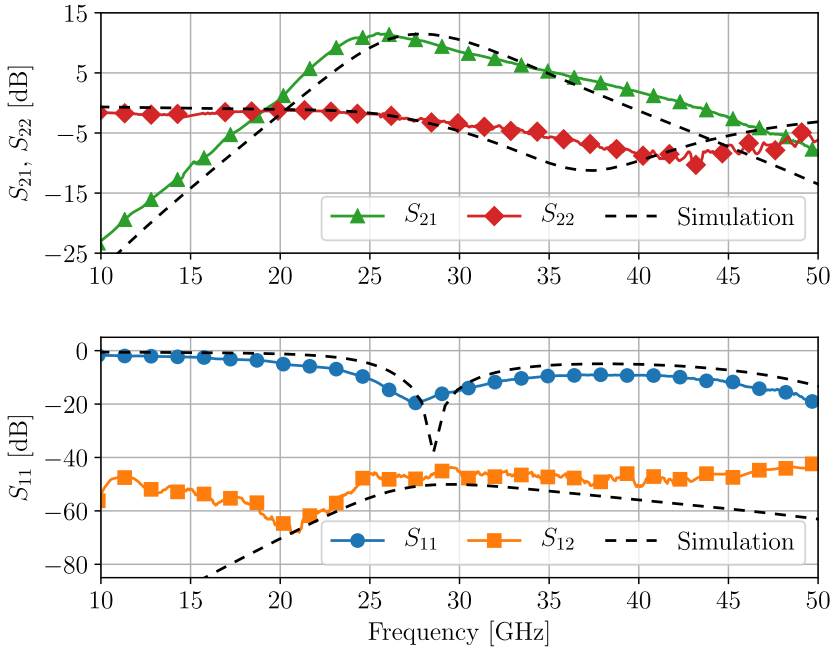


Figure 4.23: Measured (solid lines) and simulated (dashed lines) S-parameters of the prototype PA.

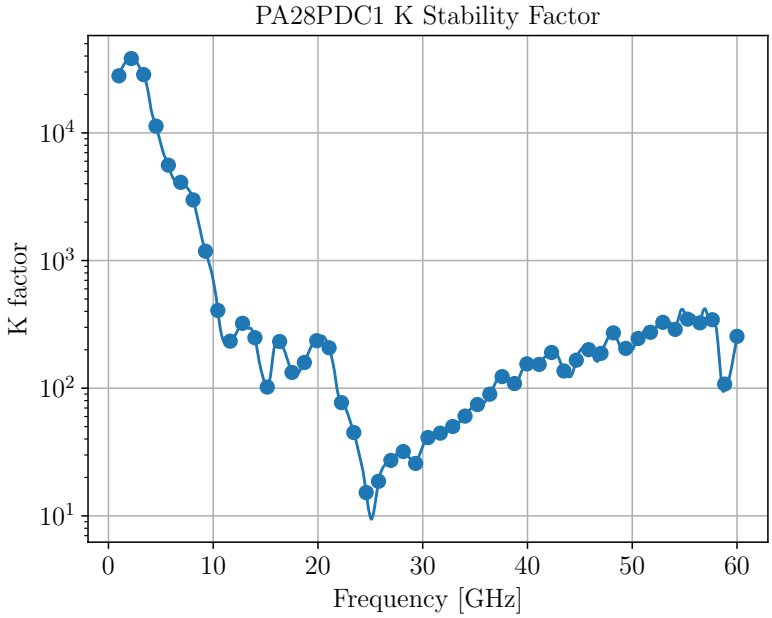


Figure 4.24: Measured stability K factor of the amplifier. Its minimum value is 10 at 26 GHz, so the circuit is unconditionally stable.

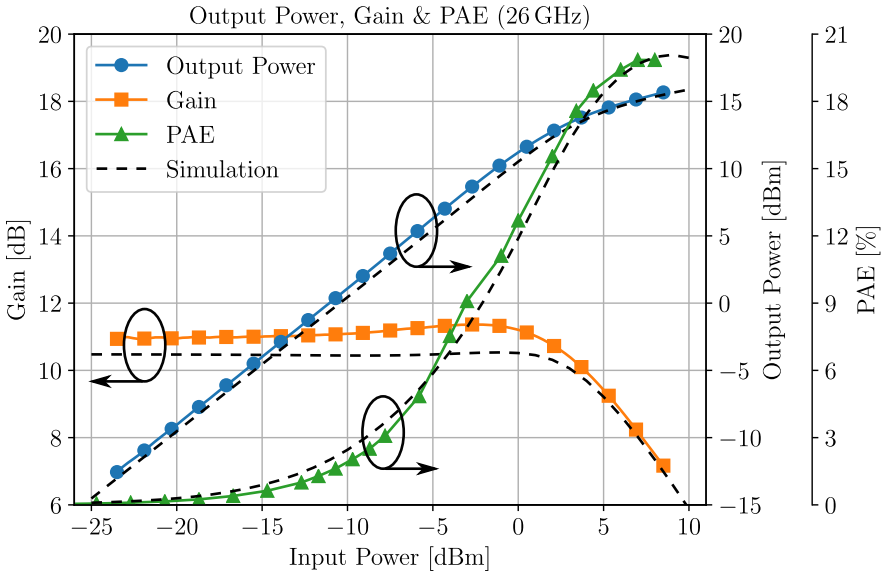


Figure 4.25: Measured output power (blue circles), gain (orange squares) and PAE (green triangles) of the PA, compared with simulations (dashed curves).

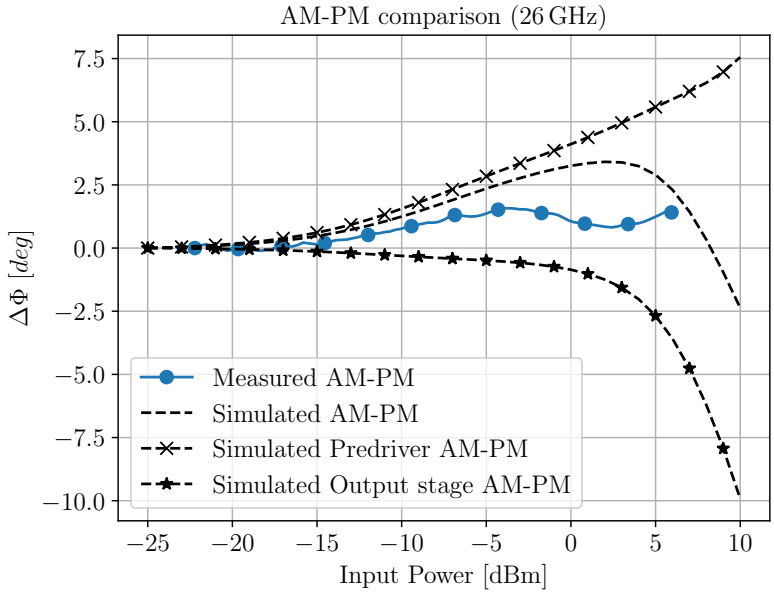


Figure 4.26: Measured and simulated AM-PM vs input power highlighting the contribution of the output and driver stages to the overall distortion.

4.4.4 Conclusion

In this section a hybrid CMOS-BJT, two-stage PA architecture was presented. This work leverages the properties of an interstage matching network based on a doubly-tuned, magnetic transformer designed to feature a single (series) resonance, to connect a highly linear CMOS predriver stage to an efficient, wideband class-J BJT output stage: the matching network allows to control the impact of the predriver on the PAE. The prototype has been realized using Infineon's 130 nm BiCMOS technology. It achieves very low AM-PM distortion ($\leq 1.5°$ over the whole output power range). The saturated output power is 16 dBm and the output P_{1dB} is 14 dBm. The peak small-signal gain is 11 dB at 26 GHz while the maximum PAE is 20 %. Overall, the proposed PA compares well with the state of the art (summarized in Table 4.5) and promises significant PAE improvement margins with more scaled BiCMOS processes.

	This work	[73]	[74]	[75]
Technology	130 nm SiGe	130 nm SiGe	28 nm CMOS	130 nm SiGe
Topology	two stage	doherty	doherty	single stage
Freq. [GHz]	26	28	32	28
B_{3dB} [GHz]	10	16.4	6	16
Gain [dB]	11	18	22	15.3
P_{sat} [dBm]	16	16.8	19.8	18.6
$P_{1dB,out}$ [dBm]	14	15.2	16	15.5
AM-PM @ P_{1dB} [deg]	1.5	10	1.5	2
PAE [%]	20	20.3	21	35
PAE @ PBO [%]	7.5 (-6 dB)	14 (-5.9 dB)	12 (-5 dB)	11 (-6 dB)
Supply voltage [V]	1.2/1.8	1.2/1.5	1	3.6
Active area [mm^2]	0.125	1.755	0.59	0.445

Table 4.5: Summary and comparison of this work performance with the state of the art.

Chapter 5

Conclusion

In this thesis, the main sources of AM-PM and AM-AM distortion in fully-integrated class J PAs have been pinpointed and circuit solutions to minimize their effect on the output signal have been proposed.

First of all, two reference class J amplifiers targeting 22 dBm saturated output power have been designed. The first one is targeted at X-band phased array radar applications at 10 GHz and the second one is targeted at 5G applications at 28 GHz. Class J is a variation on class B where, by appropriately designing the load terminations at the first and second harmonics of the amplifier, the maximum class B efficiency can be obtained with a more feasible OMN. The proposed class J OMN is based on an integrated transformer that works as a balun and performs impedance step-down from the nominal antenna load of 50 Ω. It is also discussed how the network is able to cancel out and exploit the parasitic output capacitance of the transistor in order to improve the theoretical efficiency of the PA. To verify the effectiveness of such output network in improving the efficiency, the 10 GHz class J PA is compared against a class B design targeting the same application. It has been shown that, by using the proposed class J OMN, the efficiency is raised from 31 % to 36 %. Also the 28 GHz 5G PA has shown a state-of-the-art 36 % peak PAE.

Taking as a reference the two previously described PAs, the main sources of AM-PM distortion have been singled out in the sensitivity of the input and output matching networks to the active devices parasitic capacitance variation at high power levels. Theory and simulations, developed throughout the thesis have shown that, of the two, the main contribution to AM-PM distortion is due to the BJT input impedance variation versus input power.

In the case of the X-band PA for radar applications, a variation on the design has been proposed in order to make the design suitable for high data rate communication. The trade-off between efficiency and precision of the second harmonics termination offered by class J was used to reduce the fraction of

output capacitance due to nonlinear transistor parasitics thus reducing the sensitivity of the OMN to parasitic capacitance variation. A Bessel bandpass ladder filter was chosen as a prototype to realize an IMN that simultaneously achieves low sensitivity to BJT input capacitance variation and almost constant group delay vs frequency in the operating band.

The resulting design has been fabricated using the 0.35 µm SiGe process from Infineon technologies and results in an active area of 0.27 mm^2. The new PA shares the same saturated output power as the previous design (22 dBm). The output P_{1dB} is brought closer to saturation (19 dBm instead of 16 dBm. Moreover the new design shows group delay and AM-PM distortion performance which are better suited to high data rate communication applications which employ modulation schemes with high spectral efficiency. The price to pay for such improvement is a small reduction in the peak PAE which is now 33 % instead of 36 %. The gain is also reduced: 15 dB instead of 20 dB in the reference design.

The dominant effect of input impedance variation on AM-PM is well known in the literature and solutions have been proposed especially for CMOS designs. Wang et.al. [57] have proposed a compensation technique for CMOS PAs that ensures very high linearity and low phase distortion. The method involves placing a pMOS device alongside the nMOS device that works as the amplifying unit, such that the overall capacitance seen at the amplifier input is a constant, thus improving linearity.

Using Wang's work as a starting point, another solution to minimize the impact of the input impedance variation with PA drive has been proposed. By leveraging the availability of both CMOS devices and bipolar devices in the SiGe thechnology, a two-stage hybrid BiCMOS PA design is described. The amplifier combines the best linearity and complementary fashion of the CMOS technology with the high output power and efficiency of bipolar transistors. This PA employs self-biased CMOS inverters as pre-drivers for a common-base bipolar output stage. To minimize the impact of the pre-driver on the overall efficiency of the amplifier, the work leverages the properties of an interstage matching network based on a doubly-tuned, magnetic transformer designed to feature a single (series) resonance that provides current gain between the two stages. This solution allows for a smaller first stage that consumes less power compared to an interstage matching network providing no gain. Moreover the effect of this network on PAE, P_{sat} and AM-PM distortion is analyzed in detail and the sweet-spot for efficiency was chosen.

Based on the above assumptions, a PA prototype has been fabricated using Infineon's 130 nm BiCMOS technology. The prototype achieves very low AM-PM distortion ($\leq 1.5°$ over the whole output power range). The saturated

output power is 16 dBm and the output P_{1dB} is 14 dBm. The peak small-signal gain is 11 dB at 26 GHz. The prototype maximum PAE is 20 %. Overall, the proposed PA compares well with the state of the art. Albeit effective in reducing AM-PM and AM-AM distortion, parasitics within the CMOS pre-driver degrade the overall gain and efficiency of the design. Therefore, this technique promises significant PAE improvement margins with more scaled BiCMOS processes with lower parasitics and higher transit frequencies.

Minimizing distortion seems to entail an efficiency degradation which, depending on the application, can or cannot be tolerated. Continuous-wave measurements however do not tell the whole story. With modulated signals, backoff is used to operate the PA in a more linear region thus reducing the EVM of the transmitted constellation. Having better linearity means that the high-efficiency region can be better exploited, allowing an higher average efficiency even though the maximum efficiency with continuous-wave signals is lower. 5G employs modulation schemes with high PAPR so backoff efficiency is becoming more important than ever. Dynamic bias is currently being experimented as a way to adapt the amplifier operating point to the symbol being transmitted thus improving both linearity and efficiency at the same time. Another technique, dating back to 1936, the Doherty power amplifier [76, 77], is seeing renewed interest for 5G PAs. Thanks to the clever combination of two linear amplifiers high efficiency in backoff can be obtained. Both of those techniques seem promising and may allow to recover the efficiency lost in trying to optimize the PA for maximum linearity.

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