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Design of Fully-Integrated High-Resolution Radars in CMOS and BiCMOS Technologies

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To my family

"It can't rain all the time"

- The Crow

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ABSTRACT

The RADAR, acronym that stands for RAdio Detection And Ranging, is a device that uses electromagnetic waves to detect the presence and the distance of an illuminated target. The idea of such a system was presented in the early 1900s to determine the presence of ships. Later on, with the approach of World War II, the radar gained the interest of the army who decided to use it for defense purposes, in order to detect the presence, the distance and the speed of ships, planes and even tanks.

Nowadays, the use of similar systems is extended outside the military area. Common applications span from weather surveillance to Earth composition mapping and from flight control to vehicle speed monitoring. Moreover, the introduction of new ultrawideband (UWB) technologies makes it possible to perform radar imaging which can be successfully used in the automotive [29, 40] or medical field [13].

The existence of a plenty of known applications is the reason behind the choice of the topic of this thesis, which is the design of fully-integrated high-resolution radars.

The first part of this work gives a brief introduction on high resolution radars and describes its working principle in a mathematical way. Then it gives a comparison between the existing radar types and motivates the choice of an integrated solution instead of a discrete one.

The second part concerns the analysis and design of two CMOS high-resolution radar prototypes tailored for the early detection of the breast cancer. This part begins with an explanation of the motivations behind this project. Then it gives a thorough system analysis which indicates the best radar architecture in presence of impairments and dictates all the electrical system specifications. Afterwards, it describes in depth each block of the transceivers with particular emphasis on the local oscillator (LO) generation system which is the most critical block of the designs. Finally, the last section of this part presents the measurement results. In particular, it shows that the designed radar operates over 3 octaves from 2 to 16GHz, has a conversion gain of 36dB, a flicker-noise-corner of 30Hz and a dynamic range of 107dB. These characteristics turn into a resolution of 3mm inside the body, more than enough to detect even the smallest tumor [39].

The third and last part of this thesis focuses on the analysis and design of some important building blocks for phased-array radars, including phase shifter (PHS), true time delay (TTD) and power combiner. This part begins with an exhaustive introduction on phased array systems followed by a detailed description of each proposed lumped-element block. The main features of each block is the very low insertion loss, the wideband characteristic and the low area consumption. Finally, the major effects of circuit parasitics are described followed by simulation and measurement results.

SOMMARIO

Il RADAR, acronimo per RAdio Detection And Ranging, é uno strumento che sfrutta le proprietá elettromagnetiche della materia per rilevare l'eventuale presenza e distanza di oggetti non conosciuti. L'idea di un simile dispositivo fu presentata per la prima volta nei primi anni del 1900 per determinare la presenza di navi in avvicinamento. Solo dopo qualche anno, con l'avvicinarsi della seconda guerra mondiale, cominció la vera e propria ricerca e sperimentazione. Inizialmente, infatti, il radar venne utilizzato prettamente in ambito militare per rilevare la presenza, la distanza e la velocitá di navi, aerei e carri armati nemici.

Ai giorni nostri, invece, il concetto di radar viene esteso ben al di fuori dell'ambito militare. Infatti é possibile trovare soluzioni per applicazioni che spaziano dalla mappatura del terreno alla sorveglianza delle condizioni metereologiche e dal controllo del traffico aereo all'individuazione della velocitá dei veicoli. Inoltre, l'introduzione di nuove tecnologie a larga banda (UWB), rende possibile la generazione di immagini radar le quali possono essere sfruttate con successo sia in ambito medico [13] che automotive [29, 40].

L'esistenza di un'infinitá di applicazioni conosciute legata all'estrema versatilitá dei radar é la motivazione che mi ha spinto a focalizzare il mio lavoro sull'analisi e la progettazione di radar integrati ad alta risoluzione.

La prima parte di questa tesi dá una breve introduzione circa i radar ad alta risoluzione e ne descrive il principio di funzionamento ricavandone le principali equazioni. Essa mette inoltre a confronto le varie tipologie di radar motivando la scelta di un radar integrato rispetto ad una soluzione a componenti discreti.

La seconda parte, invece, tratta l'analisi e la progettazione di due prototipi di radar CMOS ad alta risoluzione destinati alla rilevazione preventiva dei tumori al seno. Dopo una breve spiegazione delle motivazioni che stanno alla base di questo progetto, viene effettuata un'accurata analisi di sistema la quale permette di scegliere l'architettura meno sensibile alle non idealitá del ricevitore. Successivamente viene data una descrizione dettagliata di ogni singolo circuito che constituisce il ricetrasmettitore, con particolare enfasi alla generazione delle frequenze la quale costituisce il blocco piú critico dell'intero sistema. Infine, l'ultima sezione di questa seconda parte, presenta i risultati di misura sia per quanto riguarda la caratterizzazione elettrica che per quanto riguarda gli esperimenti di imaging. In particolare, sará possibile notare che il radar opera su una banda di 3 ottave da 2 a 16GHz, ha un guadagno di conversione di 36 dB, una flicker-noise-corner di 30Hz ed un range dinamico di 107dB. Tali caratteristiche si traducono in una risoluzione di 3mm nel corpo umano, piú che sufficiente per rilevare anche il piú piccolo tumore [39].

La terza ed ultima parte di questa tesi si occupa dell'analisi e progettazione di alcuni blocchi fondamentali per phased-array radar, tra i quali phase shifter (PHS), true time delay (TTD) e power combiner. La prima sezione di questa terza parte introduce esaustivamente i sistemi phased-array, mentre la seconda fornisce una descrizione dettagliata dei blocchi proposti. Le caratteristiche principali sono la bassa perdita di inserzione, la larga banda passante ed il basso consumo di area. Verranno poi presentati i principali

effetti introdotti da capacitá ed induttanze parassite, nonché alcuni metodi per limitarne i rispettivi effetti indesiderati. Seguiranno i risultati di simulazione e misura.

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Part I

RADAR OVERVIEW

1

INTRODUCTION TO RADAR SYSTEMS

The RADAR, acronym that stands for RAdio Detection And Ranging, is a particular type of systems that is able to detect the presence of objects. In principle, it was largely developed to satisfy the needs of the military for surveillance and weapon control [74]. Nowadays, however, its use is extended beyond the military context. Applications span from the safe travel of aircraft, ships and spacecraft to the weather surveillance. Other applications include medical imaging, car security, crash prevention and many others.

This chapter briefly introduces the radar system. It describes its principle of operation and gives a short insight on the equations that underlie its correct operation. Finally the last section gives a description of the major different types of radars.

1.1 DESCRIPTION AND WORKING PRINCIPLE

The working principle of a Radar system is relatively simple, even though its realization is not, in general. It consists of radiating electromagnetic energy and detecting the backscatter from reflecting objects (targets). From the received signal, informations about the target are retrieved. The range, i.e. the distance between the generating antenna and the target, is obtained from the time-of-flight and the wave propagation velocity in the medium. The angular location, instead, is retrieved by means of a directional antenna while the target velocity is retrieved due to the Doppler effect caused by the relative motion between the target and the radar antenna.

The resolution is one of the most important parameters of a radar system. The resolution can be obtained in range, in angle or both. The range resolution, usually called slant-range resolution, is the resolution along the direction of the wave propagation and is directly related to the bandwidth of the transmitted pulse. The larger the bandwidth, the higher the resolution. The angular resolution is related to the electrical dimension of the antenna. The larger the antenna, the higher the resolution. However, a high angular resolution can be obtained without using large antennas by means of the Synthetic Aperture approach (Sec. 1.6.3).

A simple block diagram of a conventional radar is shown in Fig. 1. The radar signal, which is usually a short pulse or a repetition of short pulses, is amplified by a power amplifier and transmitted by means of an antenna. The power amplifier must feature

large bandwidth and flat gain along with a high efficiency. The output power is determined by the the maximum desired range and by the receiver sensitivity. Short-range applications usually use integrated power amplifiers whose output a power in the order of milliwatts (car radar examples are [23, 88]). There are, however, applications that demand a larger output power, even in the order of kiloWatts, or more (long-range applications like weather surveillance, flight control, etc.).
The duplexer allows to share a single antenna for both receiver and transmitter side. It must show a low insertion loss and a high isolation between TX output and RX input. This allows to protect the LNA input from the large amount of transmitted power and avoids the saturation of the receiver. The duplexer is generally a circulator or a hybrid coupler. Nevertheless, it may be replaced by a simple switch in applications where TX and RX don't work in the same time slot.
The task of the antenna is to irradiate the output power of the PA and receive the reflected energy from the target. In principle it was directive and mechanically steered, hence it concentrated the power in the desired direction into a narrow beam. Recently, the same result is obtained by means of a phased array architecture without the need of mechanically moving the antenna.
The receiver captures and elaborates the backscattered signal. It is composed by a low noise amplifier and a downconversion stage. Not to impair the received signal with the noise, the LNA must feature a high gain with a low noise figure. In addition, it must show a well defined input impedance in order to match the antenna. The downconversion stage provides a translation of the received spectrum toward lower frequencies. This makes the analog-to-digital conversion and the post processing operation simpler. Depending on the system characteristics and specifications, the downconverted frequency may be zero (direct conversion architecture) or an intermediate frequency IF (this is the case of the super-heterodyne architecture). Finally, a baseband amplifier adapts the signal to the input range of the ADC while providing anti-alias filtering.

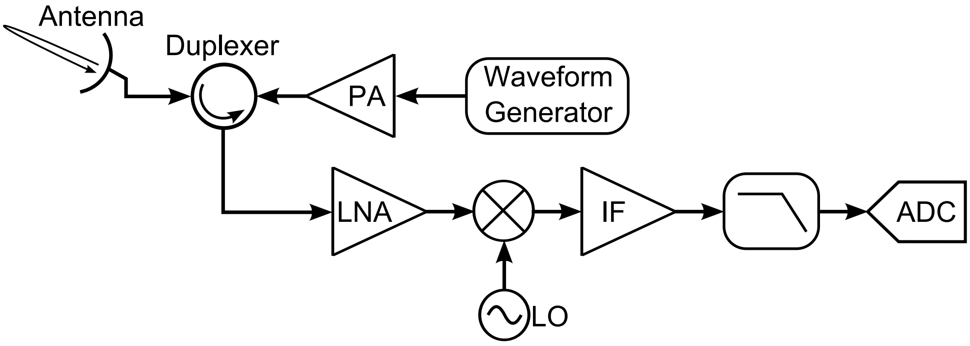


Figure 1: Simple block diagram of a conventional radar system.

1.2 IMPORTANCE OF AN INTEGRATED SOLUTION

During the World War II, the radar development increased and radars were used for defence purposes, to detect the presence, distance and speed of ships, planes and tanks. They were also used for missile guidance and tracking. Each of these applications, therefore, was related with long-range detection. As a consequence the required output power had to be high, even in the order of kilowatt. This, together with the relatively old employed technology, made the system heavy, bulky and expensive. However, it was not an issue since, usually, a single transceiver with a large antenna was mounted on ships or control towers. Later on, radar applications have been extended outside the military area, for weather surveillance, flight control, astronomy, etc. Huge parabolic antennas were used to increase the antenna gain and directivity and, sometimes, they were mounted on mobile supports that increased even more the total dimension. As a consequence, even in this case, the relatively large radar active circuit's dimension was not an issue.

Nowadays, the number of different radar applications is getting larger. New short-range applications are emerging, for example in the automotive, industrial or biomedical field. Unlike standard long-range applications, here the dimension of the radar circuit is fundamental. As an example, in a single car one may found several different radars, each used for different functions: crash prevention, adaptive cruise control, parking assistance, blind-spot detection, etc. A complete fully-integrated radar allows to reduce the system physical dimension and the implementation cost. The absence of external components, moreover, increases the robustness of the system as well as its reliability. The need of an integrated solution becomes evident in those systems based on the phased array architecture. Here, the total system is composed by N transceivers connected to an antenna array. Since the antennas spacing is related to the wavelength of the transmitted signal, a spacing of few centimeters is needed if the frequency of the signal is in the order of few GHz. Here, the use of integrated radars is mandatory to avoid long RF interconnections between antennas and radar circuits. However, short-range radar applications are not the only which can benefit from the technology scaling. Recently, in fact, fully integrated long-range applications have been presented [4].

To conclude, the availability of fully-integrated radars is seen as a need in today's applications. An integrated circuit allows to reduce both system dimension and cost while increasing the overall performances.

1.3 RADAR EQUATION

As explored in the introduction, the radar was invented for the detection and ranging of unknown targets. Modern high-resolution radars provide additional features like ground mapping, target recognition and, more recently, imaging capabilities. Nonetheless, the basic equation that describes the received backscatter power as a function of system parameters is always the same.

Consider Fig. 2 which shows the radar operating concept. The transmitted and received signals are in general considered to be generated and received from two different antennas placed in two different positions. A free-space propagation is considered, hence no multipath or reflection occurs (except the reflection introduced by the target). Additionally, we assume that the target is small enough to be uniformly illuminated by the transmitted beamwidth and its dimension along the direction of the wave propagation is small as compared with the pulse duration. The power density incident to a target at range R_t from the transmitting antenna is

$$s_t = \frac{P_t G_t}{4\pi R_t^2} \left[\frac{W}{m^2}\right], \tag{1}$$

where P_t is the transmitted power and G_t is the transmitting antenna gain. At this point, the target scatters the incident power in all directions, including back to the transmitting and receiving antennas. The power density that reach the receiver is

$$s_r = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 R_t^2 R_r^2} \left[\frac{W}{m^2}\right], \tag{2}$$

where G_r is the receiving antenna gain, R_r is the target range with respect to the receiver, λ is the wavelength and σ is the radar cross section (RCS) of the target. This term, that will be better explained in Sec. 1.4, determines the amount of incident power that the target scatters back to the antenna. In a monostatic radar, where the antenna is the same for TX and RX, $G_t = G_r = G$ and $R_t = R_r = R$, thus

$$s_r = \frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 R^4} \left[\frac{W}{m^2}\right]. \tag{3}$$

The ability of the radar to detect the received backscatter, and thus the target, depends on the receiver sensitivity. The sensitivity itself depends on the noise figure of the system, on the bandwidth of the received signal and on the needed SNR that allows a correct detection. Hence, a common form for the range equation written as a function of the input SNR of the system is

$$R = \left[\frac{P_t G^2 \lambda^2 \sigma}{(4\pi)^3 k T_e \beta (S/N)_{in} L}\right]^{\frac{1}{4}}, \tag{4}$$

where the quantity kT_e is the noise power density at the antenna terminals, β is the signal bandwidth and L is a factor that takes into account all the radar losses.

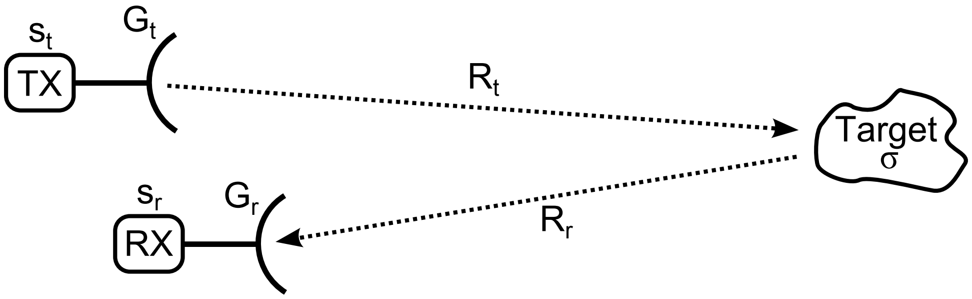


Figure 2: Derivation of the radar equation.

1.4 RADAR CROSS SECTION

A radar is able to detect or identify an unknown object because it is a source of backscattered signal. A quantification of this echo is, therefore, mandatory for a correct design of the system. For this purpose, the target is described as an effective area called radar cross section (RCS). To better understand its meaning, consider Fig. 3 that shows a monostatic radar placed at the center of an imaginary sphere whose surface contains the target. The target RCS is the cross-sectional area on the sphere's surface which isotropically re-radiates toward the receiver the same amount of power that would have radiated the target [87]

$$\sigma = \frac{\mathit{Equivalent\,isotropically\,scattered\,power}}{\mathit{Incident\,power\,density}} = \frac{4\pi R^2 s_e}{s_i}, \tag{5}$$

where R is the sphere radius ($R >> \lambda$), s_i is the incident power density and s_e is the echo power density at the radar. Notice that the radar cross section must be calculated in the far field. This makes the RCS independent on the target range. Another well used definition of the RCS is

$$\sigma = \lim_{R\to\infty} 4\pi R^2 \frac{|E_e|^2}{|E_i|^2}. \tag{6}$$

that inherently defines the RCS in the far field. Additionally, since the electric field $|E_e|$ at the receiver antenna decays with R, Eq. 6 shows the independence of the radar cross section from the target range.

The target RCS is often measured relative to that of a conducting sphere. The radar cross section of a sphere with radius a is equal to its cross-sectional area πa^2. Unlike the echo of the sphere, however, which is independent of the viewing angle, the echoes of more complex targets vary significantly with the orientation.

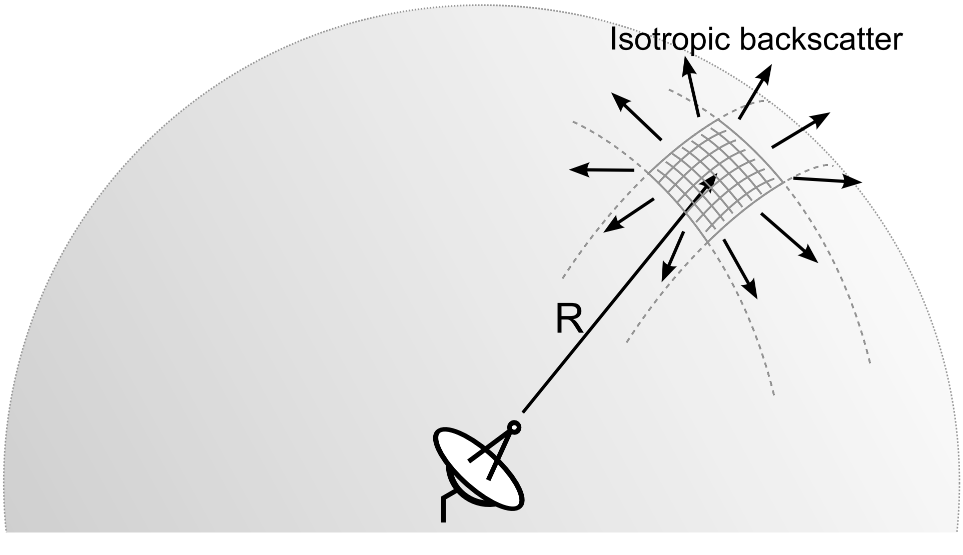
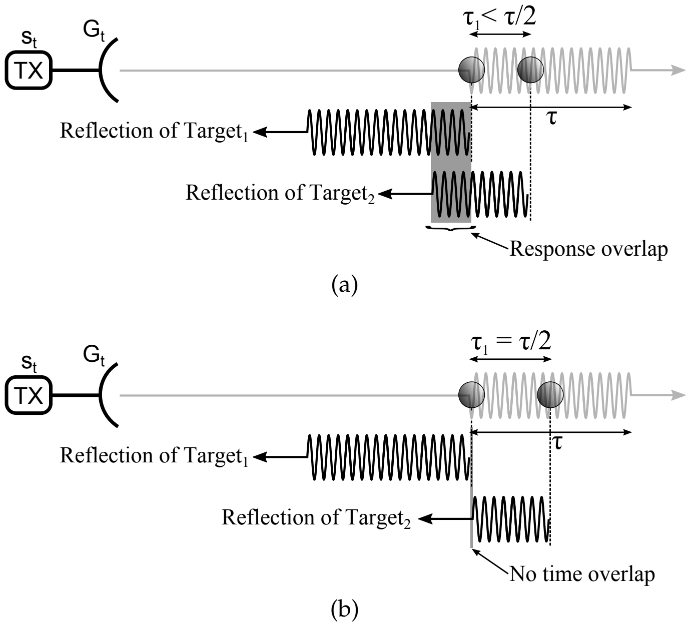


Figure 3: Explanation of the radar cross section concept.

1.5 RESOLUTION

The definition of the radar resolution is not unique. We can refer to the range resolution or angular resolution. Leveraging the Doppler effect, the radar allows moreover to determine the speed of moving targets. Thus, the Doppler resolution is another measure of the system resolution.

The radar range resolution, called slant-range resolution, can be defined as the ability to resolve point targets that are separated in range from the radar. An intuitive way to obtain the range resolution is explained as follows. Consider two targets located at ranges R_1 and R_2, corresponding to time delays t_1 and t_2, respectively (Fig. 4). At first,



$\tau_1 < \tau/2$
s_t
G_t
TX
τ
Reflection of Target_1
Reflection of Target_2
Response overlap
(a)
$\tau_1 = \tau/2$
s_t
G_t
TX
τ
Reflection of Target_1
Reflection of Target_2
No time overlap
(b)

Figure 4: Radar range resolution. Overlap between backscattered signals when the target are placed too close to each other (a) and minimum relative distance which allows a correct detection of the two objects (b).

assume that they are separated by $v\tau_1$, where $\tau_1 < \tau/2$, τ is the pulse width and v the wave propagation velocity. In this case, when the tail edge of the pulse begins to be reflected by the first target, a large amount of scatter is already available from the target number 2, Fig. 4(a). Thus, the response of the two targets overlap and cannot be separated in the time domain. Consider now the case where the target separation is $v\tau/2$ (Fig. 4(b)). In this case, when the tail edge of the pulse strikes the first target, the early-time reflection of the second approaches the first target. Hence, a separation of $v\tau/2$ is the minimum one that allows a time separation of the reflected pulses. In other words, the minimum resolution of the system is

$$\Delta_{r_s} \approx \frac{v\tau}{2} = \frac{v}{2B}, \tag{7}$$

where B is the pulse bandwidth, which is approximately related with the pulse duration as $\tau = 1/B$. As suggested by Eq. 7, in order to achieve fine range resolution one must minimize the pulse width. This causes a reduction of the average transmitted power (for a fixed peak power) and the inability of detecting targets placed at very long distances. However, a technique called "pulse compression" (not described in this introduction) allows to obtain a very high range-resolution without decreasing the signal duration. Hence it allows both high resolution and long range detection.

The Doppler resolution is the ability of a radar to resolve the target radial velocity. The Doppler frequency produced by a single point target at radial velocity v_i is

$$f_D = \frac{2v_i}{\lambda} = \frac{2f_0 v_i}{v}, \tag{8}$$

where $f_0 = v/\lambda$, $f_0 >> f_D$ is the radar carrier frequency. The Doppler resolution is fundamentally related to the system characteristics. In today's radar, the baseband signal is converted to the digital domain by means of an ADC. In this case, an exact analogy with the range resolution is obtained

$$\Delta f_D = \frac{1}{T}, \tag{9}$$

where T is the time-domain length of the transmitter pulse. As opposed to the range resolution case, a better Doppler resolution is obtained by long pulses.

In addition to what has been presented in this section, another definition of resolution is available in a conventional radar. The angular resolution, is determined by the radiation pattern of the antenna and is defined as the beamwidth of the mainlobe. In a polar plot of the antenna radiation pattern, the beamwidth is usually defined as the angle between the two points where the magnitude of the radiation pattern decreases by 3dB with respect to the peak power.

1.6 RADAR CLASSIFICATION

Radars are often classified by the types of waveforms they use. We can also distinguish between Continuous Wave (CW) and Pulsed Radars.

This section describes the similarities and differences of the most well-known radar types.

1.6.1 *Pulsed Radar*

Pulsed radar is one of the most well-known type of radars. This name arises from the type of transmitted signal: a pulse or, more generally, a train of pulses. The target range is extracted from the two-way time delay between the transmitted and received signal. As a consequence, the range-resolution increases with a decrease of the pulse duration, or equivalently, with an increase of the pulse bandwidth. The target speed, instead, can be extracted from two consecutive range measurements or using the pulse Doppler technique.

The pulse repetition frequency (PRF) is a critical design parameter: a low PRF results in a large unambiguous range (i.e. the maximum distance that can be resolved without spatial ambiguity) but a poor average transmitted power; on the other hand, a large PRF allows a high average transmitted power but decreases the maximum unambiguous range.

1.6.1.1 *Radar Equation for Pulsed Radar*

The range equation of Eq. 4 does not take into account the nature of the transmitted signal. It is thus valid for both pulsed and continuous-wave radars. Sometimes, however, can be useful to adapt the radar equation on the actual system being considered. The radar equation for a pulsed radar, derived from Eq. 4, is

$$R = \left[\frac{\hat{P_t} \tau' G^2 \lambda^2 \sigma}{(4\pi)^3 k T_e (S/N)_{in} L} \right]^{\frac{1}{4}}, \tag{10}$$

where $\hat{P_t}$ is the peak power and τ' is the pulse width.

1.6.2 *Continuous Wave Radar (CW)*

As the name suggests, continuous wave (CW) radars transmit and receive continuous waveforms. As a consequence, the average transmitted power may be relatively high even with a medium peak output power. This simplifies the output stage and makes it more reliable. Additionally, it allows a long-range operation even with solid-state components. Depending on the nature of the continuous waveform, we can distinguish between unmodulated CW and modulated CW radars. This section gives a short insight on these two categories and explains advantages and disadvantages of both.

1.6.2.1 *Unmodulated Continuous Wave Radar*

Unmodulated continuous wave radars transmit and receive signals which may be considered to be pure sinewaves. The small bandwidth of the output signal allows to reduce interference problems with other systems. This also makes the downconversion simpler since it does not need a large IF bandwidth.

The spectrum of an unmodulated CW radar echo from stationary targets is at f_0, i.e. the frequency of the transmitted signal. Conversely, if the target is moving with respect to the radar, the received signal results shifted by the Doppler shift f_D

$$f_D = \frac{2f_0 v_i}{v}, \tag{11}$$

where v_i is the relative speed between target and radar, f_0 is the frequency of the transmitted signal and v is the wave propagation velocity in the medium. As a consequence of this frequency shift, the main advantage of a unmodulated CW radar is the ability to handle, without velocity ambiguity, targets at any range and with any velocity.

Due to the signal characteristics, a unmodulated continuous wave radar is not capable to measure the target range, except with a very low maximum unambiguous range. Sometimes, however, small AM or FM modulation is employed to give a rough indication of the range.

1.6.2.2 *Frequency Modulated Continuous Wave Radar*

As explained in Sec. 1.6.2.1, an unmodulated CW radar allows a simple and accurate recognition of the target velocity but it does not allow to measure its range, except with a maximum unambiguous range in the order of the wavelength of the transmitted signal. This issue can be resolved adding a modulation scheme on the transmitted signal. Frequency modulated continuous wave radars, for example, use sinusoidal waveforms whose frequency is changed according to a modulation signal. Since, in practice, the frequency cannot be continually changed in one direction, a periodic modulation is normally used. Fig. 5(a) shows an example of a transmitted (solid line) and received (dashed line) signal backscattered from a stationary target. The signal is supposed to be a triangular LFM (linear FM) waveform. The modulation, however, does not need to be triangular; it may be sinusoidal, saw-tooth, etc. The rate of frequency change $\dot{f}$ is

$$\dot{f} = 2f_m \Delta f, \tag{12}$$

where Δf is the total frequency variation. The beat frequency f_b, defined as the difference between transmitted and received frequency, is

$$f_b = \Delta t \dot{f} = \frac{2R}{v} \dot{f}, \tag{13}$$

where R is the target range. Hence, the target range R is obtained from

$$R = \frac{v f_b}{4 f_m \Delta f}. \tag{14}$$

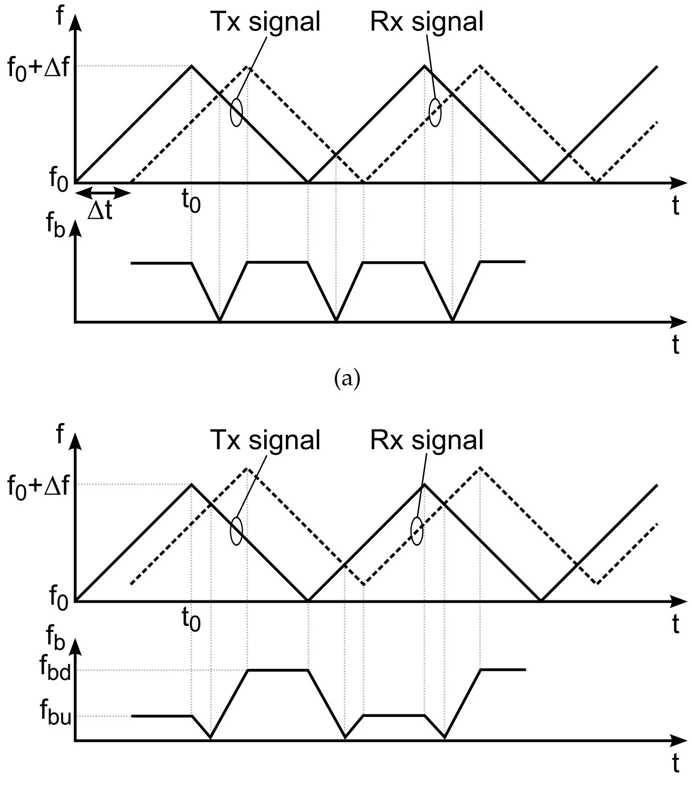
When the target is moving with a radial velocity v_i, the received signal experiences a frequency shift due to the Doppler effect. As visible in Fig. 5(b), the Doppler shift term adds or substracts from the beat frequency during the negative or positive slope of the modulated signal. Calling f_{bu} and f_{bd} the minimum and maximum beat frequency, it follows that

$$f_{bu} = \frac{2R}{v} \dot{f} - \frac{2\dot{R}}{\lambda}, \qquad f_{bd} = \frac{2R}{v} \dot{f} + \frac{2\dot{R}}{\lambda}, \tag{15}$$

where $\dot{R}$ is the target range-rate, i.e. the target velocity along a direction connecting the radar with the target. Similarly, we can obtain

$$R = \frac{v}{4\dot{f}} (f_{bu} + f_{bd}) \qquad \dot{R} = \frac{\lambda}{4} (f_{bd} - f_{bu}). \tag{16}$$

Thus, modulated continuous wave radars allow to retrieve both target range and velocity (range-rate).



(a)

(b)

Figure 5: Transmitted and received LFM signals when the target is stationary (a) or not (b).

1.6.2.3 *Radar Equation for Continuous Wave Radar*

Like in Sec. 1.6.1.1, a radar equation for continuous wave radars is derived here. Although this implementation uses continuous waveforms, and thus infinite in length, usually the data processing is made in the frequency domain by means of an ADC and a FFT. Since the FFT process cannot handle infinite length data sets, the downconverted signal is windowed after the ADC conversion. Hence, the radar equation adapted for CW radars is

$$R = \left[\frac{P_{CW} T_{win} G^2 \lambda^2 \sigma}{(4\pi)^3 k T_e (S/N)_{in} L L_{win}} \right]^{\frac{1}{4}}, \tag{17}$$

where P_{CW} is the continuous wave output power, T_{win} is the length of the window used in computing the FFT and L_{win} is a loss term associated with the windowing process.

1.6.3 *Synthetic Aperture Radar (SAR)*

Synthetic aperture radars (SAR) are specifically used to generate a high-resolution image of the illuminated volume. They allows to obtain fine resolution in both slant range and cross range without using large antennas. Slant-range resolution is the resolution along the line-of-sight direction. It depends on the bandwidth of the transmitted pulse. Cross-range resolution, instead, refers to resolution transverse to the radar's line-of-sight along the surface being mapped and depends on the aperture of the antenna. The larger the aperture, the finer the resolution.

A synthetic aperture radar takes advantage of the relative motion between the radar and the target to obtain a large antenna (synthetic) aperture using a single small antenna. In fact, as depicted in Fig. 6, for each radar position, the transceiver transmits a short pulse, processes the backscattered signal from the target and saves the results in a memory. Finally, a high resolution image of the illuminated volume is obtained by post-processing all the measured data. Even though a single antenna is used at a time, the synthetic antenna array behaves like a real antenna array having the same dimension. A similar behavior is obtained by moving the target instead of the radar, leading to an Inverse Synthetic Aperture Radar (ISAR).

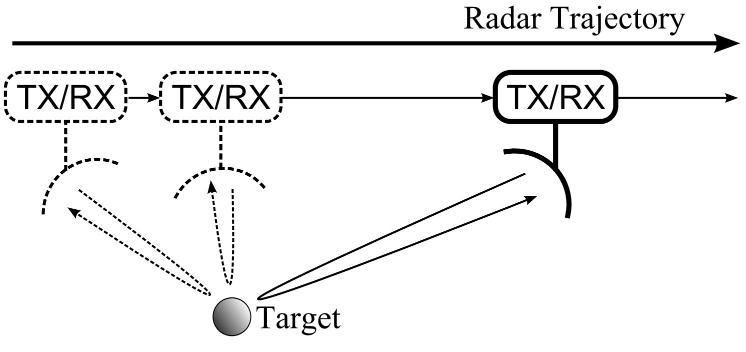


Figure 6: Principle of operation of a synthetic aperture radar (SAR).

1.6.3.1 *Stepped Frequency SAR*

As already explained, a synthetic aperture radar allows to obtain a fine resolution both in slant (Δr_s) and cross (Δr_c) range by illuminating the target from many view points. A larger pulse bandwidth corresponds to an improvement in both resolutions.

The echo signal from an illuminated target is usually observed in the time domain to obtain the desired target range. However, any signal can be described either in the time or frequency domain. In fact, a short RF pulse transmitted at a fixed pulse repetition frequency (PRF) can be defined as a Fourier series of steady-state frequency components with a frequency spacing equal to the radar's PRF [87]. Lets now see how does it work. In the TX side, the transmitted signal is a single tone stepped in frequency in order to cover the desired bandwidth (see Fig. 7). In the RX side, the I and Q components of the backscattered signal are measured and stored in a memory. As a result, a synthetic time domain pulse can be retrieved from the stored measurements by means of an IFFT. The main advantage of this implementation is that it removes the requirements for both wide instantaneous bandwidth and high sampling rate by sampling nearly-steady-state signals. Additionally, it allows to increase the resolution by generating stepped-frequency signals covering a wider bandwidth.

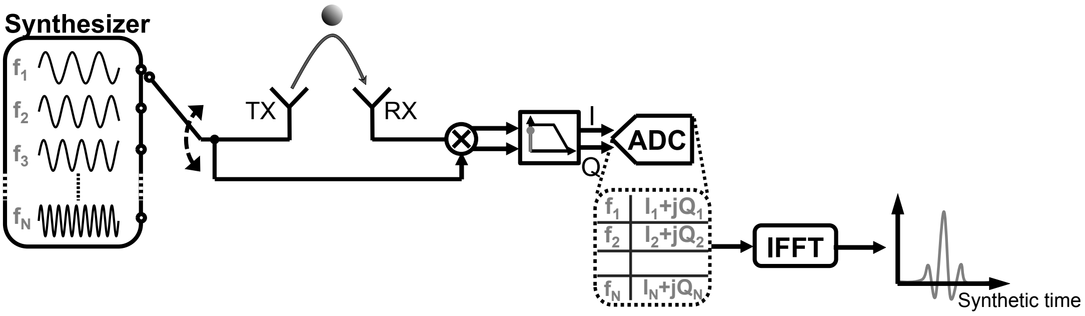


Figure 7: Principle of operation of a Stepped Frequency radar. A direct-conversion receiver is assumed.

1.6.4 *Phased Array Radar*

A phased array radar is composed by an array of N transceiver each connected to one element of an antenna array. The peculiarity of these type of systems relies on the possibility of changing the phase of the transmitted/received signal in each path. This possibility translates into a number of advantages. First, the antenna pattern can be changed, hence incrementing the antenna gain and directivity. Second, the output SNR increases and also the dynamic range. Third, the equivalent isotropic radiated power (EIRP) increases, thus a smaller output power is required for the single power amplifier. These advantages (and others) make the phased array architecture an interesting solution for a high performance radar. A more detailed description of these systems is detailed out in Chapter 6.

Part II

ANALYSIS AND DESIGN OF AN INTEGRATED HIGH-RESOLUTION RADAR FOR BREAST CANCER DIAGNOSTIC IMAGING IN 65NM CMOS

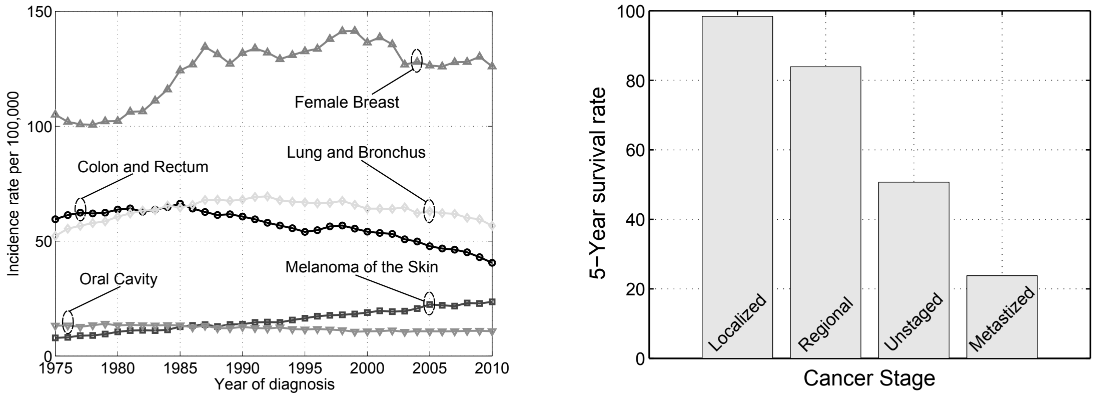
2

INTRODUCTION

In the last few years, microwave radar imaging has been intensively investigated for medical purposes. Among the many examples of biomedical applications, the detection and early diagnosis of breast cancer has seen an increase of interest[25, 54, 70, 93, 71, 72, 46, 28, 24, 26, 65].
Breast cancer is the most common non-skin-related malignancy among female population. In the United States more than 180 thousand new cases are diagnosed and more than 40 thousand women die from this disease each year [63]. Fig. 8(a) shows the age-adjusted incidence rate per 100000 people grouped by cancer site [38]. Breast cancer is by far the most incident tumor, with an incidence of at least twice that of any other types of tumors. An early prevention is the key factor in order to deliver long-term survival to patients. A 5-years survival rate of only $\approx 20\%$ is recorded if the tumor is detected in a metastasized stage, as highlighted in Fig. 8(b). On the other hand, more than 98% cure rates are possible if the cancer is detected in its first stage.
The mammography, consisting of an X-ray image of the compressed breast, is the most common imaging tool for the detection of non-palpable tumors [63]. However, ionizing radiations together with breast compression lead discomfort in patient treatment. Additionally, more than $10-30\%$ tumors are missed by the mammography due to the presence of dense glandular tissue around the tumor, absence of microcalcifications in the early stages and location too close to the chest wall or underarm. Moreover, a large number of false-positive are diagnosed, leading to a more invasive test to assess the real absence of malignancies.
Ultrawideband (UWB) microwave imaging is an attractive alternative. It leverages the contrast of dielectric proprieties between benignant and neoplastic tissues at microwave frequencies to identify the presence of significant scatterers [52]. Fig. 9 shows the permittivity and conductivity of normal and malignant breast tissues. It is worth to notice that, compared with X-ray, a permittivity ratio as large as $1:6$ between different tissues is observed at microwave frequencies. The general concept is to illuminate the breast with an ultra wideband (UWB) pulse and collect the backscatter. From the shape and the time of arrival of the reflected pulse, information on the position and size of the scatterer are retrieved. By performing a set of measurements over different antenna positions, and by processing the obtained data in a digital beam focusing fashion, a high-resolution image

of the dielectric properties of the breast tissues can be derived.

Microwave imaging is a valid alternative to the usual mammography. The high dielectric contrast between healthy and malignant tissues at microwave frequencies makes the detection simple and reliable. These features, together with the fact that the breast does not need to be compressed, lead to a more rapid and comfortable patient examination: appropriate for a mass screening program.



(a) (b)

Figure 8: Age-adjusted cancer incidence rates grouped by cancer site [38] (a) and 5-year survival rate with respect to the breast cancer stage [38] (b).

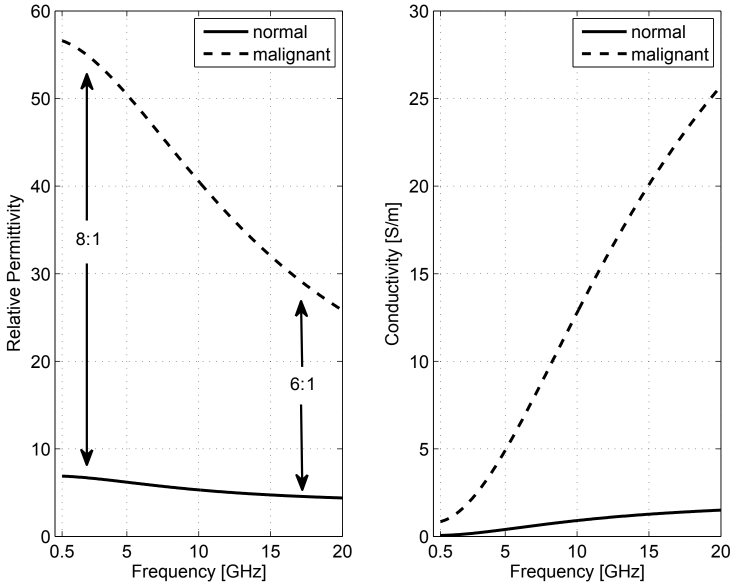
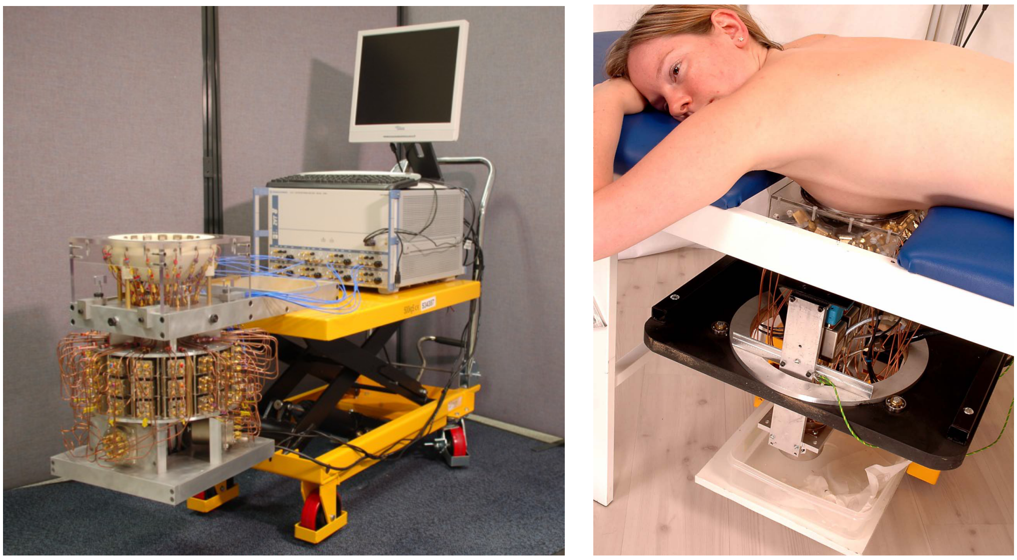


Figure 9: Cole-Cole model of the relative permittivity and conductivity of normal and malignant breast tissues.

2.1 MOTIVATIONS

Several works on microwave imaging reported over the past years show the feasibility of this technique [25, 26, 11, 45, 59, 60, 30]. Actually, the imaging system presented in [47] has demonstrated excellent results compared to X-rays and it is undergoing clinical trials. As visible in Fig. 10, the patient lies in a prone position on a special examination bed while her breast extends in a hemispherical hole, of about 17cm diameter, filled with coupling liquid for better matching. The walls of the hemispherical hole are covered with a highly-dense 60-element slot antenna array connected with an external 8-port Vector Signal Analyzer (VNA) which allows 15 simultaneous S-parameter measurements in the $4-8$GHz range. The interface between antennas and VNA is made possible by an electromechanical RF switch matrix, whose size is at least three times the one of the antenna array. The whole system, composed by PC, VNA, antenna array and switch matrix, is mounted on a hydraulic trolley to ease the transportation. The presence of a highly-dedicated laboratory instrument (VNA), common to each work which reports experimental data, makes the diagnostic tool bulky and expensive. Further, the presence of costly switch matrix and high-frequency rigid-cables limits the maximum number of antennas and introduces losses, limiting the overall performance. Additionally, the limited number of simultaneous measurements increases the examination time resulting in a lower image resolution due to the patient movement [35].

As a matter of fact, the development of custom hardware is seen as a critical need by the microwave imaging community in order to improve the performance and reduce the size and cost of the system [65]. A dedicated integrated circuit can be tailored to cover the specific wide bandwidth required by medical imaging, while achieving very large dynamic ranges. The miniaturization carried about by system integration allows to envision an antenna array made of modules in which each antenna is directly assembled together with the radar transceiver chip. A switching system is therefore avoided along with any high-frequency interconnects. Only signals at low frequencies are to be distributed to the array elements. At the same time, having a transceiver for each antenna removes any limitation on the number of simultaneous measurements that can be performed. As a result, a more compact, higher performance, and lower cost system can be obtained: ideal for an early detection or post-treatment surveillance of the breast cancer.



(a) (b)

Figure 10: Microwave breast cancer imaging system developed by the University of Bristol [47] (a) and patient under examination [45] (b).

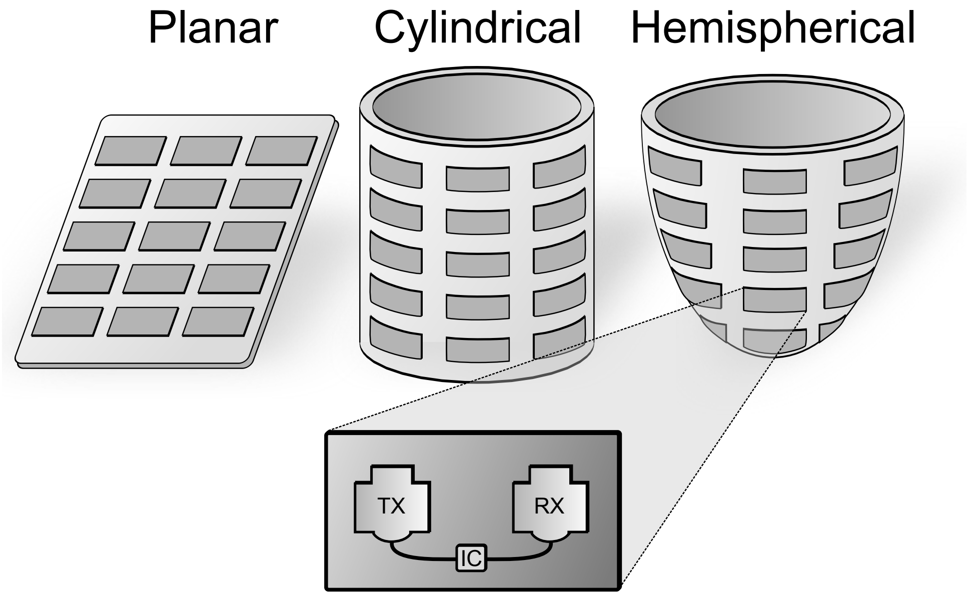


Figure 11: The three different antenna array configurations that can be used to scan the breast in a radar imaging system. Below, the envisioned imaging module made of the CMOS radar transceiver and the two wideband patch antennas.

2.2 SYSTEM OVERVIEW

As clarified in the previous section, the availability of a full-custom integrated circuit is a need for the intended application. It allows to reduce both cost and dimension, and reduces drastically the examination time. As reported in [35], in fact, the examination time plays a fundamental role in order to obtain high resolution images. A longer measurement time increases the probability of patient movement. Even the change in the blood pressure or temperature leads to approximative results.

In the microwave imaging tool proposed in this thesis, the patient's breast is positioned in front of an antenna array whose antennas are directly connected to a dedicated transceiver (Fig. 11). At a time, ideally, one transceiver transmits an ultra-wideband pulse while the others receive the backscattered signal from the breast. However, as will be better detailed out in Sec. 2.3, the combination of high resolution and large demanded dynamic range makes the implementation of the transceiver in the time-domain difficult. This problem can be circumvented by adopting the stepped-frequency continuous-wave approach (Sec. 1.6.3.1), where the UWB time domain pulse is synthetically generated starting from a set of measurements performed in the frequency domain. This operation, repeated for each antenna, can be done both in a monostatic or multistatic fashion. After all measurements are done, a $3-D$ electromagnetic characterization of the volume around the antenna array can be retrieved.

The patient position leads to different possible antenna array configurations [25]. A planar arrangement can be used to scan the naturally flattened breast when the patient lies in a supine position. On the contrary, a cylindrical or hemispherical array allow to scan the breast when the patient lies in a prone position and her breast extends through a hole in the examination bed. Among the three possible configurations, the hemispherical one is preferred because it allows the imaging from many view angles and the prone position reduces the motion effects due to patient breathing [35].

2.3 CONSTRAINTS MAPPING AND SYSTEM CHALLENGES

The continuous scaling of CMOS technologies has led to the development of plenty of new wireless standard and devices. Words like GSM, LTE, WiFi or Radar are widely used and are going to be used even more in the next few years. A complete understanding of the interaction between electromagnetic waves and human body has become a need to evaluate the potential hazard of RF radiations. In the case of biomedical application such as hyperthermia and radiometry for cancer treatment and detection, it is, moreover, a prerequisite to ensure the correct operation of the system. As a consequence, more and more papers report measurement data or fitting models on the electromagnetic proprieties of different human body tissues [52, 42, 51].

The electromagnetic properties of the breast tissues have been studied over more than 10 years. A Cole-Cole model of the relative permittivity and conductivity of normal and malignant tissues as a function of frequency is plotted in Fig. 9. This allow us to perform a finite-difference time-domain (FDTD) electromagnetic simulation to investigate the wave propagation inside the breast tissues. The simulation setup is as follows. A continuous wave source is applied to an ideal isotropic cylindrical antenna placed $1\mathrm{cm}$ away from a $2\mathrm{mm}$-thick skin layer. A $4\mathrm{mm}$ diameter tumor is inserted inside the numerical breast phantom at a distance ranging from 3 to $10\mathrm{cm}$ from the skin. The transmitted wave bounces back at the interface between adipose-dominated breast tissue and tumor while being collected by the generating antenna. The choice of tumor size and depth below the skin surface is supported by medical studies which show that smallest tumors are in the order of $9-10\mathrm{mm}$ [39] and the depht of a typical nonlactating human breast is in the order of $4\mathrm{cm}$ [18]. Additionally, almost 50% of all breast tumors occur in the quadrant near the armpit, where the breast is less than about $2.5\mathrm{cm}$ deep [66].

Fig. 12 plots the EM-simulated attenuation of the transmitted signal through the antenna-skin-antenna and antenna-tumor-antenna paths at different tumor positions. It is worth to notice the large difference between the two paths. The received signal is dominated by the skin reflection, which is large and quite constant over the entire frequency range. On the contrary, the tumor backscatter experiences a large loss and dispersion. This implies the need of a transceiver with a dynamic range in excess of $100\mathrm{dB}$ and the use of an ADC with a resolution of more than 17 bits. The use of matching liquids to reduce the air-to-skin reflection has been explored [35, 30]. However, the use of such liquids complicates the system and the almost unavoidable presence of air gaps hampers the correct imaging operation.

The radar resolution is directly related to the bandwidth of the transmitted pulse, regardless of how it has been generated. The higher the bandwidth, the shorter the pulse duration and hence the higher the resolution. The slant-range resolution Δ_{r_s} of an N-antenna array radar, i.e. in the direction of wave propagation, is proportional to the inverse of the pulse bandwidth according to

$$\Delta_{r_s} \approx \frac{v}{2B}, \tag{18}$$

where B is the signal bandwidth and v is the wave propagation velocity through the medium. Notice that the slant-range resolution is totally unrelated with the antenna array geometry and the center frequency of the transmitted signal. On the other hand the cross-range resolution Δ_{r_c}, i.e. in the direction parallel to the antenna array, is [37, 36]

$$\Delta_{r_c} \approx \frac{R}{l}\frac{v}{B}, \tag{19}$$

where R is the target range and l is the real or synthetic aperture of the antenna array (Fig. 13).

Since the smallest tumors reported in the literature are in the order of $9 - 10\mathrm{mm}$ [39, 61], a sub-centimeter resolution is preferred. A resolution of $3 - 4\mathrm{mm}$, also adequate for the intended application, requires a total bandwidth of $13 - 16\mathrm{GHz}$ and an antenna aperture of about twice the expected tumor target range. Such a large bandwidth together with the large demanded dynamic range required to correctly process the skin and tumor backscatter makes a pulsed radar implementation difficult. A simpler and more reliable architecture uses the Stepped-Frequency Continuous-Wave approach, which allows for an instantaneous narrow noise bandwidth and a very high dynamic range. In this case, continuous waves at different frequencies covering a bandwidth $B = f_{max} - f_{min}$ are transmitted and received. A synthetic time-domain pulse can then be retrieved by means of an Inverse Fast Fourier Transform (IFFT). Calling Δf the frequency step of the system, the maximum unambiguous range R_{max}, i.e. the maximum solvable range without spatial aliasing, is

$$R_{max} = \frac{v}{2\Delta f}. \tag{20}$$

Thus, a frequency step of $\Delta f = 90\mathrm{MHz}$ ensures a maximum unambiguous range of $0.55\mathrm{m}$, more than enough for this application.

To summarize, the combination of a total bandwidth of $14\mathrm{GHz}$ and an antenna array aperture $\geqslant 10\mathrm{cm}$ result in a total resolution (both Δr_s and Δr_c) of $3\mathrm{mm}$ inside the breast. The choice of the lower and upper frequency of 2 and $16\mathrm{GHz}$, respectively, maximize the signal penetration inside the body and minimize the dynamic range requirement due to the high attenuation of the tumor backscatter.

As highlighted by Eq. 18 and Eq. 19, the resolution of the system is a function of the signal bandwidth and array aperture only. No direct influence on the number of antennas are observed. However, the signal-to-clutter ratio, and thus the image quality, are significantly improved by a highly dense antenna array [36, 37]. Unfortunately, when using a commercial VNA as a transceiver, its limited port count makes the use of a big RF switch matrix necessary to interface the antenna array to the instrument. This makes the system big, expensive and, moreover, introduces additional losses which limit the performance. On the other hand, the proposed integrated transceiver can be connected to each antenna, avoiding any high-frequency interconnects. This increases the performance and reduces the implementation costs, making this architecture ideal for a cost-effective solution for follow-up post-treatment cancer surveillance.

2.4 IMAGE RECONSTRUCTION ALGORITHM

After IFFT post-processing, the output of a measurement with an N-antenna array and integrated SFCW radar transceivers (or a commercial VNA) is, assuming a monostatic configuration for simplicity, a set of time-domain waveforms. The early-time content

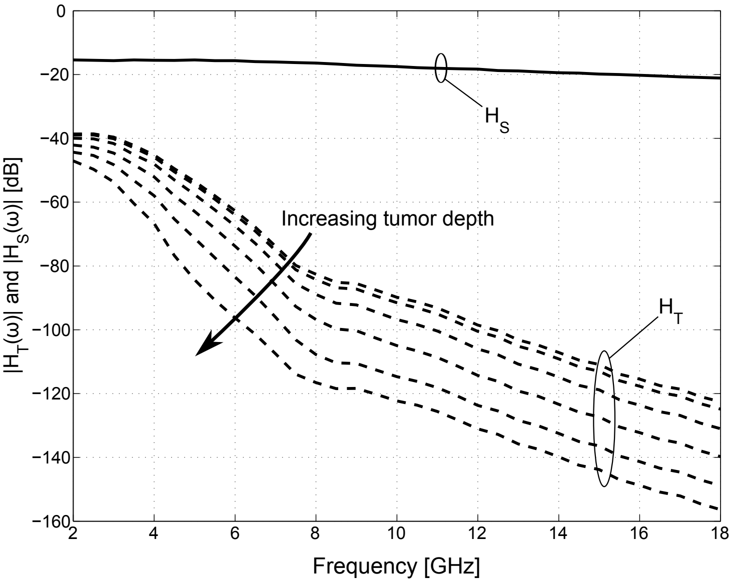


Figure 12: Antenna-Skin-Antenna ($H_S(\omega)$) and Antenna-Tumor-Antenna ($H_T(\omega)$) path attenuation for tumor depth ranging from 3 to 10cm below the skin surface. The antenna is placed 1cm away from the skin.

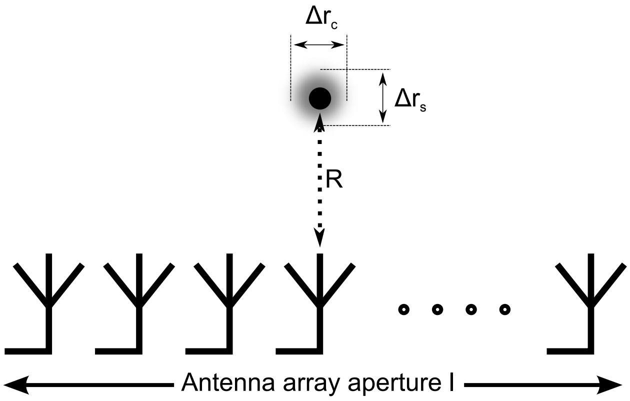


Figure 13: Typical arrangement of a N-antennas array radar showing slant and cross range resolution.

of each waveform is dominated by the large skin reflection while the late-time content contains the tumor backscatter and clutter signal. Since the skin response has a much larger amplitude with respect to the tumor response, the early-time content needs to be removed without corrupting the useful tumor signal. As proposed in [54], a calibration signal can be generated for each antenna by averaging the time response of any other antenna. In this reference signal, the skin reflection remains dominant while the tumor backscatter is reduced to negligible levels. This signal is then subtracted from the raw data, resulting in N calibrated waveforms containing only the tumor response and clutter signals. It is clear that this calibration procedure is effective as long as each antenna has the same distance from the skin. If this is not the case, more sophisticated algorithms have been presented to estimate the correct distance and efficiently remove the skin content [11, 90, 89].

The image creation can then be based on a simple delay-and-sum algorithm [77, 55]. This simple algorithm consists of calculating the intensity of each pixel by properly focusing the received signal on the pixel coordinates. First, taking into account the different electromagnetic proprieties of the different materials (air, skin and adipose-dominated breast tissue), the round-trip time $\tau_i(x, y, z)$ from the i-th antenna to the pixel of coordinates (x, y, z) is calculated. The time-domain signals $I_i(t)$ are then time shifted by the calculated round-trip time $\tau_i(x, y, z)$. In this way, the information on the considered pixel embedded in the various time-domain signals is aligned in time to the point $t = 0$. Finally, the intensity $I(x, y, z)$ of the pixel of coordinates (x, y, z) is calculated by coherently summing the contribution of all the antennas

$$I(x, y, z) = \left[\sum_{i=1}^{N} I_i(\tau_i(x, y, z)) \right]^2 . \tag{21}$$

By iterating the presented procedure for each pixel of the image, a high-resolution 2-D or even 3-D dielectric map of the inner breast can be obtained [25, 55].

2.5 SYSTEM ANALYSIS

2.5.1 *Possible System Architectures*

Based on the motivations explained in Section 2.1, we investigate the design of a low-cost fully-integrated CMOS transceiver which can be connected to each antenna of a N-antenna array and performs monostatic or bistatic measurements. Leveraging the stepped-frequency approach (c.f. Sec. 1.6.3.1, 2.3.), each IC generates a set of continuous waveforms and receives the backscattered signal from the breast. Afterwards, an external high-resolution ADC samples the low-frequency output of each transceiver and a digital processing step allows to obtain a high resolution 3-D image of the target. In the whole system, the transceiver plays a fundamental role since it must feature both large bandwidth and a very high dynamic range.

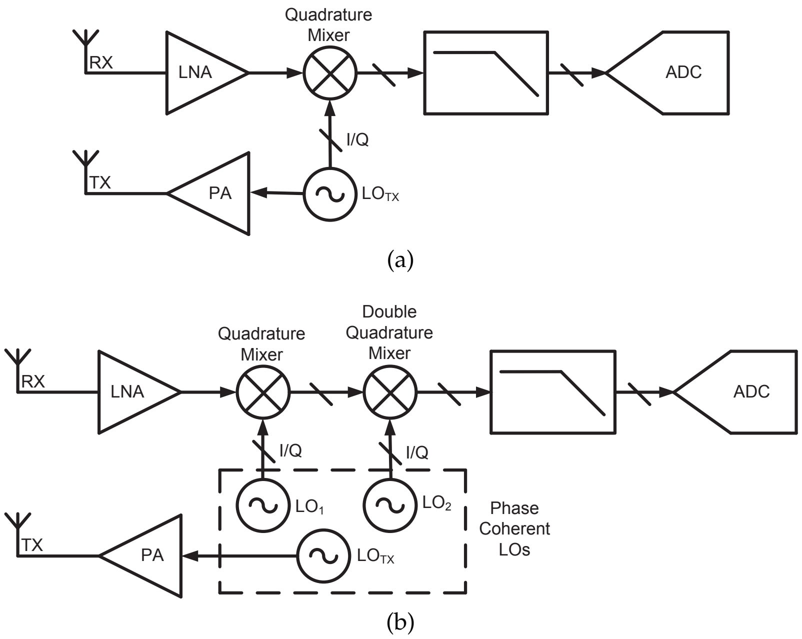
The correct system operation relies on the overall performance of the transceiver. As a consequence, care need to be taken to select the proper architecture. This section summarizes the results obtained in [8] by comparing two well-known transceiver architectures, i.e. Direct Conversion and Super Heterodyne, in terms of image quality and signal-to-clutter ratio. With the aid of a realistic behavioral model, the performance of both are evaluated in presence of the major circuit impairments like gain variation, noise, linearity and I/Q phase imbalance. Finally, the most robust and performing architecture is selected for the design of the proposed transceiver and the circuit specifications are derived based on the application requirements.

Fig. 14 shows the block diagrams of a conventional Direct Conversion and Super Heterodyne transceiver tailored for microwave radar imaging. In a direct conversion setup, a Phase Locked Loop (PLL) generates all the quadrature signals in the total bandwidth while driving both mixer and output power amplifier (PA). A TX antenna directly connected to the PA irradiates each stepped frequency waves and a RX antenna receives the backscatter from the illuminated volume. For simplicity, the antennas are supposed to be isotropic, though the comparison still holds if the antennas have constant gain over a suitable beamwidth to cover the breast surface. Furthermore,the use of two separate antennas is not a limiting factor. A similar behavior can be obtained interfacing a single-antenna to the transceiver by means of a TX/RX switch, a circulator or a directional coupler. The receiving antenna is then directly connected to a Low Noise Amplifier (LNA) which ensures high gain featuring a low Noise Figure (NF). The down-conversion stage is implemented by a quadrature mixer having PLL and LNA outputs as inputs. Since both the received and the LO signals have the same frequency, the baseband signals (I and Q) are at DC. Finally, the mixer output is low-pass filtered and digitalized by an external ADC. Notice that the presence of the baseband filter ensures a reduction of the high-frequency spurs and acts as a anti-alias filter for the analog-to-digital converter.

In a super heterodyne scheme, a PLL feeds the PA with a stepped frequency signal covering the entire system bandwidth. With the same antenna configuration like in the direct conversion case, the reflection of the breast is received and amplified by the ultrawideband LNA. The real difference between super heterodyne and direct conversion relies on the down conversion approach. A two-step quadrature downconversion is performed to a low intermediate frequency (IF). Notice that to enable possible hardware reuse, the two intermediate frequencies need to be chosen carefully. The high needed resolution requires, moreover, a low second IF frequency. Finally, the baseband signal is low-pass filtered before being digitized.

The most evident difference between the two architectures is the system complexity. The main issue with the frequency generation in the super heterodyne architecture is that all the employed LOs have to be coherent, that is they have to display a fixed and well known phase relationship when the baseband signal is sampled. This condition is, on the other hand, guaranteed in the direct conversion transceiver, as the same LO is shared between transmitter and receiver.

Since the proposed transceiver is intended to operate in a screened medical environment, the available spectrum is supposed to be free of spurs or blockers. This relaxes I/Q requirements for the super heterodyne. However, the presence of a large "in-band" interferer, i.e. the skin reflection, may cause distortion both in super heterodyne and direct conversion due to I/Q phase mismatch.



(a)

(b)

Figure 14: Block diagrams of the two UWB transceiver architectures. Direct Conversion (a) and Super Heterodyne (b).

2.5.2 *Impact of Impairments*

This section gives a short insight into the most critical circuit impairments for a transceiver tailored for breast cancer diagnostic imaging and their negative effects on the reconstructed image. Then, the most reliable and robust architecture is chosen to develop the radar transceiver.

2.5.2.1 *Gain*

Gain flatness specifies how much the conversion gain varies over the desired bandwidth. It takes into account the whole TX/RX path, including variations in the TX/RX antenna gain. Although the gain variation introduces distortion on the processed waveforms, the system shows a good robustness towards a ripple in the gain. Even a peak-to-peak ripple of $3\mathrm{dB}$ does not impair the radar performances too much, yielding a negligible level of degradation on the image quality [8].

Mismatch or process spread in the fabrication of both transceiver IC and antennas may result in a systematic gain variation over the antenna array. This contributes to deteriorate the tumor response thanks to the less efficient skin removal. However, as anticipated in Section 2.4, a more sophisticated algorithm for the skin estimation and removal can be adopted. Additionally, a calibration of the gain mismatches of each transceiver can be carried out, limiting the negative effects of the reconstructed image.

2.5.2.2 *Noise*

The impact of noise on the image quality is assessed by evaluating the time-domain waveforms processed by the transceiver. Fig. 15 shows the IFFT amplitude of the total and tumor-only backscatter from the breast. The simulation is referred to the central array's transceiver with a set of realistic parameters and impairments. Although the signal experiences a very high attenuation along the antenna-tumor-antenna path, the system shows a high robustness with respect to the thermal noise. This is due to the SFCW approach, that allows for a narrow baseband bandwidth while preserving the total UWB characteristic. Moreover, the IFFT operation leads to an intrinsic processing gain that allows the tumor enhancement with respect to the noise floor.

The high robustness to the noise is appreciated especially in the direct conversion case, where the baseband spectrum extends to DC and the high flicker noise contribution of MOS transistor is not negligible. Due to the SFCW approach the flicker noise is sampled at each frequency step f_k and is folded thanks to the sampling operation, resulting in a wideband white noise contribution [21]. In this scenario, a very low flicker noise is needed, especially for a direct conversion architecture.

2.5.2.3 *Linearity*

As discussed in Section 2.5.1, the radar operation is assumed to be performed in a screened medical environment, i.e. without other signals except those generated by the transceiver. Therefore, the linearity requirement seems to be less critical since no intermodulation between interferers occurs. However, the large magnitude of the skin reflection can excite the non-linearities of the system yielding a saturated response. Assuming to transmit a $-15\mathrm{dBm}$ tone, the maximum expected skin reflection is on the

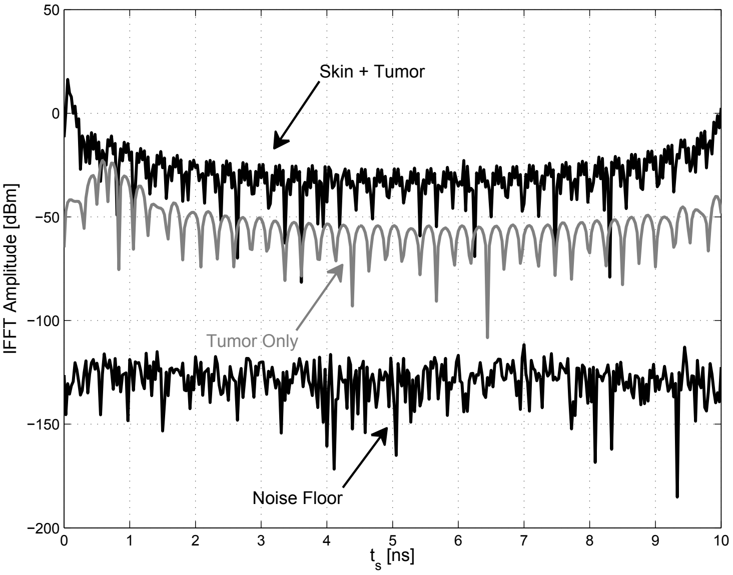


Figure 15: IFFT amplitude of the processed backscatter from the total breast and the tumor only. Plot refers to the central antenna in the antenna array configuration with a tumor depth of 3cm and a skin-antenna distance of 1cm. Other relevant system parameters are: $P_{TX} = -15\text{dBm}$, conversion gain = 40dB, NF = 10, baseband bandwidth = 100kHz, IIP2 = 20dBm, $P_{1\text{dB}} = -30\text{dBm}$ and ADC resolution of 18bit. Flicker noise, phase noise and phase mismatch are neglected.

order of −33dBm. Hence, to guarantee a correct operation, the 1dB compression point is set to be ⩾ −30dBm, both for direct conversion and super heterodyne.

Additionally to odd-order distortion, even-order intermodulation is a critical impairment in a direct conversion architecture [69]. In this scenario, however, the imaging procedure makes the transceiver more robust against second-order distortion. This depends to the fact that most of second-order distortion is due to the skin reflection which is common to all the antennas in the array. Thus, it is effectively removed by the calibration algorithm. Fig. 16 shows a simulation of the RMS error between two processed signals, one ideal and one affected by second-order distortion, before and after the skin calibration. The plot is normalized to half-LSB of a 18bit ADC with a 2V input range. As shown, the RMS error of the signal obtained after the calibration algorithm is more than one order of magnitude smaller than that before the calibration. To conclude, the contribution of second-order distortion is negligible for values of IIP2 greater than 10dBm.

2.5.2.4 *Phase-related inaccuracies*

A correct image reconstruction relies on the ability of the system to recover the phase of the backscattered signal. Hence, transmitted and received LO signals have to be coherent, i.e. they must exhibit a well know phase relationship. In this sense, phase inaccuracies, such as quadrature error, mismatch and phase noise, are critical impairments for a proper receiver operation.

The signal received at each antenna consists on the sum of two terms: the first is the skin backscatter and the second is related to the small reflection of the tumor. The presence of phase inaccuracies leads to two contributions of distortion, that are weighted by the antenna-skin-antenna $|H_S|$ and antenna-tumor-antenna $|H_T|$ transfer function, respectively. Remembering from Fig. 12 that $|H_S|$ is more than 20dB larger than $|H_T|$, the

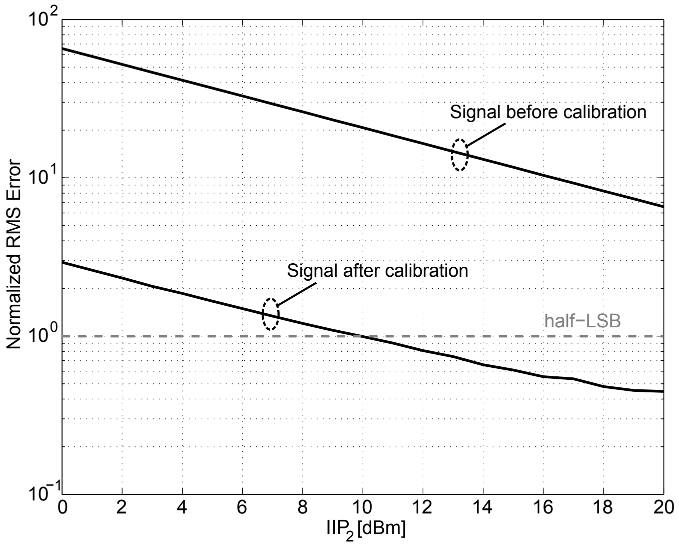


Figure 16: Comparison between the RMS error before and after the calibration algorithm. The plot is normalized to half-LSB of a 18bit ADC with 2V input range and the simulation refers to the central antenna in the antenna array configuration with a tumor depth of 3cm and a skin-antenna distance of 1cm.

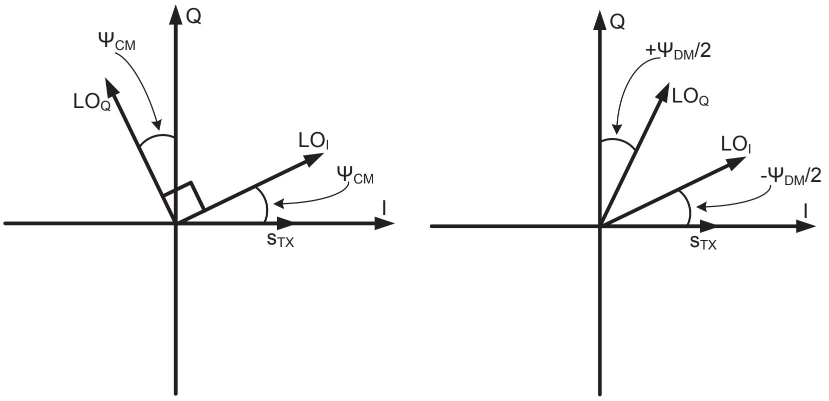
net distortion is dominated by the term relative to skin reflection. The larger the phase inaccuracies, the larger the distortion. Since the set of phase inaccuracies is different for each receiver connected to the antennas, the skin content response is different as well. This results in a non perfect skin calibration together with the inability to correctly enhance the tumor response.

Let's now consider the total phase inaccuracies as a sum of common mode ψ_{CM} and differential mode ψ_{DM} terms (see Fig. 17). Simulations show that constant values for $\psi_{CM,DM}$ do not impair the reconstructed imaged that much. In this case, only the tumor position is not well evaluated.

In general, however, common-mode and differential-mode phase mismatches are supposed to be frequency-dependent and uncorrelated between the different transceivers in the antenna array. To better capture this effect, ψ_{CM} and ψ_{DM} are modeled as gaussian variables with zero mean and variance $\sigma^2_{\psi CM}$ and $\sigma^2_{\psi DM}$, respectively. In this case, a larger variance $\sigma^2_{\psi CM}$ and $\sigma^2_{\psi DM}$ corresponds to a lower tumor amplitude and a larger clutter. Fig. 18 shows a simulation of the errors introduced by phase mismatch for different values of their standard deviation. To better appreciate the magnitude of such errors, the plot is normalized to half-LSB of a 18bit ADC with 2V input range. It is straightforward to note that the error increases rapidly with an increase in $\sigma_{\psi CM,DM}$, and its magnitude is confined in one half-LSB only for phase deviations smaller than few degrees.

The random I/Q phase mismatch is not the only phenomenon that affects the image quality. The synthesizer's phase noise (PN) also acts as a source of errors. Since I and Q signals are supposed to be generated from the same VCO, the phase noise behaves like common-mode I/Q inaccuracies.

To summarize, constant and frequency-independent phase errors are not critical for the tumor detection since they introduce only an error on the evaluation of the tumor position. On the other hand, frequency-dependent phase mismatches and phase noise are critical even for small values of their variance. They enhance the clutter level with respect to the tumor response, leading to a possible failure in the detection of the neoplastic tissue.



(a) (b)

Figure 17: Phase inaccuracies of quadrature LO signals: (a) common-mode phase error and (b) differential-mode phase error.

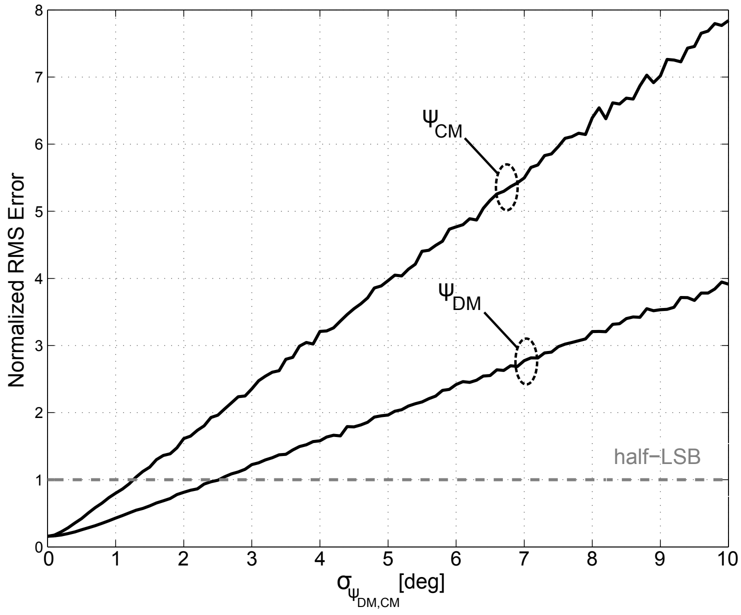


Figure 18: Normalized RMS error introduced by phase inaccuracies versus their standard deviation $\sigma_{\psi CM}$ and $\sigma_{\psi DM}$. The plot is normalized to half-LSB of a 18bit ADC with 2V input range and the simulation refers to the central antenna in the antenna array configuration with a tumor depth of 3cm and a skin-antenna distance of 1cm.

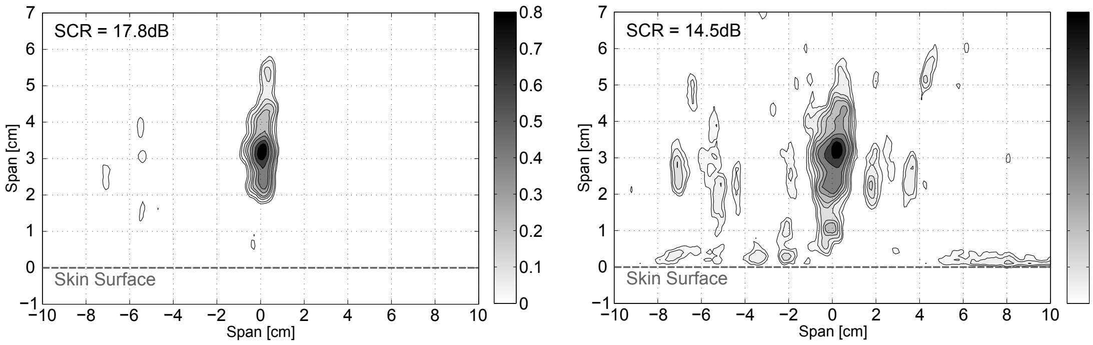
2.5.3 *Architecture Comparison*

In this section, the performance of the two different architecture, i.e. direct conversion and super heterodyne, is compared by generating a simulated tumor image with the same set of impairments. The quality of the reconstructed image is quantified by means of the signal-to-clutter ratio (SCR), defined as the average intensity of the image in the area where the tumor is located over the average intensity of the image elsewhere

$$\mathrm{SCR} = \frac{\sum\limits_{(x,y)\in A_T} I(x,y)/A_T}{\sum\limits_{(x,y)\in A_T^C} I(x,y)/A_T^C} \tag{22}$$

where A_T is the area containing the target and A_T^C is its complementary area. Fig. 19 (a) and (b) show the reconstructed image of a 4mm-diameter target obtained with a direct conversion and a super heterodyne architecture, respectively. With the set of system parameters and impairments presented in Tab. 1, the image SCRs are 17.8dB for the direct conversion and 14.5dB for the super heterodyne. This highlights the robustness of the first architecture with respect to the second one.

To conclude, direct conversion and super heterodyne architectures for SFCW breast cancer detection are compared. The most critical impairment affecting the reconstructed image is the I/Q phase inaccuracies, including the phase noise of the LOs. For this reason, the super heterodyne transceiver seems to be less robust against phase mismatch since it performs two downconversion, each of which introduces errors in the processed signal. Only when the phase errors of the second downconversion are neglected the two architectures show comparable performances. However, even in this case, a direct conversion architecture is preferable due to its simpler implementation that avoids the use of multiple coherent LOs.



(a) Direct Conversion

(b) Super Heterodyne

Figure 19: Reconstructed target image with the two architectures and the same set of system parameters and impairments as in Tab. 1.

2.5.4 *Constraints Mapping Summary*

One of the most challenging system specification arises from the breast tissue properties. The high attenuation at microwave frequencies along with the high reflection experienced by an electromagnetic wave at the air-skin interface, result in a large demanded dynamic range in excess of 100dB. The operating bandwidth is obtained directly from the required imaging resolution of 3mm inside the breast. A bandwidth from 2 to 16GHz accommodates both the high demanded imaging capabilities and the high attenuation at higher frequencies. A similar bandwidth together with the need of a very high

Table 1: Set of System Parameters and Impairments

TX Power	$-15\mathrm{dBm}$
Conversion Gain	$40\mathrm{dB}$
Gain Ripple	$3\mathrm{dB}$
1dB Compression Point	$-30\mathrm{dBm}$
IIP2	$20\mathrm{dBm}$
Noise Figure	$10\mathrm{dB}$
Baseband Bandwidth	$100\mathrm{kHz}$
Phase Inaccuracies	$\sigma_{\psi_{CM,1,2}} = \sigma_{\psi_{DM,1,2}} = 1.5^\circ$
Phase Noise	$-110\mathrm{dBc/Hz@1MHz}$ offset

dynamic range are difficult to address with a pulsed radar architecture. Thus, a Stepped Frequency Continuous Wave radar approach is chosen. The narrow instantaneous bandwidth of this radar allows for a very high dynamic range while preserving the UWB characteristic of the system.

Another specification related to the dynamic range is the ADC resolution. An effective ADC resolution in excess of 17bit is required to handle both the tumor response and the skin backscatter. Since commercial high-resolution ADCs don't have a very high bandwidth, the baseband frequency needs to be low. This, together with the results highlighted in Section 2.5.3, makes the direct conversion architecture the best candidate for this application.

Without loss of generality, setting the transmitted power to $-14\mathrm{dBm}$, the high skin reflection sets the minimum P_{1dB} of the receiver to $-34\mathrm{dBm}$. Moreover, the weak tumor response around $-134\mathrm{dBm}$ (c.f. Fig. 12) sets the maximum allowable noise figure to $10\mathrm{dB}$ with a noise bandwidth of $1\mathrm{KHz}$ (that of the ADC).

The most critical impairments of a direct conversion receiver are the DC offset, the flicker noise and the second-order distortion. In the proposed system, the DC offset is calibrated out as discussed in Section 5.2.3.2 while the flicker noise is mitigated adopting the chopper stabilization technique. The IIP2 is specified to be greater than $10\mathrm{dBm}$ as discussed in Section 2.5.2.3.

The real resolution of the reconstructed image depends strongly on the phase inaccuracies of the system. To this regard, the requirement on the I/Q phase mismatch of the local oscillator is specified to be less than 1.5° over the entire bandwidth (c.f. Section 2.5.2.4). This is the most challenging specification of the entire transceiver.

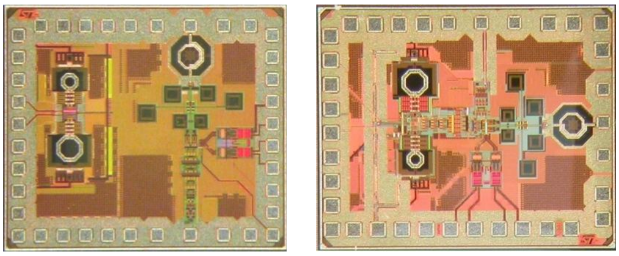
3

TRANSCEIVER DESIGN

This chapter describes the design of two IC prototypes, named SKuRAD1 and SKuRAD2 (Fig. 20), tailored for breast cancer diagnostic imaging. As compared to similar circuits, the presented system addresses some design challenges. First of all, it operates from S to Ku band, thus covering 3 octaves. Second, the large backscatter of the skin acts as an in-band interferer that coexists with the weak tumor echo. This calls for a large instantaneous dynamic range. Then, since the imaging process is essentially based on phase measurement, the quadrature error and phase noise have to be as small as possible and constant over the whole bandwidth. Finally, the narrow baseband introduced by the Stepped Frequency approach requires an ultra-low fliker noise corner.
The first prototype, SKuRAD1, consist of the complete direct conversion receiver. It is composed by a wideband LNA, a linearized transconductor, a current-mode passive mixer and a chopped TIA as the baseband conditioning circuit. The quadrature LO signal is generated by a reconfigurable frequency divider by $1, 2$ or 4 starting from an external signal that spans the higher octave. For testing purposes, SKuRAD1 contains, moreover, a first version of the VCOs that will be implemented in SKuRAD2. The author's main contribution include the design of the programmable frequency divider, the design of the input test buffer used to feed it with an external signal and the design of the output test buffer used to verify the correct operation of the divider in the frequency range of interest. The second prototype, SKuRAD2, is the complete radar transceiver. It essentially contains the same receiver as in SKuRAD1 (with minor changes in the signal path) with an improved version of the frequency divider. Then an integer-N PLL generates all the signals in the higher octave and a harmonic-rejection output buffer drives the output antenna. The author's main contribution for this IC include the re-design of the improved frequency divider as well as the design of the harmonic rejection output buffer.

3.1 THE CHOICE OF THE TECHNOLOGY

The target of this work is the realization of an ultrawideband radar tailored for the breast cancer diagnostic imaging. As stated in the previous sections, the microwave characteristics of the human body together with the required resolution for this application, results



(a) SKuRAD1 (b) SKuRAD2

Figure 20: Microphotograph of SKuRAD1 and SKuRAD2.

in a 14GHz bandwidth and a very high demanded dynamic range. To achieve these performances, the system must feature a flat conversion gain in a very large bandwidth and must exhibit a low noise figure. A low flicker noise is also important to avoid to corrupt the desired DC signal. The most stringent specification, however, is the maximum tolerable I/Q phase mismatch of 1.5° over the entire bandwidth.

As will be presented later in this chapter, the proposed LO generation chain is made of a PLL that covers the higher octave ($8-16$GHz) followed by a programmable frequency divider which can divide by 1, 2 or 4 and generates the quadrature signals over the entire 3 octaves. The programmable frequency divider is definitively the most critical block of the design. It must be fast enough to cover with margin the higher octave and to accurately generate the quadrature signals.

A 65nm CMOS technology is used in this design as it features an adequate f_T to enable the operation of the circuits in the band of interest.

3.2 RECEIVER - SKURAD1

This section describes the design of the first integrated circuit, named SKuRAD1, tailored for breast cancer diagnostic imaging. Its block diagram is shown in Fig. 21. To amplify the weak tumor backscatter, it uses a wideband LNA followed by a linearized transconductor. Then a current-mode passive mixer downconverts the signal while a chopped Transimpedance Amplifier (TIA) drives an external $\Sigma\Delta$ ADC. The quadrature LO signal in the $1.75-15$GHz range is obtained by means of a programmable frequency divider by $1, 2$ or 4 (named DQG) which is fed by an external signal in the $7-15$GHz range. An input test buffer interfaces the external LO input signal with the frequency divider and an output test buffer allows to verify the correct operation of the DQG. The last two blocks are used only for test purposes.

3.2.1 *Low Noise Amplifier (LNA)*

The Low Noise Amplifier is the first stage of the receiver chain. It must provide good input matching and high gain while featuring a low Noise Figure. Due to the instantaneous narrow bandwidth of the Stepped Frequency approach, more than one LNA architecture is possible. One of them can use a set of switchable narrowband LNAs centered at different frequencies. This solution can be very simple but it occupies a large area. Another solution can use a single reconfigurable narrowband LNA, but in this case the presence of an additional tuning line makes the design less robust and difficult.

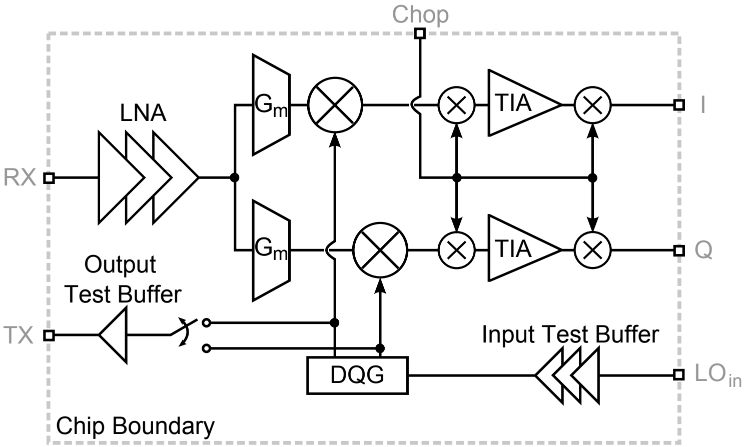


Figure 21: SKuRAD1 block diagram.

The proposed solution uses a cascade of three sections to instantaneously cover the entire bandwidth. The first stage is responsible for input matching and noise figure. Since a reactive input matching network is not recommended due to the high fractional bandwidth and the relatively low lower frequency, a noise cancelling approach is used. This solution allows to decouple the input matching from the noise figure, exploiting the simultaneous noise and power matching [12]. Fig. 22 depicts the proposed noise cancelling LNA, which is composed by a common-gate (CG) and a common-source (CS) stage. The noise generated from transistor M_1 is added in phase opposition at the output nodes without impairing the useful signal when $|Z_{CG}| = |Z_{CS}|g_{m2}R_s$, where R_s is the source impedance. In this solution, the combination of the input inductor $L_{in} = 520pH$ and the common-gate input impedance results in a good input matching over almost 4 octaves, from 1.5 to 20GHz. Moreover, it takes advantage of the topology to perform the single-ended to differential conversion without the need of an additional balun. The bias current of the CG and CS is 2mA and 7mA respectively while the MOS dimensions are $W_1 = 40\mu m/L_1 = 0.06\mu m$ and $W_2 = 80\mu m/L_2 = 0.06\mu m$. This arrangement translates into $|Z_{CG}|/|Z_{CS}| \approx 3$. A good cancelling matching is obtained by implementing resistance R_{CS} as a parallel combination of three resistors of value R_{CG}.
The second and third stage of the LNA are visible in Fig.23 and are, respectively, a differential and a pseudo-differential pair. This choice allows to improve both signal balance and linearity. The bias current is, 6mA and 12mA.
All three stages use shunt-peaked load to widen the bandwidth. The gain of the three stages are 13dB, 7dB and 2dB respectively with an additional 8dB peaking around 17GHz. This is used to equalize the complete LNA response and expand even more the bandwidth. Since each shunt-peaked load has intrinsically a low quality factor, for a compact layout each inductor (except for the input inductor L_{in}) is made by stacked square coils.

3.2.2 *Low 1/f Downconverter*

Resistively-degenerated transconductance (G_m) stages are used in the I/Q paths to convert the LNA output voltage into current, as shown in Fig. 24. Each G_m stage is biased with 8mA, and makes use of a $R_{deg} = 46\Omega$ degeneration resistor. Self-biased active loads are employed: this configuration avoids the need of an auxiliary common-mode

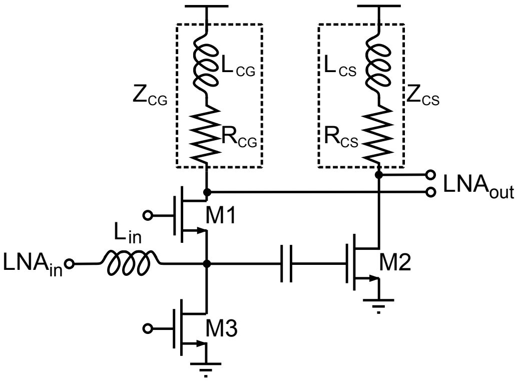


Figure 22: Noise Cancelling LNA. Biasing not shown.

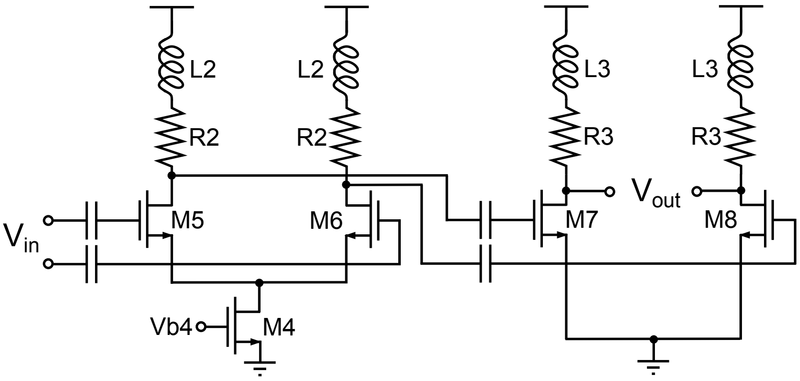


Figure 23: Second and third stage of the LNA. Biasing not shown.

feedback control loop.

Current-mode passive mixers are capacitively coupled to the transconductor outputs. This choice results in both good linearity and good noise performance, preventing the flicker noise of the commutating devices to corrupt the downconverted signal [16]. A large and constant swing of the LO signal across the band is essential to achieve good mixer performance. The proposed DQG plays a key role in this, as discussed in Section 3.2.3.

The use of passive mixers is not sufficient to address the high flicker noise of MOS transistors. Typically, current-mode mixers are loaded by baseband transimpedance amplifiers (TIAs), based either on common-gate stages or on op-amps with resistive feedback. The flicker noise of the devices of the TIAs is not suppressed, ultimately setting the flicker noise corner of the receiver. To overcome this limitation, the chopper stabilization technique is used to reduce the flicker corner below 100 Hz. Chopper stabilization is a widespread technique, usually applied to voltage amplifiers [22, 21, 6, 92]. Its use with TIAs in a downconversion mixer is, however, unprecedented. The combination of passive current-mode switches and chopper stabilized TIAs results in a highly linear, low noise downconversion mixer with a very low flicker noise corner.

The schematic of the proposed TIA is shown in Fig. 25. The amplifier is based on a common-gate stage. Compared to an op-amp with resistive feedback approach, this choice allows to decouple the input and output common-mode voltages. As a consequence, the input common-mode voltage can be kept low, which is beneficial for the mixer switches (nMOS transistors), without impairing the output swing. Local feedback (transistors M3 and M8) is used around the common-gate input stage (transistors M2 and M9) to decrease the differential TIA input resistance, $R_{in,TIA}$, as

$$R_{in,TIA} \approx \frac{2}{g_{m2} g_{m3} r_{01}}. \tag{23}$$

The input branches of the TIA are biased with 250μA each, such that a differential input resistance of 35Ω is achieved at a small power consumption. The input currents are mirrored to the output branches where resistors R perform the current-to-voltage conversion.

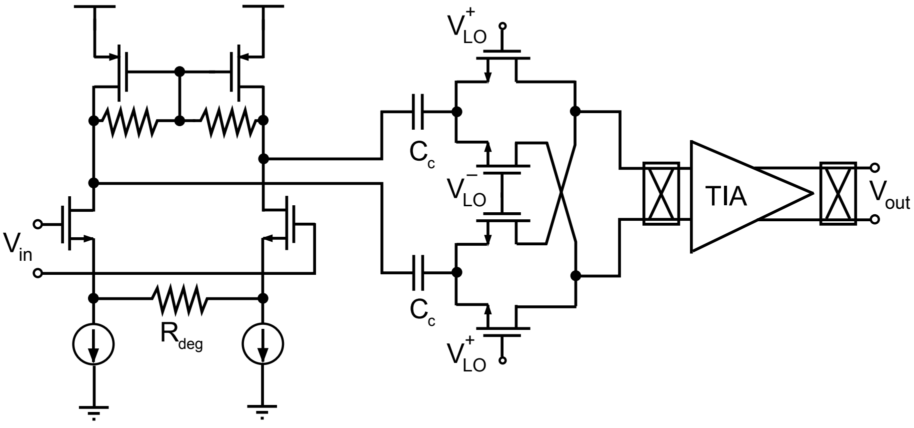


Figure 24: Schematic of one path of the quadrature downconverter.

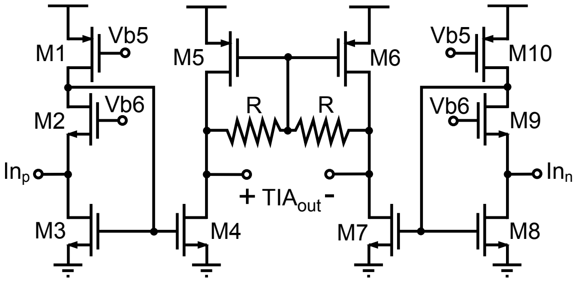


Figure 25: Schematic of the transimpedance amplifier (TIA). Biasing not shown.

3.2.3 *Frequency Divider and Quadrature Generator (DQG)*

As discussed, the local oscillator (LO) quadrature accuracy is the most stringent specification for a receiver tailored for stepped-frequency microwave imaging. The quadrature error must be small, and constant over the entire wide receiver bandwidth. Sudden changes in the I/Q phases cannot be tolerated, even if they occur for few frequencies in the wide covered span.

Accurate generation of quadrature signals over multiple octaves can be achieved by using static frequency dividers by two. However, this technique cannot be used in the proposed radar receiver because of the high frequencies involved. Apart from the power consumption of the divider yielding the frequencies for the higher octave, the generation of the LO signals at twice the frequency, i.e. from 15 to 30GHz, with extremely low phase noise (also a sensitive specification for the system [8]) and large tuning range, would re-

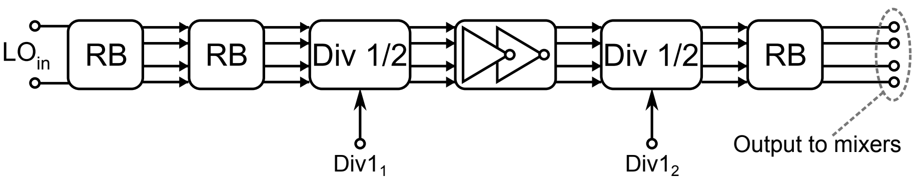


Figure 26: Block diagram of the proposed programmable frequency divider/quadrature generator (DQG).

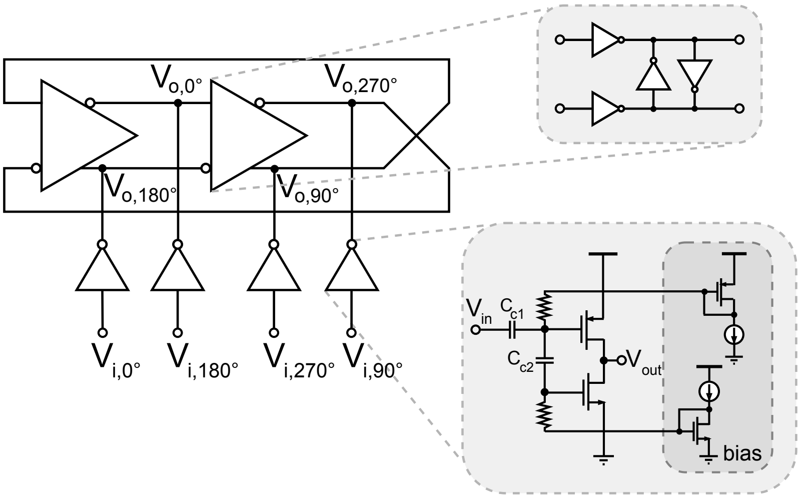


Figure 27: Simplified schematic of the regenerative buffer (RB).

quire many power hungry VCOs to meet the requirements. The use of a polyphase filter to generate the I/Q phases in the higher octave is also a possibility. To meet the required quadrature accuracy over one octave while being robust to process spreads, the filter should feature more than three sections, thus introducing more than 18dB losses. Since a large LO swing is required by the mixer switches, buffers would be needed to drive the polyphase filter and to regenerate the signal after it. Simulations suggest that such buffers would consume as much current as the entire proposed DQG. In addition, the LO signal would be tapped from different points of the circuit to cover the various octaves. As a consequence, the feed to the mixer could be uneven across the band in amplitude and, most importantly, in phase.

The proposed solution is able to address all the aforementioned issues. It is composed by a cascade of two programmable injection-locked dividers. Each divider can divide by 1 (no frequency division) or 2 depending on one configuration bit. A PLL (not implemented in SKuRAD1) is supposed to generate signals over the higher octave, namely from 7.5 to 15GHz. The DQG is then capable of producing quadrature signals over three octaves starting from the PLL output.

The block diagram of the DQG is shown in Fig. 26. Two regenerative buffers (RBs), based on injection locked ring oscillators, drive the first programmable divider. An interstage buffer made of two-stage tapered CMOS inverters interfaces the two programmable dividers. The interstage buffer is AC-coupled to the output of the first programmable divider, and the input inverter is biased at its logical threshold by means of replica biasing. At the end of the chain, another regenerative buffer is used to drive the mixers. The injection locked regenerative buffer intrinsically operates at large output swings, hence providing a large drive to the mixers with minimum amplitude variations across the band. The interface between the LO distribution and the mixers is the same regardless the DQG is dividing by 1, 2, or 4. This avoids discontinuities in the operation of the DQG due to changes in the loading of the LO distribution chain. The architecture of the DQG, made of a cascade of several injection-locked stages, has the advantage of progressively improving the quadrature accuracy [44], such that every stage contributes to reduce the quadrature error in any used configuration. Moreover, the use of injection locked circuits based on inductorless ring oscillators results in very wide locking ranges [80]. As a consequence, the DQG does not need any calibration nor tuning.

The schematic of the regenerative buffer is shown in Fig. 27. The core of the circuit is a two-stage differential ring oscillator in which the delay cells are differential static CMOS latches with input buffers as injection elements. Although the RB is basically a digital circuit in its structure, a full custom design is needed to guarantee the correct operation up to 15GHz. Analog techniques are also required. An example is given by the injection buffers of the RB, shown in Fig. 27. The buffers are essentially CMOS inverters. However, to make them operate correctly in the required frequency range, even in presence of input signals with less than rail-to-rail swing, AC-coupling through capacitors $C_{C1} = 310\text{fF}$ and $C_{C2} = 120\text{fF}$ is employed, which makes the inverters work as analog amplifiers. This is similar to the approach reported in [53]. Note that two decoupling sections are used in cascade, as opposed to connecting one terminal of both and directly to the input. The chosen arrangement in fact reduces slightly, but effectively, the capacitive loading on the driving stage. Moreover, it allows for a more compact layout since the smaller can be conveniently placed in the neighborhood of the pull-down nMOS, leaving more space for the larger. The bias voltages of the nMOS and pMOS transistors are obtained by means of current mirrors, shared among the buffers.

The schematic of the programmable divider is shown in Fig. 28. Similarly to the RB, the programmable divider is built around a two-stage differential ring oscillator. The topology of the delay cell is also similar (cf. Fig. 28), although the transistor size is differently optimized in each block. The possibility of having a programmable divider is based on the multiphase injection locking concept [17]. Depending on the phase progression of the signals fed to the divider, harmonic or super-harmonic injection locking occurs, enabling either division by 1 (same input and output frequency) or frequency division by 2. Different division ratios are hence obtained by reconfiguring the injection network, as shown in Fig. 29. In the divide-by-one mode, a complete quadrature sequence (0°,90°,180°, and 270°) must be injected at the four nodes of the ring oscillator. Consequently, nodes "A" (cf. Fig. 29) are grounded and quadrature phases are injected into the ring oscillator through pseudo-differential pairs. As shown in Fig. 28, the pull-up transistors of the delay inverters of the ring oscillator are effectively made larger, as compared to the divide-by-two configuration, to counteract the undesired pull-down effect of the injection devices (M_{j1} through M_{j4}) in Fig. 29. The latter would in fact tend to decrease the output common mode voltage of the ring oscillator, and in turn the oscillation amplitude. In the divide-by-two mode, nodes "A" in Fig. 29 are floating. A signal with 0° phase is fed to both injection devices M_{j1} and M_{j2}, that thus operate as a single transistor connected across the output nodes of one of the delay cells of the ring oscillator. Similarly, a signal with 180° phase is fed to injection devices M_{j3} and M_{j4}. Such a direct injection arrangement enables superharmonic injection-locking operation [80], and consequently frequency division by 2. The injection devices M_{j1} through M_{j4} are AC-coupled to the phase distribution multiplexers, which are built out of tri-state CMOS gates. The DC bias voltage fed to the injection transistors is tailored for divide-by-1 and divide-by-2 operation. It is important to emphasize, however, that these bias voltages are set by design, and that no tuning is required for the DQG to operate over three frequency octaves.

The frequency divider is supposed to be driven by an integrated PLL which generates signals over the higher octave. However, in the first radar prototype (SKuRAD1), the PLL has not been implemented. Thus, an input buffer has been designed to interface the differential frequency divider inputs with an external single-ended signal generator (cf. Fig. 21). This buffer is made by a cascade of three resistively loaded differential and pseudo-differential pairs.

A single common-drain output buffer (cf. Fig. 21) has been designed to verify the locking extrema of the DQG and measure the amplitude mismatch of the four phases. Four pass-transistors are used to connect the four DQG output signals to the single output buffer. Since this buffer is for testing purposes only, a high performance is not needed here. Hence, to avoid to introduce large parasitics to the frequency divider outputs, the pass-transistors are very small and are placed close to the mixers. The bias of the buffer is programmable, such that it can be turned off without corrupting the normal operation of the DQG.

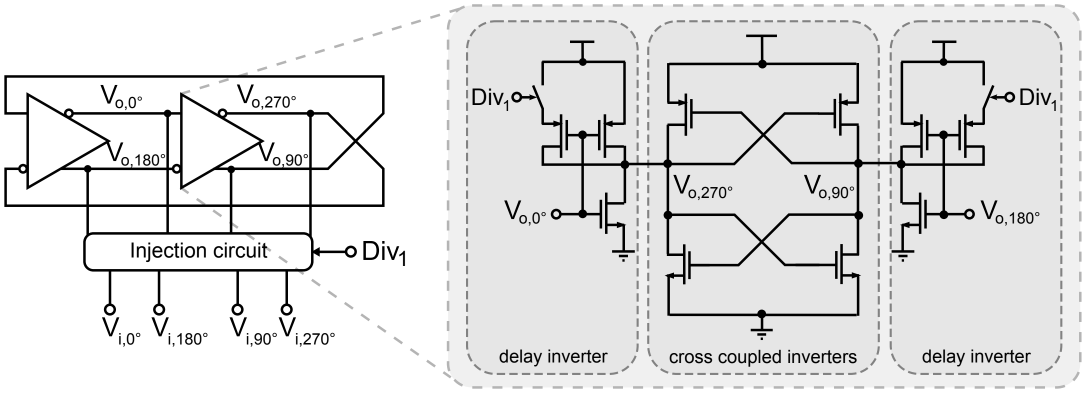

Vo,0°
Vo,270°
Vo,180°
Vo,90°
Injection circuit
Div1
Vi,0°
Vi,180°
Vi,90°
Vi,270°
Div1
Vo,0°
Vo,270°
Vo,90°
Div1
Vo,180°
delay inverter
cross coupled inverters
delay inverter

Figure 28: Simplified schematic of the proposed programmable frequency divider by 1 or 2 with a detailed schematic of the delay cell.

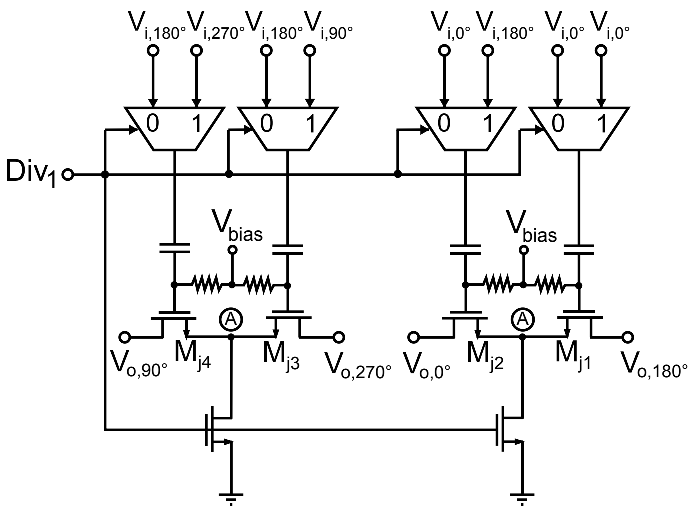

Vi,180°
Vi,270°
Vi,180°
Vi,90°
Vi,0°
Vi,180°
Vi,0°
Vi,0°
0 1
0 1
0 1
0 1
Div1
Vbias
Vbias
A
A
Vo,90°
Mj4
Mj3
Vo,270°
Vo,0°
Mj2
Mj1
Vo,180°

Figure 29: Simplified schematic of the injection network of the programmable divider.

3.3 TRANSCEIVER - SKURAD2

This section describes the design of the second radar prototype, named SKuRAD2, tailored for breast cancer diagnostic imaging. Its block diagram is shown in Fig. 30. Concerning the receiver chain, only small changes have been done with respect to the previous design. These include the LNA biasing circuit and the correction of a mistake in the connections between the mixers and the TIAs (there was a small layout difference in the I and Q connection to the TIAs). The programmable frequency divider is completely new and is capable to work at higher frequencies compared to the previous design while consuming less power. The frequency divider is then fed by an integer-N PLL which generates all the signals in the higher octave (i.e. from 8 to 16GHZ). Finally, a Harmonic Rejection TX buffer drives the TX antenna. Notice that SKuRAD2 represent the complete transceiver and, hence, it can be used to perform some realistic imaging experiments (Sec. 5.2).

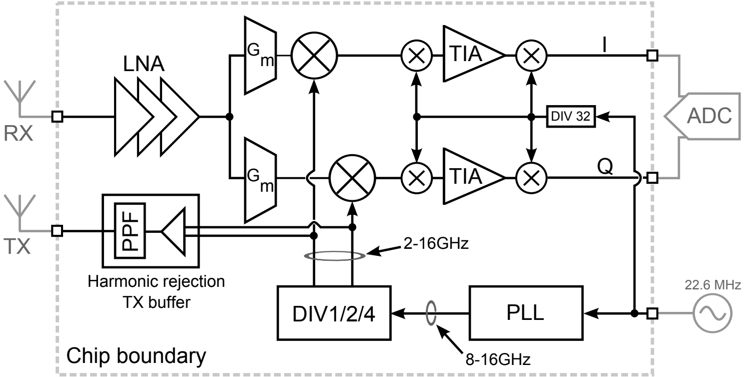


Figure 30: SKuRAD2 block diagram.

3.3.1 *Integer-N Phase Locked Loop (PLL)*

The frequency synthesizer has to generate all the signals in the $8 - 16\text{GHz}$ range while having good phase noise performance over the entire bandwidth. The proposed solution consists of an integer-N PLL locked to a 22.6MHz reference (Fig. 31). It relies on two VCOs not to trade the phase noise performance for the tuning range. Each VCO is followed by a prescaler by 4, such that multiplexing between the two PLL feedback signals is implemented at a lower frequency. The PLL loop is then closed by means of a current steering Charge Pump (CP) and a third order Loop Filter (LF). Both of them contribute to reduce reference spurs.

3.3.1.1 *Voltage Controlled Oscillator (VCO)*

The two VCOs are differential LC oscillators (Fig. 32) with nMOS cross-coupled pair as negative resistance element and pMOS as tail current generator connected to the center tap of the tank inductor. Each tank is optimized for a correct operation in the lower and higher frequency band. To maximize the quality factor, each inductor is an octagonal single-turn thick-metal coil (this technology does not allow circular shapes). The corresponding inductance value is 350pH and 180pH for the lower and higher band VCO respectively.

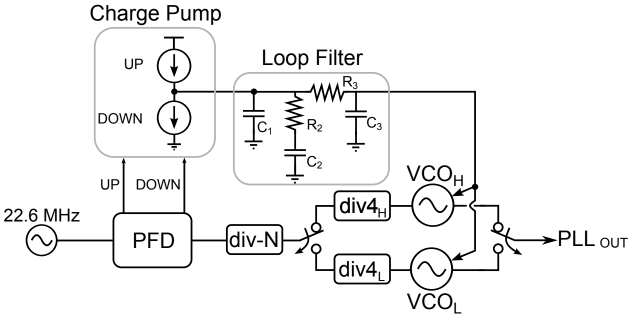


Figure 31: Frequency synthesizer block diagram.

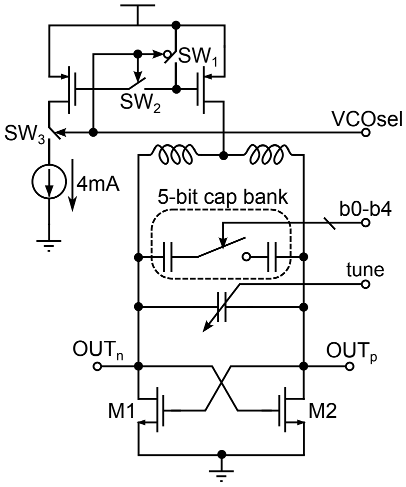


Figure 32: Schematic of one differential LC oscillator.

Tuning is achieved by a 5-bit binary-weighted switched-capacitor bank and a small MOS varactor for continuous tuning. The unity cell of the capacitor bank is visible in Fig. 33. It is composed by a series of 2 MIM capacitors and an nMOS M_{SW}. When the control voltage $V_b = 0V$, the nMOS is OFF and hence the differential capacitance offered by the cell is roughly $C_{par}/2$ (assuming $C \gg C_{par}$), where C_{par} is the parasitic capacitance at nodes A and B. Otherwise, when $V_b = V_{DD}$, the nMOS acts as a closed switch and the differential capacitance become $C/2$. The width of transistor M_{SW} is choosen as a compromise between quality factor and tuning range [79]. The larger the switch, the higher the quality factor but the lower the C_{max}/C_{min} ratio due to the bigger parasitic capacitances. The presence of transistors M_{P1},M_{P2},M_{N1} and M_{N2} ensures the correct DC voltage across the switch. When $V_b = V_{DD}$, they set the source and drain voltage to $0V$, allowing the switch to turn on in a correct way. Otherwise, when $V_b = 0V$, they are used to set the drain and source DC voltage to V_{DD}. This reduces the parasitic capacitance C_{par} by biasing the drain-bulk and source-bulk junction of M_{SW}.

In order to allow to turn on just one VCO at a time, control switches are present in the bias network. When $VCO_{sel} = V_{DD}$, SW_3 and SW_2 are closed while SW_1 is open. In this case the bias current is correctly mirrored with a mirror ratio of 3.5 and 5 for the VCO_L and VCO_H respectively. When $VCO_{sel} = 0V$, SW_3 and SW_2 are open, SW_1 is closed and the VCO is turned OFF.

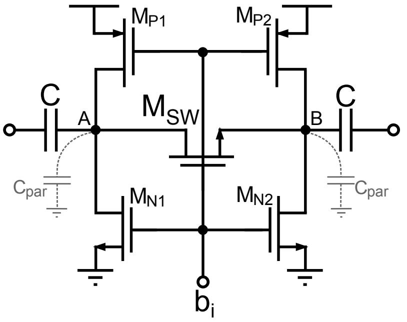


Figure 33: Unity cell of the capacitor bank.

3.3.1.2 *Charge Pump and Loop Filter*

The charge pump is the key element of a PLL design. A simplified diagram is shown in Fig. 34. It is composed by two current sources controlled by the Phase-Frequency Detector (PFD) which inject and remove a charge into the loop filter (LF). The width of UP and DOWN control signals determine whether the net charge is injected or removed from the LF. This causes an increase or decrease of the output voltage V_{LF}. Ideally, when the lock condition is reached, UP and DOWN pulses have the same width resulting in a zero net charge injected in the filter.

However, when implemented at circuit level, both PFD and charge pump show non-idealities that reduce the PLL performance. The main unwanted effect is the presence of reference spurs caused by mismatches between I_{UP} and I_{DOWN} or by charge sharing [15], charge injection and clock feedthrough.

The mismatch between charging and discharging current usually occurs due to the finite output impedance of current sources caused by the channel length modulation of deep submicron devices. This leads a non-zero charge injected in the filter even when the loop is in lock condition. Moreover, the charge stored in the channels of the switch transistors reaches the output node when they are turned ON or OFF, leading to a charge injection error. Finally, charge sharing between parasitic capacitances can occur when the MOSFET are switched ON.

A schematic of the proposed charge pump is depicted in Fig. 35. Various techniques are employed to minimize the generation of reference spurs. A current steering topology is adopted, with a charge pump current equal to $I_{CP} = 500\mu A$. The use of two complementary branches allows the I_{UP} and I_{DOWN} currents to continuously flow through the charge pump. Since the current flowing through transistors M_{P1} and M_{N1} is kept constant, the voltage variations at nodes A and B are minimized. As a consequence, the charge sharing from nodes A and B to the output node V_{LF} is drastically mitigated. A unity gain configuration op-amp is used to force the voltage of node C in the auxiliary branch at the same level of the output node V_{LF}. To minimize the mismatches between the charging and discharging currents I_{UP} and I_{DOWN}, an additional op-amp is used to ensure that nodes C and D are at the same voltage level. The amplifier forces the I_{UP} and I_{DOWN} currents to be equal, in the limit of transistor mismatches. A relatively large capacitor is required to guarantee the stability of the loop. In this design, $C_{stab} = 24.8pF$ ensures a phase margin of 70° across PVT. Transistors M_{P3}, M_{P5}, M_{N2} and M_{N4} are driven by complementary phases and are used as dummy switches to decrease the undesired charge injection at the output node and at node C when devices M_{P2}, M_{P4}, M_{N3} and M_{N5} are turned off.

To achieve an even lower spur level, the PLL loop filter (LF) is a third order design, Fig. 36. It is useful to filter out spurs or noise generated by the PLL at frequencies ten times the loop bandwidth. All the filter components are integrated. The value of capacitors $C_1 = 1.8\text{pF}$ and $C_2 = 58.3\text{pF}$ and resistor $R_2 = 11\text{k}\Omega$ are chosen to set the PLL loop bandwidth (1MHz) and phase margin (60°), while the value of capacitor $C_3 = 660\text{fF}$ and resistor $R_3 = 30\text{k}\Omega$ are set as a compromise between higher out-of-band attenuation (and thus spur reduction) and lower noise generated by R_3.

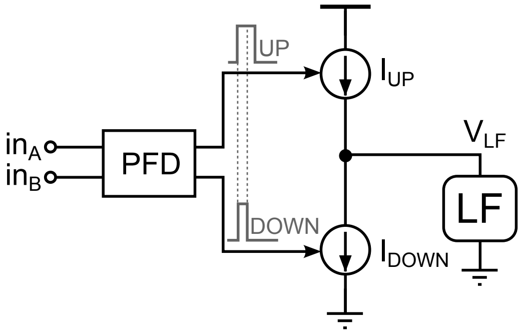

UP
I_{UP}
V_{LF}
in_A
in_B
PFD
LF
DOWN
I_{DOWN}

Figure 34: Conceptual block diagram of a simple charge pump.

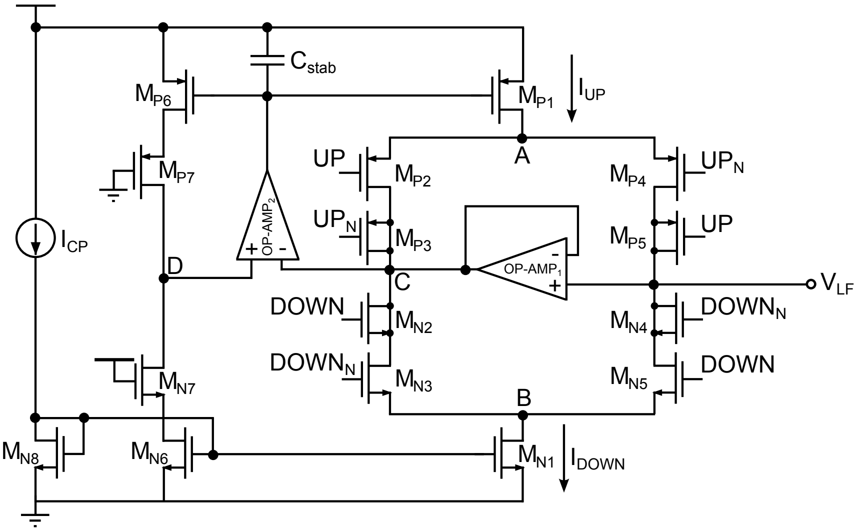

C_{stab}
M_{P6}
M_{P1}
I_{UP}
M_{P7}
UP
M_{P2}
A
M_{P4}
UP_N
$OP\text{-}AMP_2$
UP_N
M_{P3}
M_{P5}
UP
I_{CP}
D
$OP\text{-}AMP_1$
C
V_{LF}
DOWN
M_{N2}
M_{N4}
$DOWN_N$
$DOWN_N$
M_{N3}
M_{N5}
DOWN
M_{N7}
B
M_{N8}
M_{N6}
M_{N1}
I_{DOWN}

Figure 35: Schematic of the proposed charge pump.

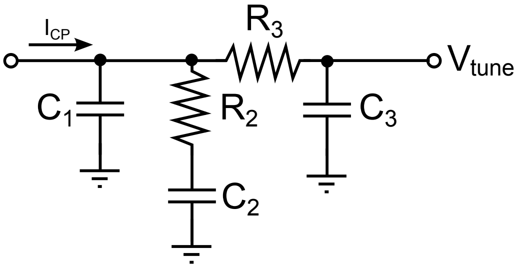

I_{CP}
R_3
V_{tune}
C_1
R_2
C_3
C_2

Figure 36: Schematic of the proposed third order loop filter.

3.3.1.3 *Prescaler*

A prescaler by 4 is used to relax the design of the programmable divider and to multiplex between the two feedback path at a lower frequency. It is based on injection locking on a four-cells ring oscillator and is similar to the design presented in [81], as sketched in Fig. 37. Each cell is a differential CMOS inverter having nMOS as pseudo-differential pair and pMOS as cross-coupled load. The injection method is based on the direct injection mechanism [78] enabled by nMOS connected across the output terminals of each cell. To widen the locking range, a multi-phase injection technique is adopted [17]. Concerning this, the use of a 4-cells ring oscillator requests a differential input signal which is simply available at the VCO output nodes.

The size of the transistors of the inverter cell is different in the two prescalers in order to adapt the self oscillation frequency of the ring oscillator to the output frequency of each VCO. It is $5/0.08\mu m$ and $5/0.06\mu m$ for the low and high band prescaler (inside the same cell, nMOS and pMOS have the same size). The size of the injection transistor M_{inj} is, instead, the same for both designs and is $5/0.06\mu m$. Finally, a switch connects each delay cell to V_{DD} and allows to turn OFF the prescaler when the respective path is not used. Otherwise, without an injection signal the ring oscillator would oscillate at its self-oscillation frequency and this may corrupt the signal in the other path or increment the output spur level.

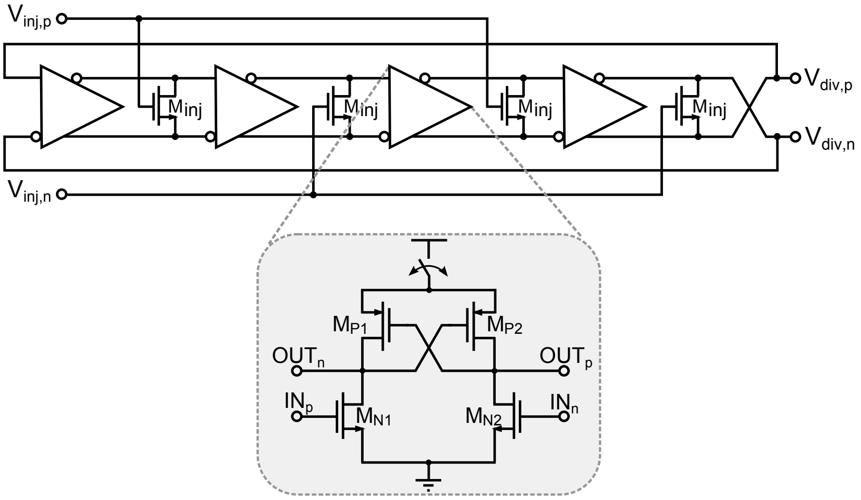


Figure 37: Schematic of the proposed injection-locked prescaler by 4 with a detailed view of the delay cell.

3.3.1.4 *Low-Frequency Programmable Divider*

The programmable divider is based on a modular dual-modulus architecture like in [82] and is composed by a chain of 7 2/3 divider cells. The complete schematic is sketched in Fig. 38. The 2/3 divider cell divides the frequency of the input signal either by 2 or 3 depending on the logic level of signals p_i and M_i. The M_i signal becomes active only once in a division cycle and is propagated back in the chain regardless of the value of p_i input. When M_i becomes high, the state of the input is checked and, if p_i = "1", the 2/3 cell is forced to swallow one extra period of the input signal, thus dividing by 3.

A chain of n 2/3 cells is able to implement a frequency divider of any integer modulo from 2^n to $2^{n+1}-1$. The division range is thus limited to roughly a factor of two, which

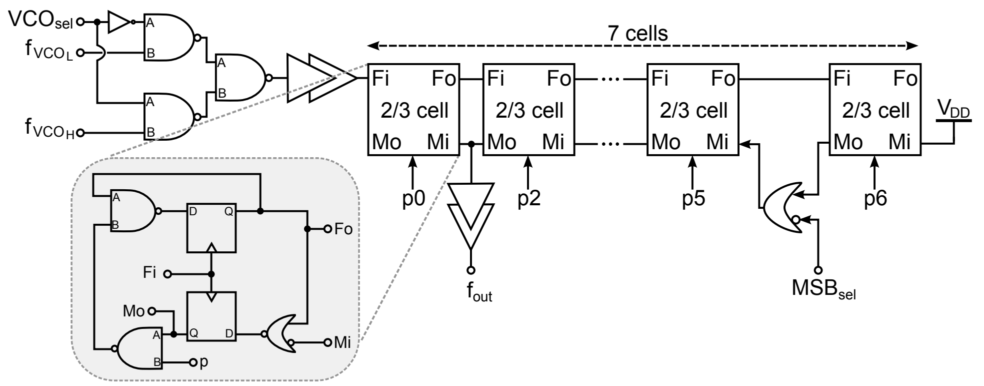


Figure 38: Schematic of the programmable frequency divider used in the PLL loop.

is not enough to cover with margin the 1-octave tuning range of the PLL. In order to extend the division range, a simple OR gate is added to the schematic. When $MSB_{sel} = "0"$ the M_i input of the sixth cell becomes high regardless of the output of the next cell. In this way, the chain behaves like a $n_{min} = 6$ cell frequency divider and hence the minimum and maximum division factors become unrelated [85]. By choosing $n_{min} = 6$ and $n_{max} = 7$ a division factor ranging from $N_{min} = 64$ to $N_{max} = 255$ is obtained. This means that, taking into account the division by 4 introduced by the prescaler, the covered frequency range is $[4f_{REF}N_{min} \quad 4f_{REF}N_{max}] = [5.78GHz \quad 23GHz]$ which is more than enough to cover 1 octave with some margin for PVT variations.

The schematic of the single 2/3 cell is visible in the inset of Fig. 38. It is made of two D-type flip flop implemented in TSPC logic. This allows to avoid additional inverters that would make the design operate at much lower frequencies. A multiplexer realized as a cascade of NAND gates is added in front of the programmable divider in order to choose between the two prescaler outputs, depending on which VCO is turned ON.

3.3.2 *Improved Frequency Divider and Quadrature Generator (IDQG)*

The LO frequency divider is the most critical block of the design. It generates all the quadrature signals from 2 to 16GHz with a small I/Q phase error. SKuRAD1 prototype uses a chain of two injection-locked programmable dividers to achieve the desired performance. Each divider can divide by 1 or 2, obtaining a total maximum frequency division of 4. In this way, the LO chain generates quadrature signals in the range $1.75 - 15GHz$.

The solution proposed in SKuRAD2 is based on the same idea. The VCOs generate differential signals which are fed to an improved version of the programmable frequency divider by means of tri-state gates. A block diagram of the frequency divider is shown in Fig. 39. A chain of 3 regenerative buffers (RB - the same regenerative buffer implemented in SKuRAD1) interfaces the PLL output with the divider core; one more RB is used as buffer to the mixer and the transmitter output. The divider core is the innovative solution of this design. It is based on injection locking on a 4-stage differential ring oscillator (see Fig. 39 and Fig. 40). Leveraging the multi-phase injection technique, and reconfiguring the injection network, the ring oscillator is forced to lock to the fundamental PLL frequency, or to half the fundamental, or to one fourth of it. As a consequence, in a single stage, division by 1, 2, or 4 is achieved. This arrangement proves to be more

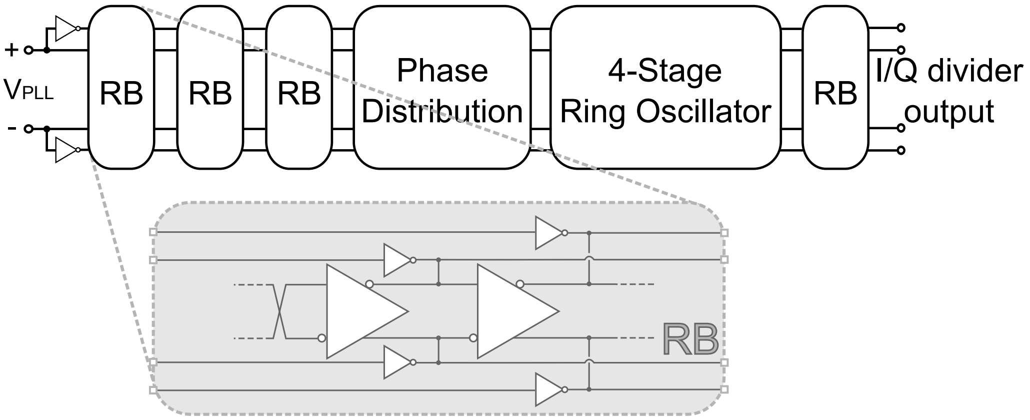
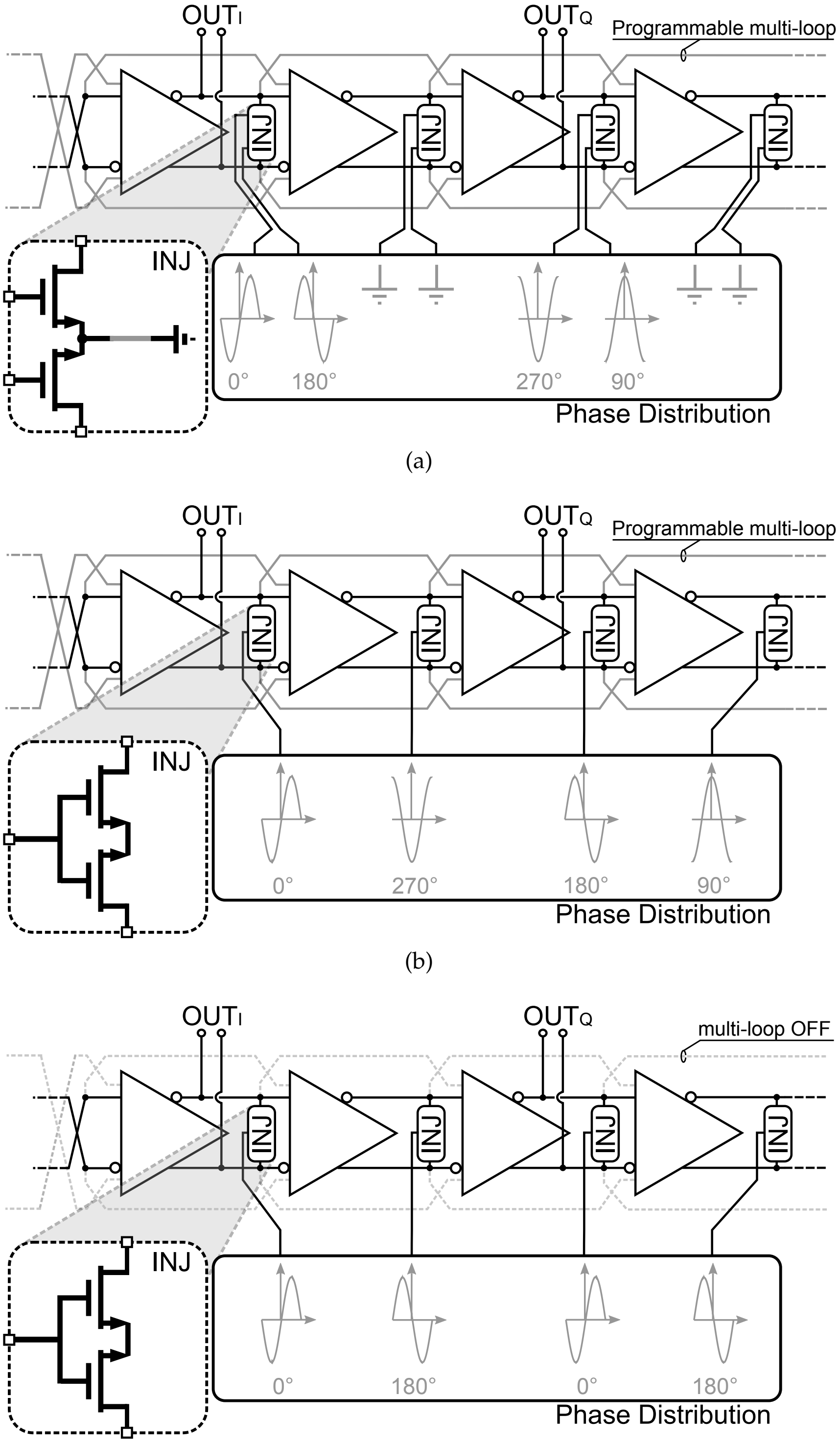


Figure 39: Block diagram of the proposed programmable frequency divider (IDQG).

robust and to be able to operate at higher frequencies with respect to a solution made of a cascade of two dividers by 1 or 2, as proposed in SKuRAD1.
If a correct phase sequence is injected in multiple points of a ring oscillator, the locking range is widened [17]. Conversely, a wrong phase sequence results in a very narrow locking range, and injection locking is unlikely to take place. Therefore, a ring oscillator injected with signals at a given frequency will select, among different possible modes of operation, the one that matches the provided input phase sequence. In the differential 4-stage ring oscillator used in this work, the phase difference between the input of each delay cell and the corresponding non-inverting output is 45°. Hence, the output nodes of the ring oscillator are in an octet-phase sequence. To force locking at the fundamental frequency (divide-by-1 mode), the injection network is configured as a pseudo-differential pair that injects quadrature signals into alternate delay cells, as shown in Fig. 40(a). In divide-by-2 mode, the octet-phase sequence at the output corresponds to a quadrature sequence at the divider input. In this case, the injection network is reconfigured to operate as a single device with drain and source connected between the output nodes of the differential delay cell (direct injection), as shown in Fig. 40)(b). Consequently, the injection network operates as a mixer and super-harmonic injection occurs [80]. Finally, in divide-by-4 mode, the octet-phase sequence at the divider output corresponds to a differential sequence at the divider input (see Fig. 40(c)). Thus, differential phases are fed to the injection networks in a direct injection fashion.
An injection-locked divider based on a ring oscillator is an inductorless circuit. It occupies a small area and features a wide locking range, in excess of several octaves [80]. As a consequence, no tuning or calibration is needed. Nevertheless, the free running oscillation frequency of the ring oscillator must be in the neighborhood of the divider output frequency. To guarantee the oscillation up to the maximum frequency (i.e. 16GHz), the differential delay cell must be carefully designed. A very simple cell is shown in Fig. 41(a). It uses only 4 MOSFETs (except the injection network) and occupies a small area. Its small dimension, with small output capacitances, results in a low power consumption and a very large locking range. However, the output frequency of a ring oscillator made of a cascade of 4 of these cells may be very low. In addition, when loaded with an output buffer, the frequency further decreases. This problem may be attenuated by using the cell of Fig. 41(b), which is the same implemented in the DQG of SKuRAD1. An increase of the output frequency is obtained by an increase of $W_{M_N^*}$ and $W_{M_P^*}$. This results in a larger cell dimension with associated larger power consumption and lower


OUT$_I$
OUT$_Q$
Programmable multi-loop
INJ
0°
180°
270°
90°
Phase Distribution
multi-loop OFF

(a)

(b)

(c)

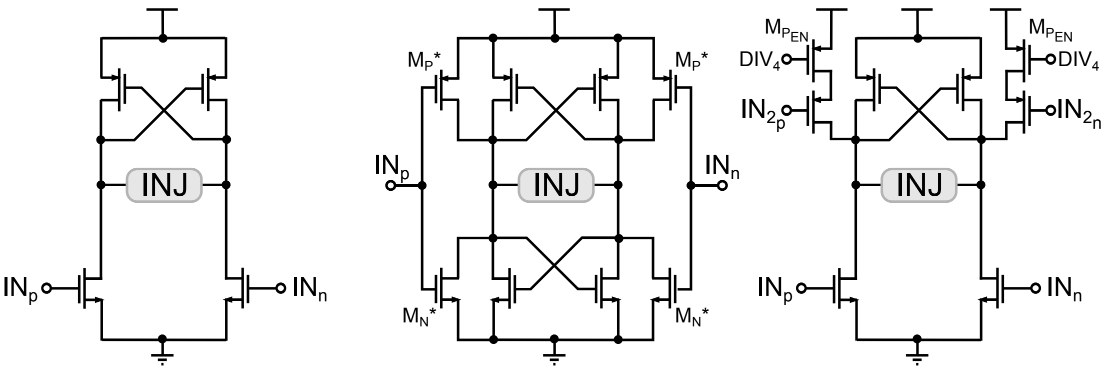
Figure 40: Schematic of the divider core in the three modes of operation: divide-by-1 (a), divide-by-2 (a) and divide-by-4 (a).

locking range with respect to the previous cell. Anyway, a cascade of 4 of these cells results in a frequency well below the target of 16GHz. Forcing a 4-stage CMOS differential ring oscillator to operate at frequencies in excess to 16GHz is, in fact, difficult even in scaled technologies. As a consequence, a multi-loop topology is employed to additionally increase the oscillation frequency of the ring [56]. Fig. 41(c) shows the schematic of the proposed delay cell. It is substantially a combination of (a) and (b). Hence, it features a large tuning range with a lower power consumption with respect to (b). Most importantly, it allows the multi-loop operation through the secondary inputs $\mathrm{IN}_{2_{p,n}}$. In the divide-by-4 operation mode, however, a lower output frequency is needed. In this case, MOSFETs $M_{P_{EN}}$ can be turned off in order to disable the multi-loop feature.

A phase distribution network is used to route the quadrature phases to the injection circuitry, and thus select the desired division ratio. It is implemented by means of multiplexers based on tri-state gates, as shown in Fig. 42. The multiplexers select which of the four possible phases is routed to each injection device, depending on the desired frequency division ratio. Since each injection transistor is fed at most by three different phases (see Fig. 40), the fourth tri-state gate of the multiplexer is a dummy element to balance the capacitive load seen by the RB, while minimizing the fan out of the multiplexers. Each of the four phases is routed to at most seven different injection devices, as shown in Fig. 40. Each signal is AC-coupled to seven different multiplexers by reusing the same biasing network, as illustrated in Fig. 43. This arrangement balances the loading on the RB for the various signals of the phase sequence. In Fig. 43, the schematic of the basic tri-state gate of the multiplexer is also shown.

The RBs, the same as in SKuRAD1, are injection-locked 2-stage differential ring oscillators, as shown in Fig. 39. The principle of operation is similar to the divider core. However, the lack of reconfigurability leads to an even wider locking range. Hence, the same design can be operated both as a buffer at the input of the divider and at its output without the need of any tuning. The RBs show a locking range in excess to 3 octaves.

Quadrature signals are generated by the RBs out of the differential PLL signals. Since a multi-phase injection results in a wider locking range [17], two loaded inverters facilitate the injection locking of the first RB (Fig. 39). It is worth to notice that the quadrature accuracy here is not ultimately important since, along the chain, each injection-locked stage contributes to progressively improve the quadrature accuracy [44]. Thus, even an initial error of some tens of degrees allows to obtain the desired quadrature error of $\leqslant 1.5°$.



(a) (b) (c)

Figure 41: Schematic of various type of delay cells that can be used in a ring oscillator. Simple and without frequency tuning (a), cell used in SKuRAD1 that allows the frequency tuning (b) and the proposed SKuRAD2 cell that allows the multi-loop feature (c).

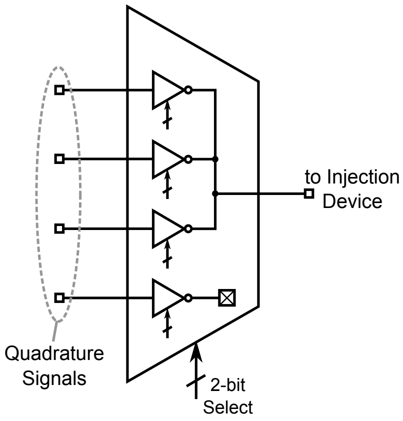


Figure 42: Schematic of the multiplexer used in the phase distribution network.

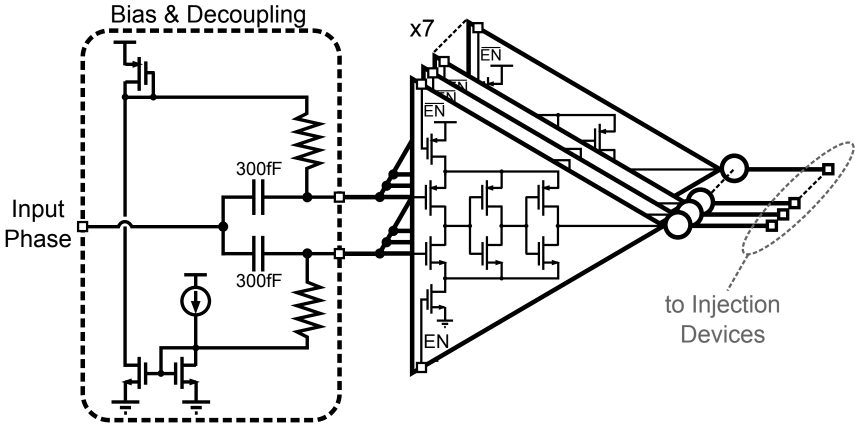


Figure 43: Sketch of the phase distribution network.

3.3.2.1 *Layout Strategies for High Quadrature Accuracy*

To guarantee such a high quadrature accuracy, some efforts have to be spend on the layout of the frequency divider. In fact, the layout of this block took a long time, comparable with the time required for the design.

The first obvious rule that has to be observed is that the layout must be symmetrical. Apart from this, however, other strategies have been put in place. All paths have been made balanced with respect to the capacitive parasitics. Every employed capacitor (for the AC-coupling for example) has been screened with grounded lines to reduce the cross-coupling between paths carrying signals with different phases and to balance the parasitic capacitances.

To guarantee some spacing between AC-coupling capacitors and to ensure symmetric interconnections between IDQG and phase distribution network, the layout of the programmable frequency divider must be stretched, as visible from the concept-layout of Fig. 44. As a result, large parasitic capacitances are associated with the long interconnections between the 4 cells of the multi-loop ring oscillator. To reduce the undesired cross-coupling between paths carrying different phases, every long interconnections has been similarly screened with grounded lines (Fig. 44). This increases the parasitic capacitance to ground, but strongly reduces the Miller effect. As a consequence, each output node of the IDQG results loaded with a smaller parasitic capacitance. This also helps the operation in the higher octave.

Finally, every circuit cell (e.g. the delay cell in the divider and RB) has been also screened, such that every corresponding MOS device in different cell instances is loaded with similar parasitic capacitances.

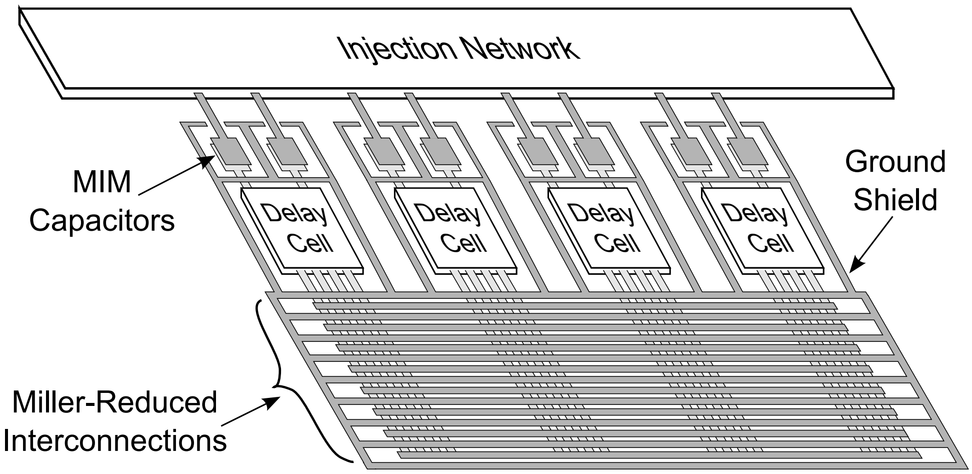


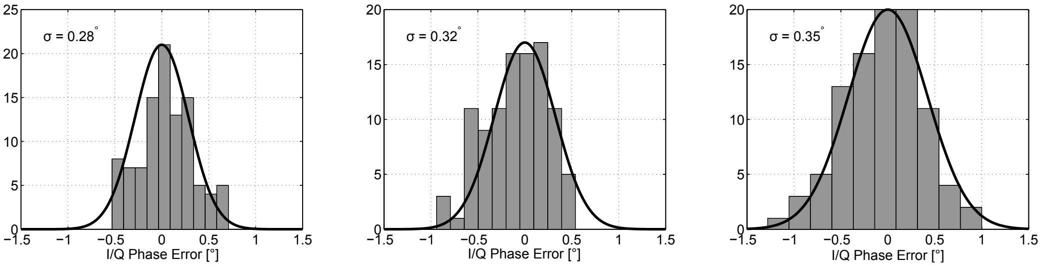
Figure 44: Concept-layout of the IDQG showing the strategies adopted to reduce and balance the total parasitic capacitances.

3.3.2.2 *Quadrature Accuracy and IDQG Performance*

To assess the robustness of the proposed LO generation, a set of 100 Monte Carlo simulations have been done over the extracted layout with respect to process variations and mismatch.

Fig. 45 shows the histograms of the quadrature error in the three different division modes for an input frequency of 16GHz. As shown, the standard deviation is always smaller than 0.35°. The same simulation, made over the entire frequency range, is shown in Fig. 46. Here, the standard deviation of the quadrature error Δ_ψ is shown to be smaller than 0.5° in the total band of $2-16$GHz.

The simulated 0-peak amplitude of the fundamental harmonic of the mixer input signals is shown in Fig. 47(a). As visible, the signal amplitude is constant over the entire bandwidth and is always larger than $V_{DD} = 1.2V$. This follows from the fact that the IDQG outputs rail-to-rail square waves. To conclude this section, Fig. 47(b) shows the standard deviation of the amplitude mismatch between any of the quadrature phase signals. In the three modes of operation it is always smaller than 6mV.



(a) (b) (c)

Figure 45: Histograms showing the simulated (100 Monte Carlo iterations) quadrature error in the three modes of operation: divide-by-1(a),divide-by-2(b) and divide-by-4(c).

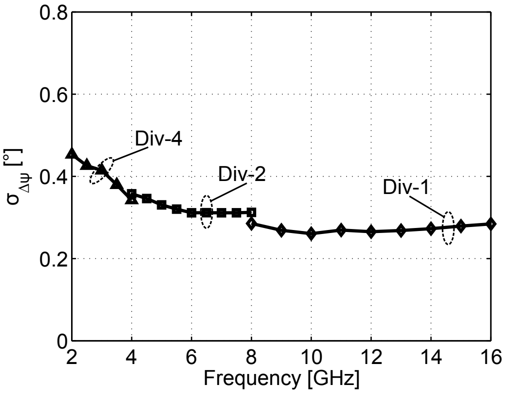


Figure 46: Simulated (100 Monte Carlo iterations) standard deviation of the quadrature error Δ_ψ.

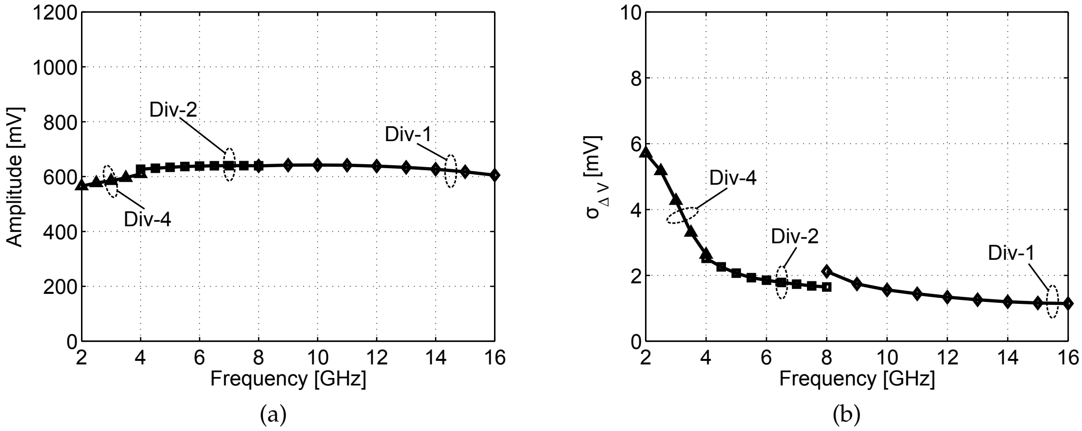


Figure 47: Simulated $0-peak$ voltage at the mixer inputs (a) and its standard deviation $\sigma_{\Delta V}$ (b).

3.3.3 *Harmonic Rejection TX Buffer*

One of the biggest impairment that may affect a multi-octave transceiver is the presence of the transmitted signal harmonics. These harmonics might fall within the bandwidth of the receiver and corrupt the desired signal. This effect is heavily accentuated in the proposed application, where a very high dynamic range is required to resolve the weak tumor backscatter. In the selected direct conversion architecture, the differential quadrature downconverter inherently suppress even harmonics, but is sensitive to odd ones. to a first-order approximation, a harmonic rejection of 100dB is needed at the TX side to achieve the desired 100dB dynamic range. However, the third harmonic of the transmitted signal is in band ($2-16$GHz) only for output frequencies smaller than 5.3GHz. A lower frequency corresponds to a lower attenuation of the antenna-tumor-antenna path (cf. Fig. 12), hence a smaller demanded dynamic range. As an example, at 5.3GHz the required dynamic range is lower than 50dB. Additionally, considering the fact that the third harmonic of a square wave has an amplitude of 10dB less with respect to the fundamental (both transmitted signal and LO signal are square waves), a harmonic rejection of at least 40dBc results adequate.

The output buffer has the task of delivering -14 dBm to the 50Ω antenna load, while isolating the LO port of the receiver downconverter from the output port of the trans-

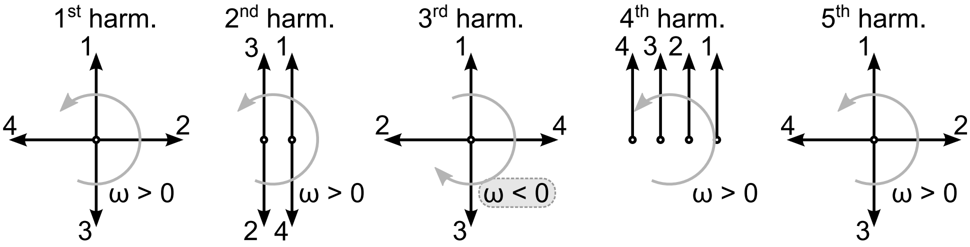


Figure 48: Phasor sequences of the harmonics of quadrature signals.

mitter. Moreover, it must filter out the harmonics of the transmitted signal, with special emphasis to the odd ones, that must be suppressed in excess of 40dBc in a wideband fashion. Achieving such a goal is not trivial at all. Using low-pass or band-pass filtering would require a high-order structure to get a steep roll-off and a high out-of band attenuation. Moreover, such a topology should be made programmable and able to automatically track the position of the harmonics in the frequency spectrum to attenuate them while leaving the desired signal pass through. A tunable notch filter, as the one in [84], could be an alternative solution. However, it would occupy a large silicon area due to the need of reactive components. Moreover, it would be extremely difficult to make it tunable over a multi-octave frequency range, not to mention that a single notch would only solve the issue with one specific harmonic tone. In addition, this solution suffers the overhead due to the need of automatic tuning and calibration.

The proposed harmonic rejection solution is simple, robust, wideband, and inductor-less, thus compact. It is based on asymmetric poly-phase filters (PPFs). It leverages the quadrature signal sequence available at the output of the programmable frequency divider as follows. It is well known [10, 27] that PPFs are capable of discriminating between positive and negative frequency components, as they operate on sets of quadrature signals, that can be interpreted as complex signals. A quadrature sequence of phasors is called a forward sequence if each phasor leads the following one in the sequence, and a reverse sequence in case each phasor lags the next one in the sequence [10, 27]. Since the forward and reverse sequences are one the complex conjugate of the other, they can be interpreted as a set of positive frequency phasors and a set of negative frequency phasors, respectively. If the quadrature signals do not have sinusoidal waveforms, and yet they are evenly spaced in time, the fundamental tones make a forward quadrature sequence. Their harmonics, however, do not, in general. As shown in Fig. 48, the second harmonics make a differential sequence, the fourth harmonics make a common-mode sequence, and only the fifth harmonics make another forward quadrature sequence. More importantly, the third harmonics make a reverse quadrature sequence, that is if the fundamental is at the positive frequency $+\omega$, the third harmonic is at a negative frequency: -3ω. A PPF can thus be used to let the fundamental through while notching out the third harmonic.

The schematic of the harmonic rejection buffer is shown in Fig. 49. A three-stage PPF is designed to achieve broadband operation across PVT variations. The frequencies of the transmission zeros of the three RC sections are staggered as discussed in [10]. An attenuation in excess of 40dBc of the third harmonic is consistently achieved in the $6-16$GHz range, as shown in Fig. 50(a). A matrix of switches is embedded between the second and third stage of the PPF. This arrangement results in a double feature. On the one hand, the switches can be used to turn the transmitter off and perform loop-back calibration of

DC offsets, local oscillator feedthrough, and transmitter-receiver leakage, as described in [9]. On the other hand, it allows to reverse the signal phase sequence just before the last filter section. As a consequence of this sequence reversal, the higher frequency transmission zero is moved from the negative frequency axis to the positive frequency one, as shown in Fig. 50(b). This configuration enables the PPF to simultaneously attenuate the third and the fifth harmonics when the fifth harmonic is in-band. The capacitance is designed to be the same ($C = 150\text{fF}$) in the three sections of the PPF. However, it is slightly decreased in the third section to take into account the parasitic capacitances of the switches (see Fig. 49). To make the operation of the switches maximally effective, 1pF coupling capacitors and 10kΩ resistors are used to set the DC bias voltage at the source/drain of the switch transistors to ground.

The PPF is driven by a regenerative buffer, similar to the one described in Sec. 3.3.2,that ensures isolation between the downconverter LO port and the transmitter output port. Since the required output power is not very high, the pass-band losses provided by the three-section wideband PPF can be tolerated. Finally, by connecting together the output terminals associated to quadrature signals, signal currents are summed (see Fig. 49): the fundamental tone is reinforced by 3dB, while the second harmonic is suppressed.

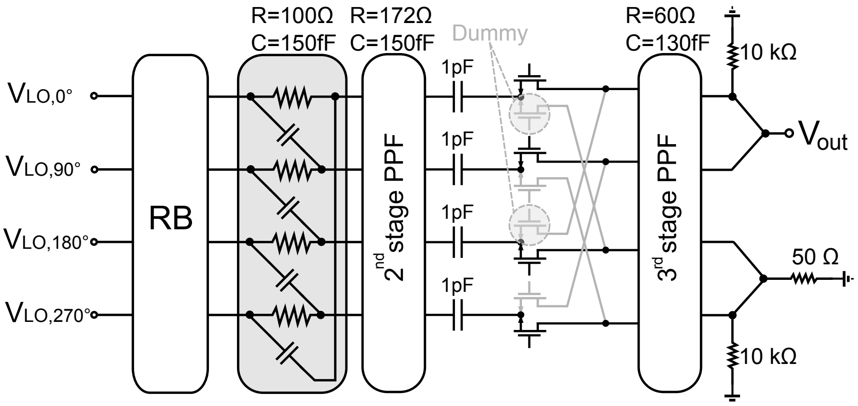
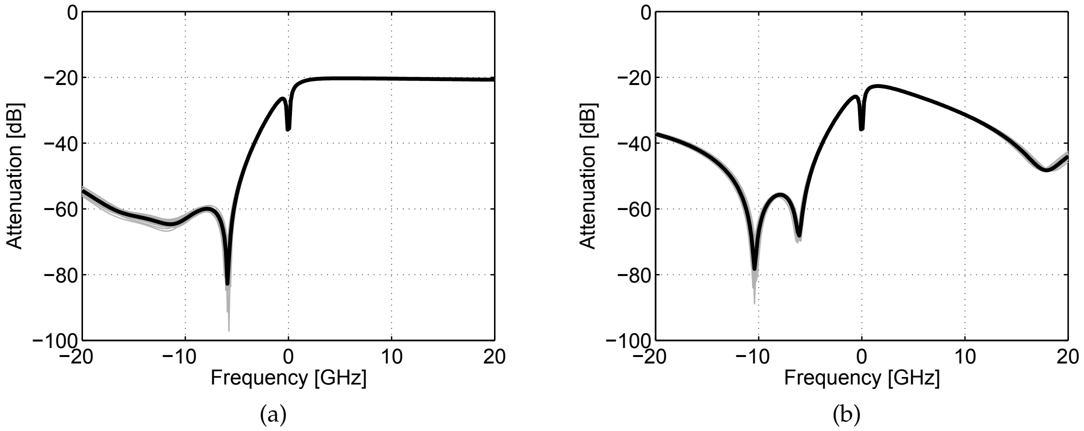


Figure 49: Schematic of the proposed harmonic rejection output buffer.



(a) (b)

Figure 50: Simulated (nominal along with 50 Monte Carlo instances) transfer function of the reconfigurable PPF: (a) configuration to suppress 3^{rd} harmonic (b) configuration to suppress both 3^{rd} and 5^{th} harmonics (used when 5^{th} harmonic is in-band).

4

MEASUREMENT SETUP

SKuRAD1 and SKuRAD2 are realized in a $65nm$ CMOS technology. They implement a receiver and a complete transceiver for a Stepped Frequency Continuous Wave Radar, respectively. As a consequence of the system complexity, some control signals need to change during one measurement (for example when the divider has to change the division modulo or when the PLL changes frequency). For this purpose, a shift register of more than 100 bits is implemented in each IC. This allows us to simply set the configuration bits, bias currents and DC voltages of each block. The register programming, the data acquisition and the imaging generation is made possible thanks to a dedicated full-custom measurement setup.

This chapter is organized as follows. Section 4.1 describes the PCB used to program the shift register, measure the TIAs output and transfer the measurement data to a personal computer. Section 4.2 describes the 2-axis mobile frame used during the imaging experiments to move the target and obtain an ISAR configuration. Finally, Section 4.3 describes the dedicated management software and the communication protocol for the PC-µC data exchange.

The author implemented the entire measurement setup, including the design and implementation of any circuit and PCB, as well as any mechanical and firmware/software realization (both for microcontroller and for PC).

4.1 FULL CUSTOM CHIP PROGRAMMING AND ACQUISITION SYSTEM

The complexity of the complete system led to the realization of a full-custom board to simplify the measurements. The proposed board has been extensively used both for the electrical characterization and the imaging experiments. It makes it possible to program the ICs, measure the baseband signal, and move the target through a GUI running on a laptop.

The main feature of the PCB is a commercial 2-channels 31-bit $\Delta\Sigma$ ADC from Texas Instruments (ADS1282). It features a chopped input PGA and a total SNR of $130dB$. Due to the high dynamic range of this component, the layout of the PCB is critical. To cope with the co-presence of both the microcontroller and the high accuracy ADC, the analog and digital grounds have been carefully separated. Moreover, no switching traces (with the exception of the ADC clock and SPI) have been placed near the converter. Even the μC firmware has been optimized, since no data communication is allowed during an ADC conversion. The measured ADC SNR of 130dB demonstrates the effectiveness of the board layout.

Another feature of the board, which is visible in Fig. 51, is the presence of an ATMEGA32 microcontroller used to program the shift register, drive the stepping motors and communicate with the PC through an RS232 interface. An input/output level translator and an programming input connector completes the board.

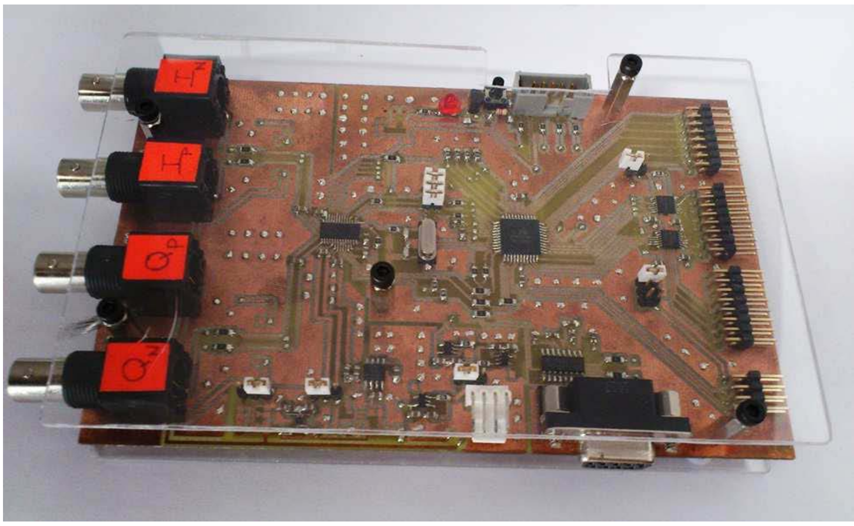


Figure 51: Proposed full custom board containing a μC, an ADC and a serial interface.

4.2 2-AXIS MOBILE FRAME FOR ISAR CONFIGURATION

A synthetic aperture radar (SAR) generates a high resolution image of the illuminated scene by performing a set of measurements at different antenna positions. This increments the effective array dimension, thus increasing the system resolution. In the opposite way, an inverse synthetic aperture radar (ISAR) obtains the same results by moving the target instead of the antenna. However, for both configurations, something able to move accurately either the antenna or the target is needed.

This section presents a 2-axis mobile frame used to move the target in the $x-y$ plane. It is completely made of aluminium with the exception of the wood support which reduces the backscatter near the target. Its dimension is approximately 60x45cm with an effective span of approximately 30x20cm. High accuracy and repeatability are needed to obtain a high resolution image. Hence, the wood support is moved by two high-precision stepper motors through screws and nuts. Due to the screw thread of 1mm/revolution, the ideal accuracy of the system is 2.5μm with a half-step motor driving. Hovewer, the medium-quality of the mechanical parts (not dedicated and expensive lead screws/ball screws have been used) is the main factor that limits the overall accuracy. Hence, a total resolution of $100-200$μm is estimated.

The general purpose I/O pins of the ATMEGA32 cannot drive the motors directly. Thus, a motor driver board has been realized using a TB62206. This PCB is capable to drive the motors with 35V and up to 1.5A/phase, more than enough for the intended application. Fig. 53 shows the complete measurement setup including the ADC/µC board, the 2-axis mobile frame and the motors driver board.

4.3 MANAGEMENT SOFTWARE, COMMUNICATION PROTOCOL AND DATA FLOW

The high complexity and reconfigurability of SKuRAD1 and SKuRAD2 requires more than 100 configuration bits. The ADC board presented in Section 4.1 was realized with the intent of simplifying the measurement setup, but, the large number of possible configurations makes it unmanageable if the board is controlled by either a laboratory instrument or a generic software.

To simplify the measurement procedure, a dedicated software has been realized which manages the ADC board and the mobile frame. It is programmed using Visual Basic 6.0 and is fully configurable. Fig. 54 shows the main page of the proposed software. The main features are listed below

- Simple connection with the ADC board through the RS-232 interface
- Fast and simple setting of bias current and voltage of each SKuRAD1/SKuRAD2 block
- ADC control and automatic calibration
- Mobile frame control
- Automatic measurement for the image generation
- VNA control feature, allowing a VNA image generation

To prevent data loss between PC and microcontroller, a simple communication protocol is implemented. Each data exchange must be allowed by the PC and begins with the transmission of a command (CMD) followed by some optional parameters. The µC receives the packet, executes the command and, if required, transmits the result back to the PC. The µC-execution completes with the transmission of the execution-done command (CMD-done). At this point, the PC receives the execution-done command (and some other optional results), executes the requested routine (eg. ADC data visualization, update of the mobile frame coordinates, calculation of the new frequency point, ecc...) and closes the transmission. If no data is received back from the µC within 2/3 seconds from the transmission of CMD, a timeout occurs and the command is transmitted another time. A simple flow-chart of the communication protocol is visible in Fig. 55.

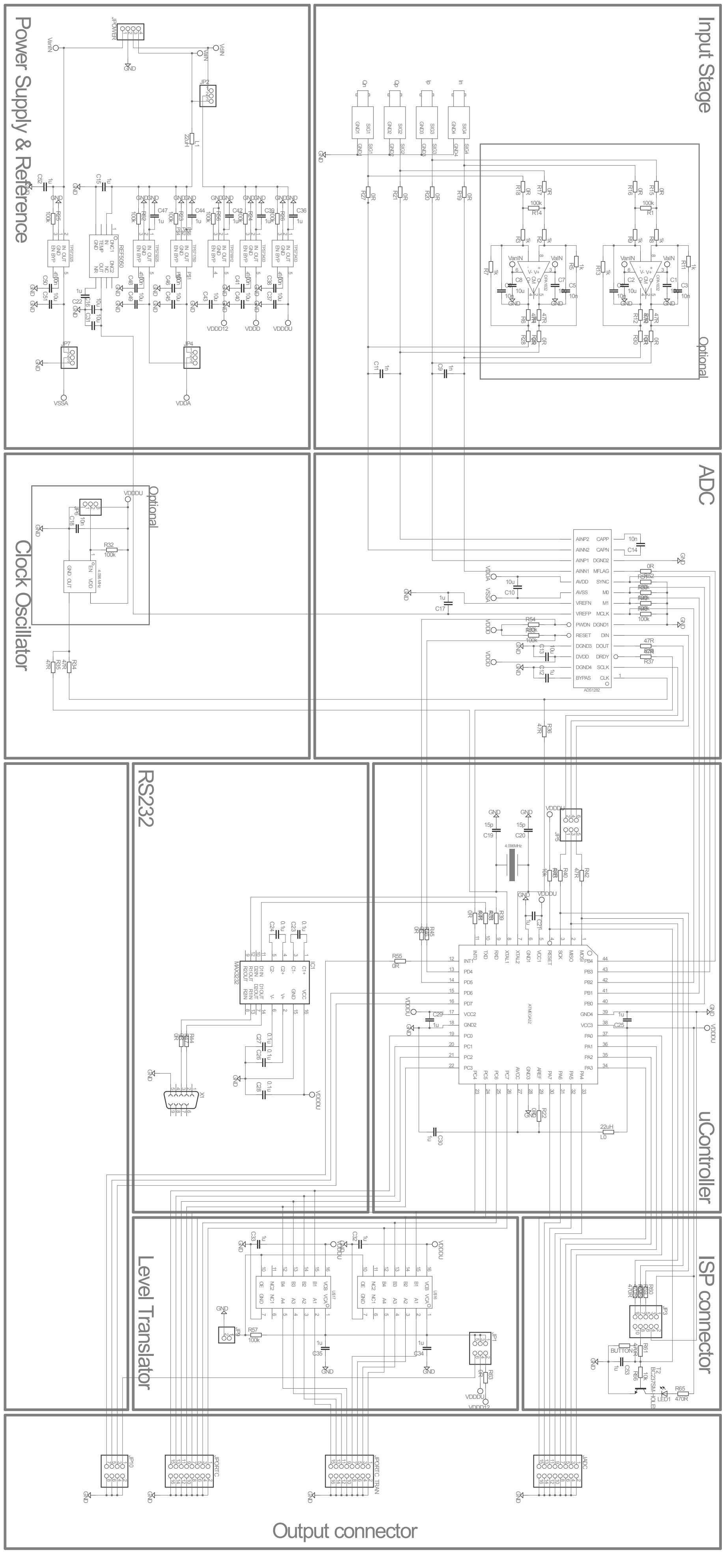

Power Supply & Reference
Input Stage
Optional
ADC
Clock Oscillator
Optional
uController
RS232
Level Translator
ISP connector
Output connector

Figure 52: Schematic of the proposed PCB.

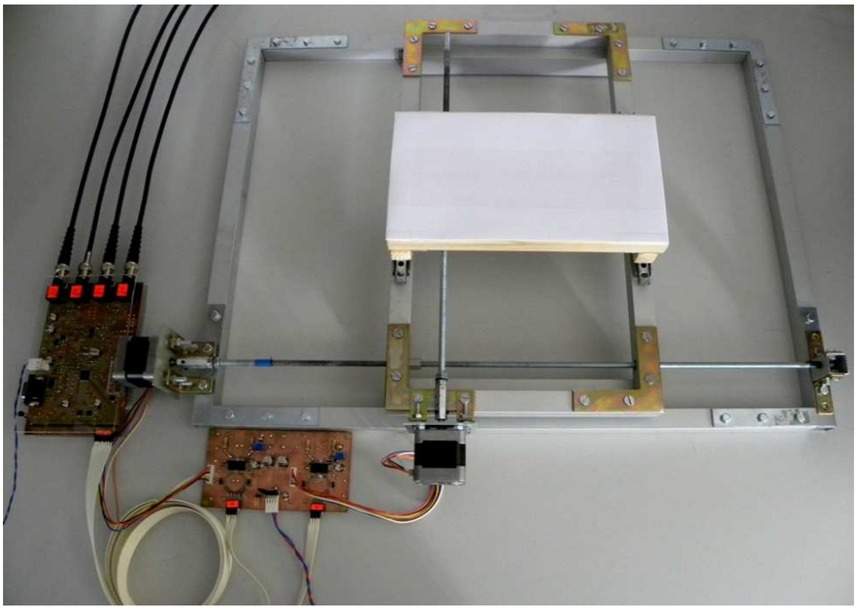
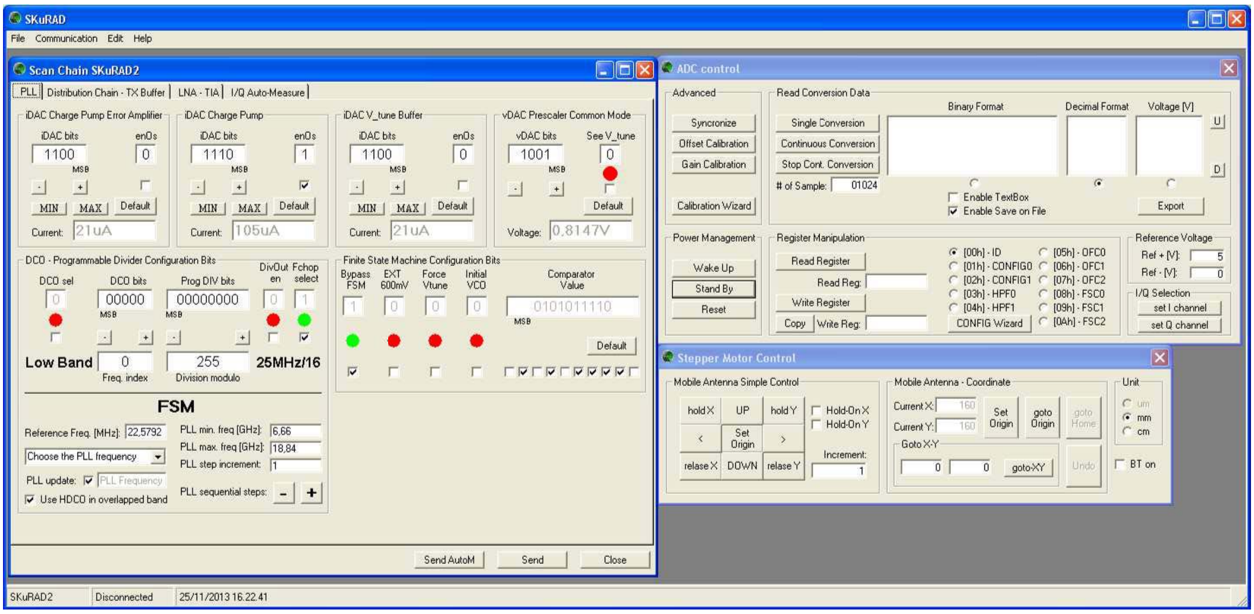


Figure 53: Photograph of the proposed measurement setup.


SKuRAD
File
Communication
Edit
Help
Scan Chain SKuRAD2
PLL
Distribution Chain - TX Buffer
LNA - TIA
I/Q Auto-Measure
MSB
-
+
MIN
MAX
Default
Send AutoM
Send
Close
ADC control
Advanced
Syncronize
Offset Calibration
Gain Calibration
Calibration Wizard
Read Conversion Data
Single Conversion
Continuous Conversion
Stop Cont. Conversion
Binary Format
Decimal Format
Voltage [V]
U
D
Export
Power Management
Wake Up
Stand By
Reset
Register Manipulation
Read Register
Write Register
Copy
CONFIG Wizard
Reference Voltage
I/Q Selection
set I channel
set Q channel
Stepper Motor Control
Mobile Antenna Simple Control
hold X
UP
hold Y
<
Set Origin
>
relase X
DOWN
relase Y
Mobile Antenna - Coordinate
Set Origin
goto Origin
goto Home
Goto X-Y
goto-XY
Undo
Unit

iDAC Charge Pump Error Amplifier: iDAC bits 1100, enOs 0 ☐, Current: 21uA

iDAC Charge Pump: iDAC bits 1110, enOs 1 ☑, Current: 105uA

iDAC V_tune Buffer: iDAC bits 1100, enOs 0 ☐, Current: 21uA

vDAC Prescaler Common Mode: vDAC bits 1001, See V_tune 0 ☐, Voltage: 0,8147V

DCO - Programmable Divider Configuration Bits: DCO sel 0 ☐, DCO bits 00000, Prog DIV bits 00000000, DivOut en 0 ☐, Fchop select 1 ☑

Low Band, Freq. index 0, Division modulo 255, 25MHz/16

Finite State Machine Configuration Bits: Bypass FSM 1 ☑, EXT 600mV 0 ☐, Force Vtune 0 ☐, Initial VCO 0 ☐, Comparator Value 0101011110 ☐ ☑ ☐ ☑ ☐ ☑ ☑ ☑ ☑ ☐

FSM

Reference Freq. [MHz]: 22,5792

Choose the PLL frequency

PLL update: ☑ PLL Frequency

☑ Use HDCO in overlapped band

PLL min. freq [GHz]: 6,66

PLL max. freq [GHz]: 18,84

PLL step increment: 1

PLL sequential steps: – +

SKuRAD2 | Disconnected | 25/11/2013 16.22.41

# of Sample: 01024

○ ● ○

☐ Enable TextBox

☑ Enable Save on File

Read Reg:

Write Reg:

● [00h] - ID ○ [05h] - OFC0

○ [01h] - CONFIG0 ○ [06h] - OFC1

○ [02h] - CONFIG1 ○ [07h] - OFC2

○ [03h] - HPF0 ○ [08h] - FSC0

○ [04h] - HPF1 ○ [09h] - FSC1

○ [0Ah] - FSC2

Ref + [V]: 5

Ref - [V]: 0

☐ Hold-On X

☐ Hold-On Y

Increment: 1

Current X: 160

Current Y: 160

Goto X-Y: 0 0

○ um ● mm ○ cm

☐ BT on

Figure 54: Screenshot of the main page of the measurement software.

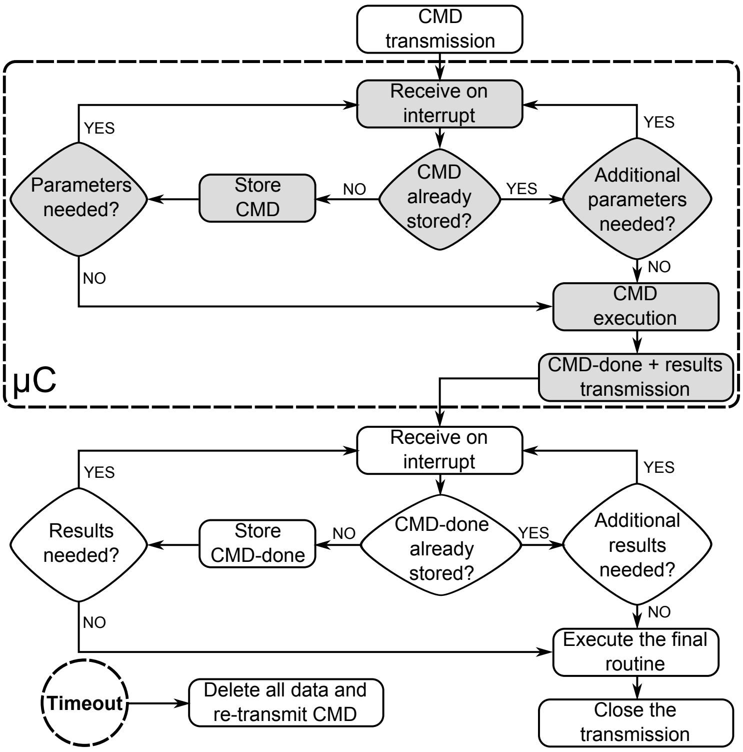

CMD transmission
Receive on interrupt
YES
YES
Parameters needed?
Store CMD
NO
CMD already stored?
YES
Additional parameters needed?
NO
NO
CMD execution
CMD-done + results transmission
μC
Receive on interrupt
YES
YES
Results needed?
Store CMD-done
NO
CMD-done already stored?
YES
Additional results needed?
NO
NO
Execute the final routine
Timeout
Delete all data and re-transmit CMD
Close the transmission

Figure 55: Flow chart of the implemented communication protocol. A gray background refers to μC routines, while a white background refers to PC instructions.

5

MEASUREMENT RESULTS

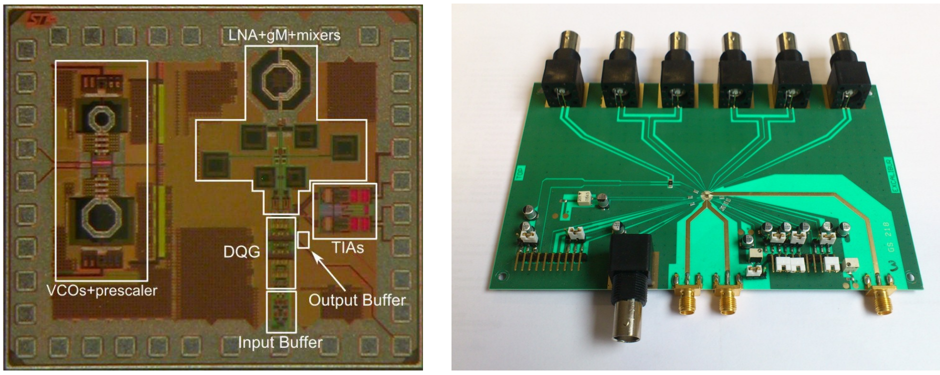
5.1 ELECTRICAL CHARACTERIZATION

5.1.1 *SKuRAD1 Measurements*

This section presents the electrical characterization of the first prototype of the radar tailored for the breast cancer diagnostic imaging, named SKuRAD1. It is implemented in a $65nm$ CMOS technology from ST Microelectronics and occupies an area of $1x1.2mm^2$ including PADs. It is composed by a wideband 3-stage LNA, a quadrature downconverter, 2 chopper Transimpedance Amplifiers (one for each I/Q path) and a programmable frequency divider which generates the quadrature LO signals from 1.75 to $15GHz$. The prototype includes also other blocks, like input and output test buffers and VCOs, that are implemented only for test purposes. The chip microphotograh is shown in Fig. 56(a).
Unless otherwise noted, the main measurement setup is as follows. The chip is mounted with the chip-on-board technology on a Rogers RF PCB. All PADs are bonded, excluding LNA and test buffer inputs. RF measurements have been done with the aid of a RF-probe station capable of measuring up to $18GHz$ (the upper frequency is limited by the cables). GSG probes are manufactured by |Z|PROBE and are characterized up to $40GHz$. TIA's low-frequency outputs have been connected to an external low noise amplifier (LeCroy DA1855A) which performs the differential-to-single ended conversion and is capable of driving the low 50Ω input impedance of the spectrum analyzer.
This section is organized as follows. Sec. 5.1.1.1 presents the biasing condition and the power consumption of each block. Sec. 5.1.1.2 and 5.1.1.3 present the performance of the system in terms of conversion gain and overall noise. Finally, Sec. 5.1.1.4 introduce the linearity measurements followed by Sec. 5.1.1.5 which presents the I/Q imbalance of the receiver.

5.1.1.1 *DC Power Consumption*

SKuRAD1 chip is powered by a 1.2V power supply. Without taking into account the contribution of input and output test buffers, it consumes $124mW$. A detailed breakdown of the power consumption is presented in Tab. 2.



(a) (b)

Figure 56: Microphotograph of SKuRAD1(a) and PCB used to perform the measurements (b).

Table 2: SKuRAD1 DC power consumption

	DC Current [mA]	DC Power [mW]
LNA	34	40.8
G_m	16	19.2
TIAs	2	2.4
DQG	51	61.2
Buffer$_{OUT}$	3.5	4.2
Buffer$_{IN}$	58	69.6

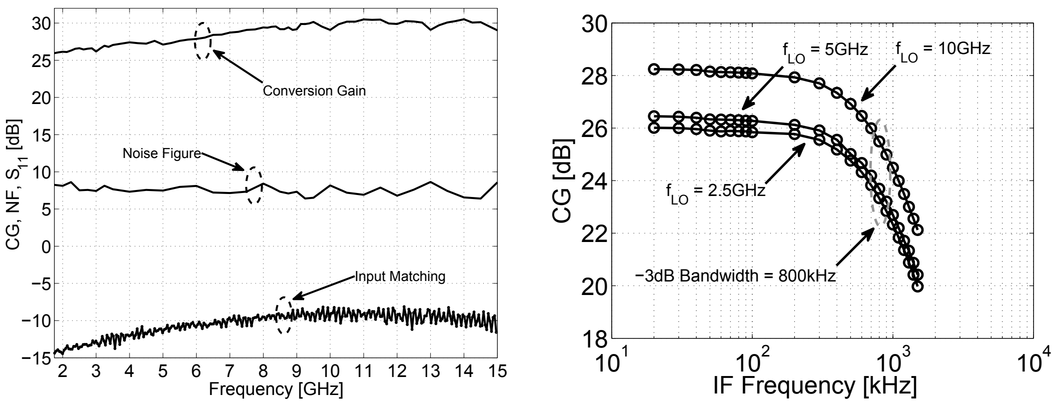
5.1.1.2 *Conversion Gain and Noise Figure*

The conversion gain (CG) and noise figure (NF) have been measured with the aid of Agilent E4407B Spectrum Analyzer and Agilent E8257D/N5183A as RF signal generators. The input matching has been measured with an Agilent E8361A Vector Network Analyzer.

Conversion gain, noise figure and LNA input matching are reported in Fig. 57(a) versus the entire frequency range of interest. The CG is as high as 31dB while the $|S_{11}|$ is always lower than -9dB. The NF spans from 6.4dB to 8.6dB with an average value of 7.6dB. A plot of the conversion gain as a function of the intermediate frequency is reported in Fig. 57(b) for the three different modes of operation of the DQG. In any case, the baseband bandwidth, limited by the TIA, is 800kHz.

5.1.1.3 *Flicker Noise*

The 1/f noise is a potential show-stopper in this system, due to the extremely narrow baseband bandwidth and the direct-conversion architecture. The 1/f noise corner frequency has been measured with the aid of an external ADS1282 ADC. The ADC is an oversampling converter, and it embeds both an anti-alias and a decimation filter. Consequently, it sets the noise bandwidth of the receiver to 1kHz. The chopper frequency has been selected to be 1MHz to avoid any aliasing (the ADC sampling frequency is 4.098MHz), and yet prevent noise folding. A plot of the measured input-referred noise power density is shown in Fig. 58. The flicker noise corner is as low as 40Hz. This un-



(a) (b)

Figure 57: SKuRAD1 measurement results: (a) conversion gain (CG), noise figure (NF) and LNA input matching ($|S_{11}|$); (b) conversion gain vs. intermediate frequency for the three DQG operation modes.

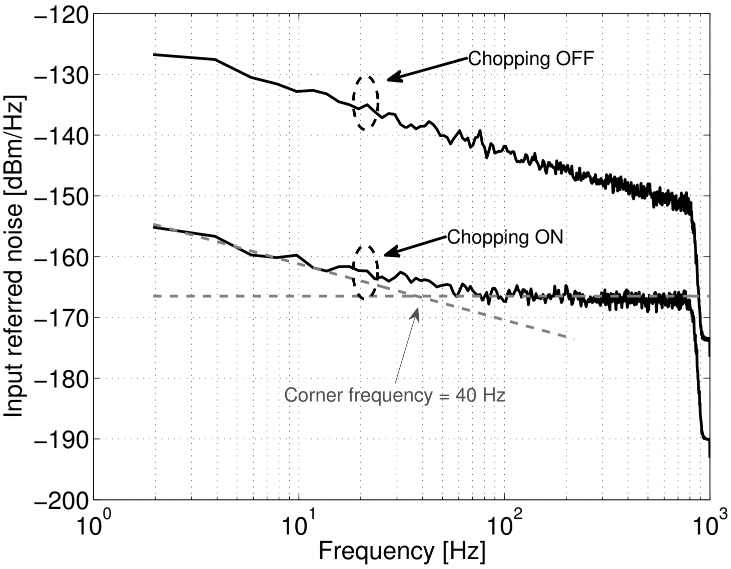


Figure 58: Measured receiver input-referred noise PSD with and without the chopper stabilization of the TIA. The LNA input is closed with a 50Ω load and the DQG is in the divide-by-two operation mode with an input frequency of 10GHz.

precedented result demonstrates the effectiveness of the chopped stabilization technique applied to a wireless direct conversion receiver. The input-referred noise, integrated over the 1kHz ADC band, and combined with the measured P_{1dB}, gives a dynamic range in excess of 106dB, showing that the performance of the proposed receiver is adequate to process simultaneously the strong skin backscatter and the weak echo from the tumor.

5.1.1.4 *Linearity*

Several linearity tests have been carried out. Fig. 59 shows the power of the first harmonic and the third order intermodulation with respect to the input power level. The two input tones have a frequency of (7GHz + 60kHz) and (7GHz + 220kHz) respectively and the third order intermodulation has a frequency of 100kHz.

The measured P_{1dB} as a function of the LO frequency is shown in Fig. 60. From 2 to

15GHz it is greater than −28dBm, well above the −34dBm maximum received signal that we expect from the analysis in Section 2.5.4.

Two-tone measurements are performed to assess the intermodulation performance of the receiver. Since medical imaging is performed in a screened environment, the required third-order intermodulation performance of the receiver is quite relaxed. However, although the desired signal is the only one being received, and although it is a purely sinusoidal tone, still there might be some spurious tones associated with it. Assuming the transmitted signal is generated by an integer-N PLL with a reference frequency of some 10MHz, some reference spurs might be there as undesired interferers. The spurious themselves would be out of the TIA band, and thus be filtered out, but their intermodulation product would corrupt the desired signal. To assess this scenario a two-tone test has been carried out with tones at 25 and 50.05MHz offset from the LO, for various LO frequencies. The IIP3 measured in this condition is reported in Fig. 60: it is greater than −12dBm across the LO frequency range. As a consequence, the maximum relative level of the PLL spurs (S_l) that can be tolerated is

$$S_l \leqslant \frac{3P_{RX} - 2IIP3 - P_d}{3} = -19\text{dBc}. \qquad (24)$$

where $P_{RX} = -34$dBm is the maximum signal we expect to receive, and $P_d = -134$dBm is the maximum distortion we can tolerate to have a 100dB dynamic range. Clearly, the third-order intermodulation distortion performance of the proposed radar receiver results in very loose spurious specifications set on the radar transmitter.

As opposed to third-order intermodulation distortion, second order intermodulation is critical for the proposed direct-conversion receiver, as the skin backscatter acts as a strong in-band interferer. IIP2 has been measured setting the two tones such that both the tone frequencies and the intermodulation products fall within the TIA band. The result is shown in Fig. 60 for seven chip samples: the median value is 30dBm while the worst case is 22dBm.

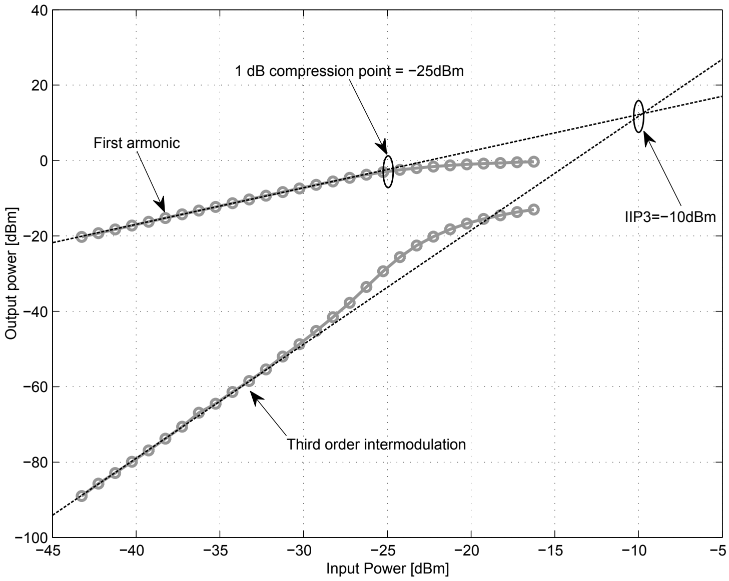


Figure 59: Measured output power of the first harmonic and 3^{rd} order intermodulation versus input power.

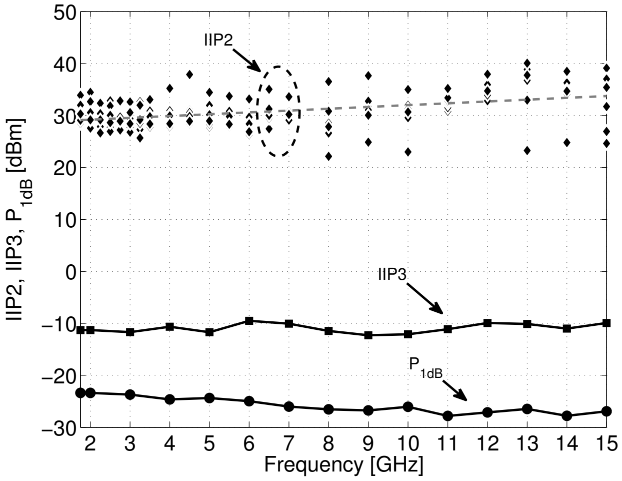


Figure 60: Measured P_{1dB}, IIP3 and IIP2 as a function of the LO frequency.

5.1.1.5 *I/Q Imbalance*

As discussed in Sec. 2.5, in a high-resolution imaging system, the quadrature phase and gain mismatches are very critical impairments. The measured I/Q phase and gain mismatches of seven samples are shown in Fig. 61 and have been measured after the TIAs (hence at IF frequency) with the aid of a high performance oscilloscope. The quadrature error is less than 1.5° across the entire band while the gain imbalance is lower than 0.8dB. In Fig. 61, note that a clear systematic gain mismatch is observed. Such a behaviour was tracked back to a layout error, resulting in a mismatch in the parasitic resistances of the input traces of the TIAs in the in-phase and quadrature paths. Once the systematic gain error is removed from the data in Fig. 61, the residual gain mismatch is limited to few tenths of dB. The good quadrature accuracy achieved over such a wide frequency range confirms that the proposed DQG is capable of excellent performance.

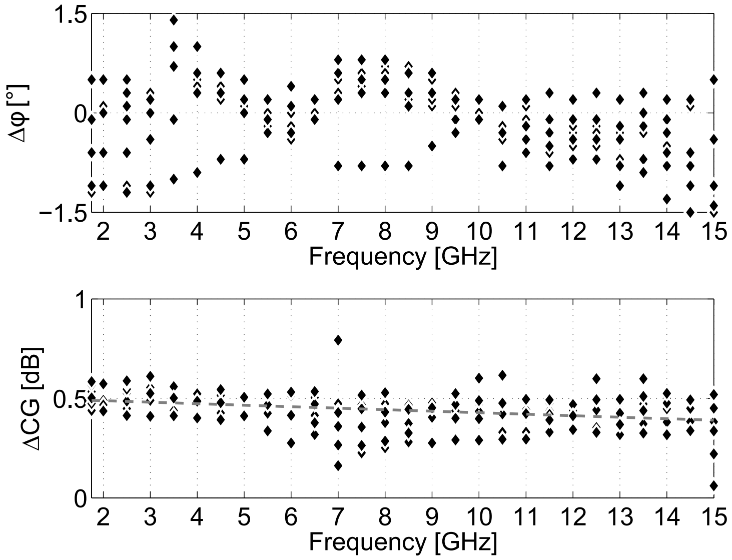


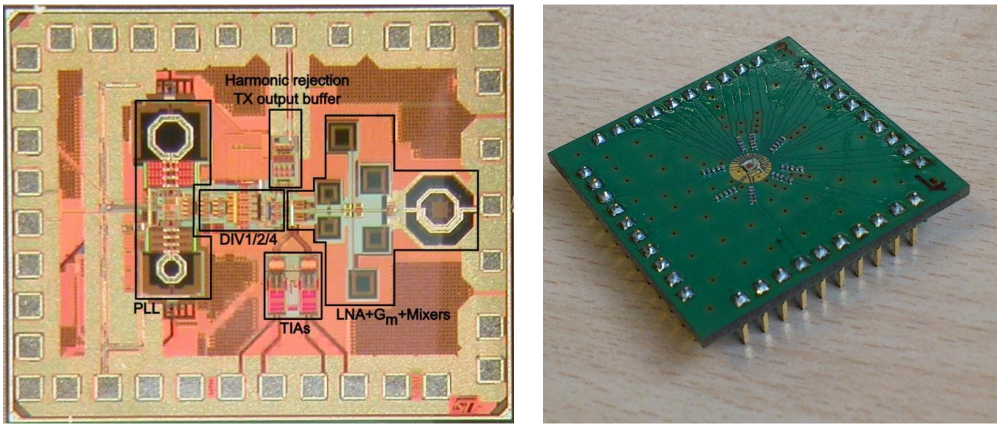
Figure 61: Measured quadrature phase error (Δφ) and conversion gain mismatches (ΔCG) for 7 samples.

5.1.2 *SKuRAD2 Measurements*

This section presents the electrical characterization of the second prototype of the radar tailored for the breast cancer diagnostic imaging, named SKuRAD2. Like SKuRAD1, it is also implemented in a 65nm CMOS technology from ST Microelectronics and occupies an area of 1x1.3mm^2 including PADs. It is the complete ultra-wideband transceiver, thus it is composed by the same receiver as in SKuRAD1 (as already discussed, only small changes have been made in the receiver chain), a new and improved version of the programmable frequency divider, an integer-N PLL which generates signals in the $8-16$GHz range and a harmonic rejection output buffer. The chip microphotograh is shown in Fig. 62(a).

The measurement setup is quite similar to that used for SKuRAD1. This time each chip is mounted with the chip-on-board technology on a small FR4 PCB (Fig. 62(b)) which is then connected to a bigger PCB containing all the components and connectors. This solution allows us to save money since all the expensive components have been bought only once for the bigger board. All PADs are wire-bonded, excluding the LNA input and the TX output. RF measurements have been done with the aid of a RF-probe station capable of measuring up to 18GHz (the upper frequency is limited by the cables). GSG probes are manufactured by PICOPROBE and are characterized up to 40GHz. TIA's low-frequency outputs have been connected to an external low noise amplifier (LeCroy DA1855A) which performs the differential-to-single ended conversion and is capable of driving the low 50Ω input impedance of the spectrum analyzer. Finally, a 22.5792MHz high performance crystal oscillator (CCHD-957) has been used as the PLL reference signal.

The section is organized as follows. Sec. 5.1.2.1 presents the biasing condition and the power consumption of each block. Sec. 5.1.1.2 presents the conversion gain and the noise figure of the modified receiver. Sec. 5.1.2.3 introduces the linearity measurements while Sec. 5.1.2.4 and Sec. 5.1.2.5 show the performance of the PLL in terms of tuning range, phase noise and spur level. Finally, Sec. 5.1.2.6 presents the fundamental and harmonic output power of the harmonic rejection TX buffer while Sec. 3.3.2.2 presents some simulations of the improved frequency divider.



(a) (b)

Figure 62: Microphotograph of SKuRAD2(a) and PCB used to perform the measurements (b).

5.1.2.1 *DC Power Consumption*

SKuRAD2 is powered by a 1.2V power supply. In the worst case condition (i.e. at 16GHz with the frequency divider configured as a divider-by-1) it consumes 204mW. A detailed breakdown of the power consumption is presented in Tab. 3.

Table 3: SKuRAD2 DC power consumption

	DC Current [mA]	DC Power [mW]
LNA	28	33.6
G_m	20	24
TIAs	2	2.4
VCO_L	25	30
VCO_H	33	39.6
Prescaler	2.7	3.24
Div-N+PFD+CP	2.3	2.76
RBs+DIV1/2/4	69	82.8
TX output buffer	13	15.6

5.1.2.2 *Conversion Gain and Noise Figure*

The conversion gain and noise figure have been measured with the aid of Agilent E4407B Spectrum Analyzer and Agilent E8257D as RF signal generator. The input matching has been measured with an Agilent E8361A Vector Signal Analyzer.

Conversion gain, noise figure and LNA input matching are reported in Fig. 63 versus the entire frequency range of interest. The CG is 36dB with a maximum variation of 4.2dB. The −3dB IF bandwidth is 600kHz as depicted in Fig. 64. The variation of the IF bandwidth with respect to SKuRAD1 is related to an increment of the transresistance of the TIAs. The NF spans from 5.5dB to 8.4dB with an average value of 7dB.

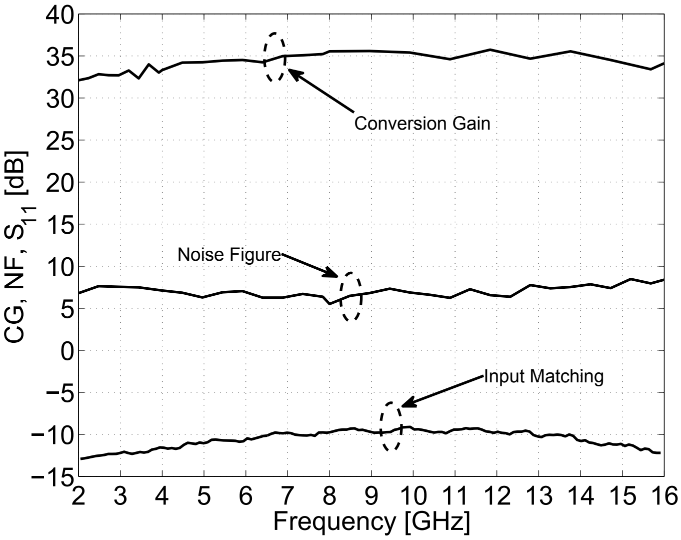


Figure 63: Conversion Gain (CG), Noise Figure (NF) and LNA Input Matching (S_{11}).

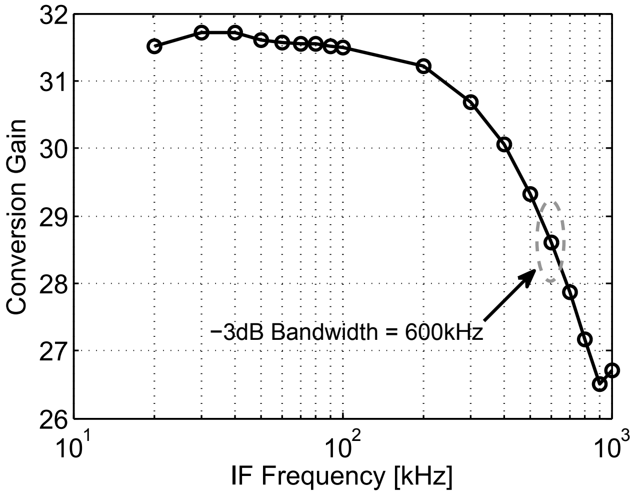


Figure 64: Conversion Gain vs. intermediate frequency @$F_{PLL} = 8GHz$ in the divide-by-4 operation mode.

5.1.2.3 *Linearity*

A two tone test has been carried out to report the linearity performances of the receiver. Fig. 65 shows the P_{1dB} and IIP3. The P_{1dB} is always better than $-28dB$ while the input-referred IP3 is better than $-13dBm$. The two input tones have a frequency of $f_{LO} + 30MHz$ and $f_{LO} + 60.050MHz$, well outside the baseband bandwidth, while their third order intermodulation has a frequency of 50kHz which falls inside the TIAs bandwidth. Additionally, Fig. 66 shows the IM3 as a function of the input power when the two tones are both outside (out-of-band IIP3) or inside (in-band IIP3) the TIAs bandwidth. In the last case, the tone frequencies are $f_{LO} + 60kHz$ and $f_{LO} + 220kHz$ with an intermodulation frequency of 100kHz.

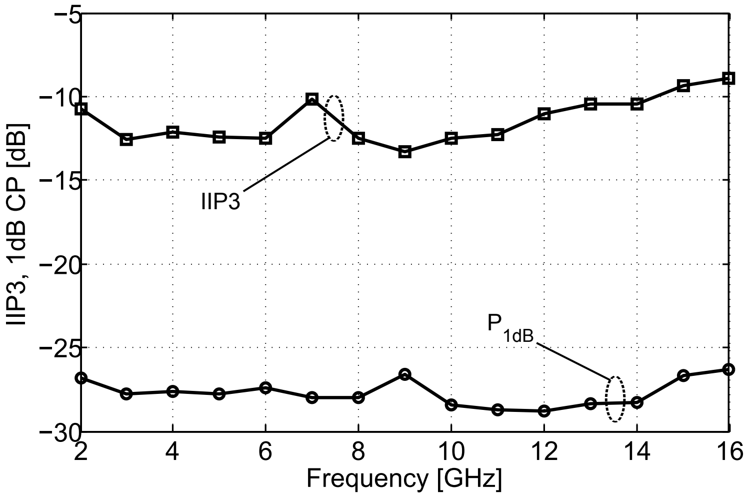


Figure 65: Measured P_{1dB} and out-of-band IIP3 as a function of the LO frequency.

5.1.2.4 *Phase Noise and Tuning Range*

The performance of the PLL have been measured after the programmable divider by 1/2/4 and the harmonic rejection TX buffer with the aid of Agilent E4407B spectrum analyzer. Due to the relatively low output power ($\approx -14dBm$), we used an external

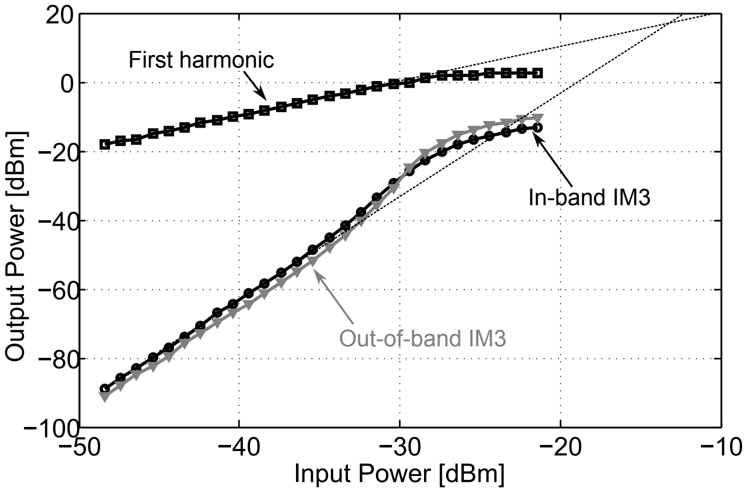
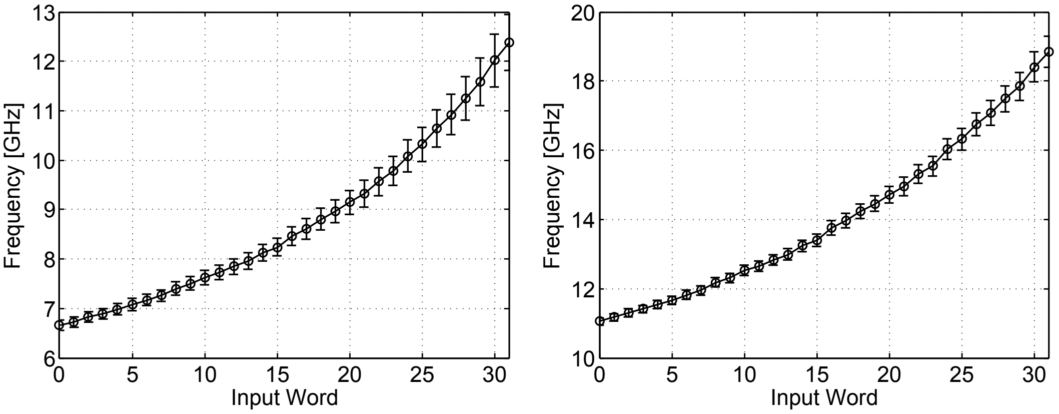


Figure 66: Measured fundamental and third harmonic intermodulation power as a function of the input power.

ZVA-183-S+ wideband amplifier to obtain an accurate measurement. The two VCOs tune from 6.5 to 13GHz and from 11 to 19.3GHz having an overall fractional tuning range of 99%. Fig. 67 shows the measured tuning range of the PLL. It covers with margin the designed bandwidth. Moreover, the 2GHz overlap between the two VCOs makes the design robust against PVT variations.

The VCOs phase noise @10MHz offset is visible in Fig. 68 over the entire frequency range. The offset frequency (10MHz) has been chosen well outside the PLL bandwidth (1MHz) where the VCO is approximately the only contributor to the PLL phase noise. Over the entire frequency range of interests (i.e. 8 − 16GHz), the VCOs PN@10MHz offset is always better than −129dBc/Hz.



(a)

(b)

Figure 67: Measured tuning range of VCO_L(a) and VCO_H(b).

Fig. 69(a) shows the PLL phase noise for two different carrier frequencies. The RMS jitter integrated from 1kHz to 100MHz is 0.68ps(2.2°) and 0.52ps(2.4°) for the 9 and 13GHz carrier respectively. Fig. 69(b) shows the PLL phase noise for different division ratios. Here, the phase noise reduction of 6 and 12dB in the divide-by-2 and divide-by-4 operation mode is visible.

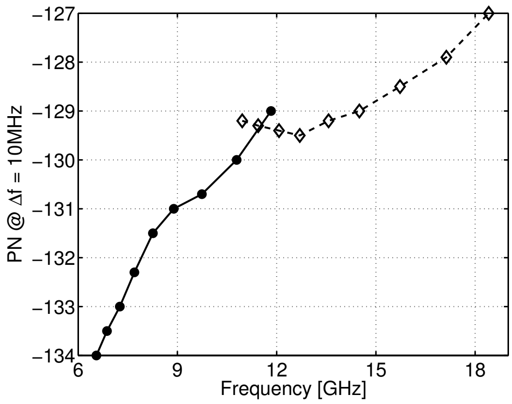
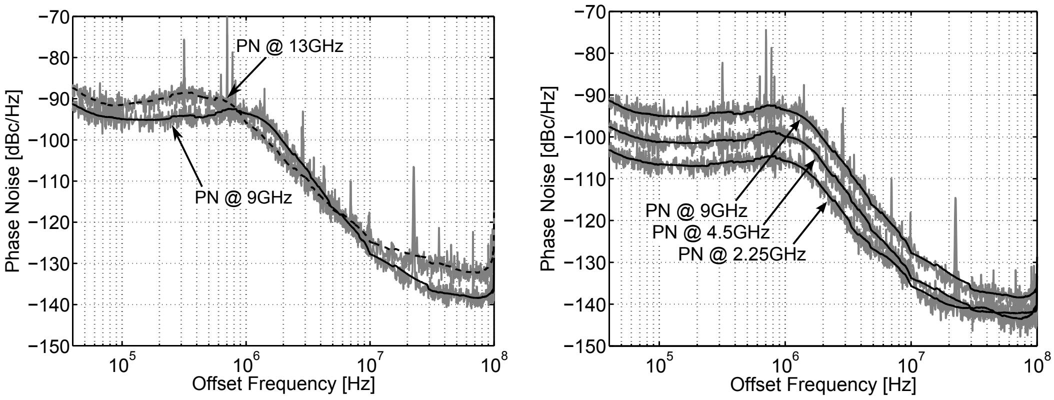


Figure 68: Measured phase noise of VCO_L and VCO_H. at 10MHz offset from the carrier. For this measurement, the chip has been powered with an external battery.



(a) (b)

Figure 69: Measured PLL phase noise for two different carrier frequencies (a) and for three different division ratios (b). For these measurements, the chip has been powered with an external power supply.

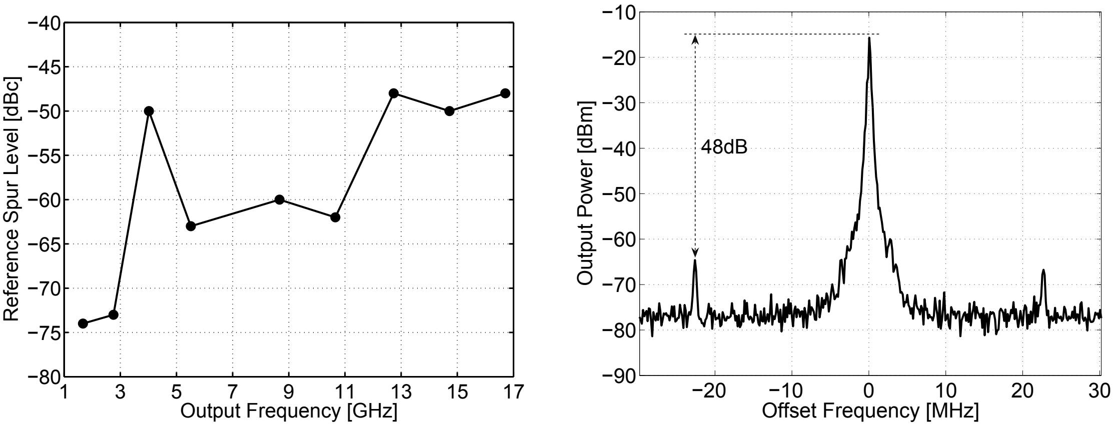
5.1.2.5 *Reference Spur and Settling Time*

The PLL spur level at different carrier frequencies and for different division ratios is visible in Fig. 70(a). The reference spur level is always better than -48dBc. An example of the PLL output spectrum is shown in Fig. 70(b). This has been measured for a carrier frequency of 12.7GHz and shows the worst case spur level.

The transient of the PLL tuning voltage is shown in Fig. 71. The PLL reaches the lock condition in approximately 2μs.

5.1.2.6 *Harmonic Rejection TX*

To verify the effective usefulness of the proposed transceiver in a breast cancer imaging tool, the output characteristics have been measured. The average TX output power is -14dBm (Fig. 72(a)) with a harmonic rejection in excess of 40dBc up to the fifth harmonic. Only the 4th harmonic is less attenuated, but this is not an issue since it is intrinsically rejected by the receiver. As a proof, the measured 4th-harmonic conversion gain is shown in Fig. 72(b). Finally, the switches in the TX buffer allow to suppress the first harmonic by more than 55dB, useful for the calibration process.



(a) (b)

Figure 70: Measured reference spur level as a function of the LO frequency (a) and Measured LO output spectrum at 12.7GHz (b).

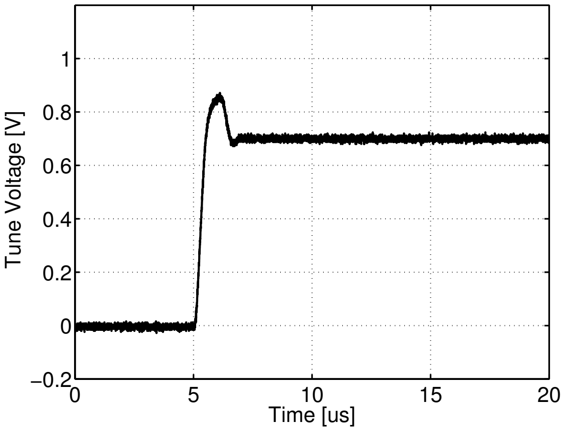
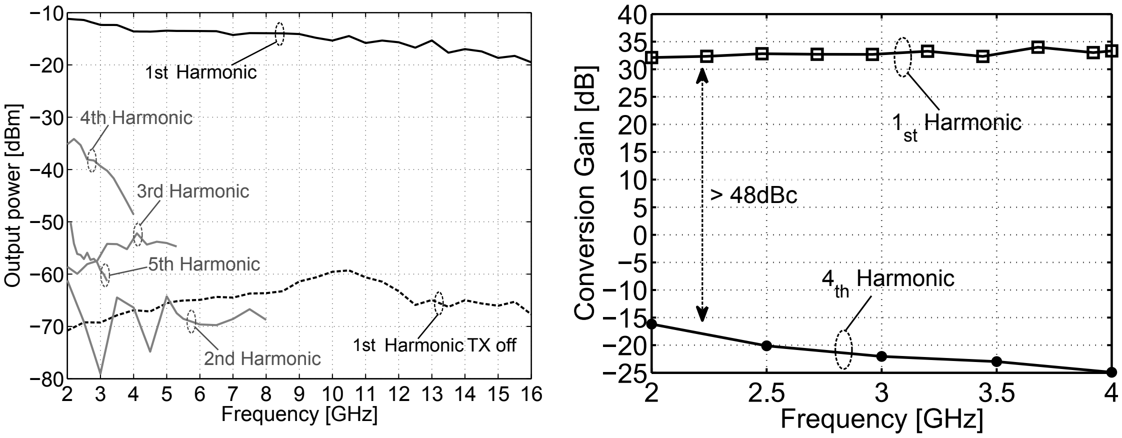


Figure 71: Measured PLL transient tune voltage.



(a) (b)

Figure 72: Measured TX output power and harmonic rejection (a) and measured receiver 4^{th} harmonic conversion gain (b).

5.2 IMAGING EXPERIMENTS

As already described in Chapter 2, the final imaging system consists of an array composed by some elementary modules which can be organized to form different shapes. The single element of the array is made of the realized radar transceiver together with a TX and RX patch antennas. Although measurement results of the electric characterization of SKuRAD2 are in good agreement with the system analysis and constraints for the intended application, nothing has been done (up to now) to verify the effective usefulness of the proposed design in an imaging context.
This chapter proposes some imaging experiments able to proof the operation of the transceiver as an imaging tool. Experiments have been done with SKuRAD2 and a couple of wideband TX/RX patch antennas realized on the same Roger substrate. Due to the fact that RF pads have been probed, it was impossible to realize a real antenna array. As a consequence, we used a full custom 2-axis mobile frame (described in Sec. 4.2) to move the target obtaining an Inverse Synthetic Aperture Radar.
This section is organised as follows. Sec. 5.2.1 reports the design of the proposed wideband path antennas. Sec. 5.2.2 introduces some preliminary imaging experiments while Sec. 5.2.3 shows the imaging results using a realistic breast phantom that mimics the electro-magnetic proprieties of the real breast.

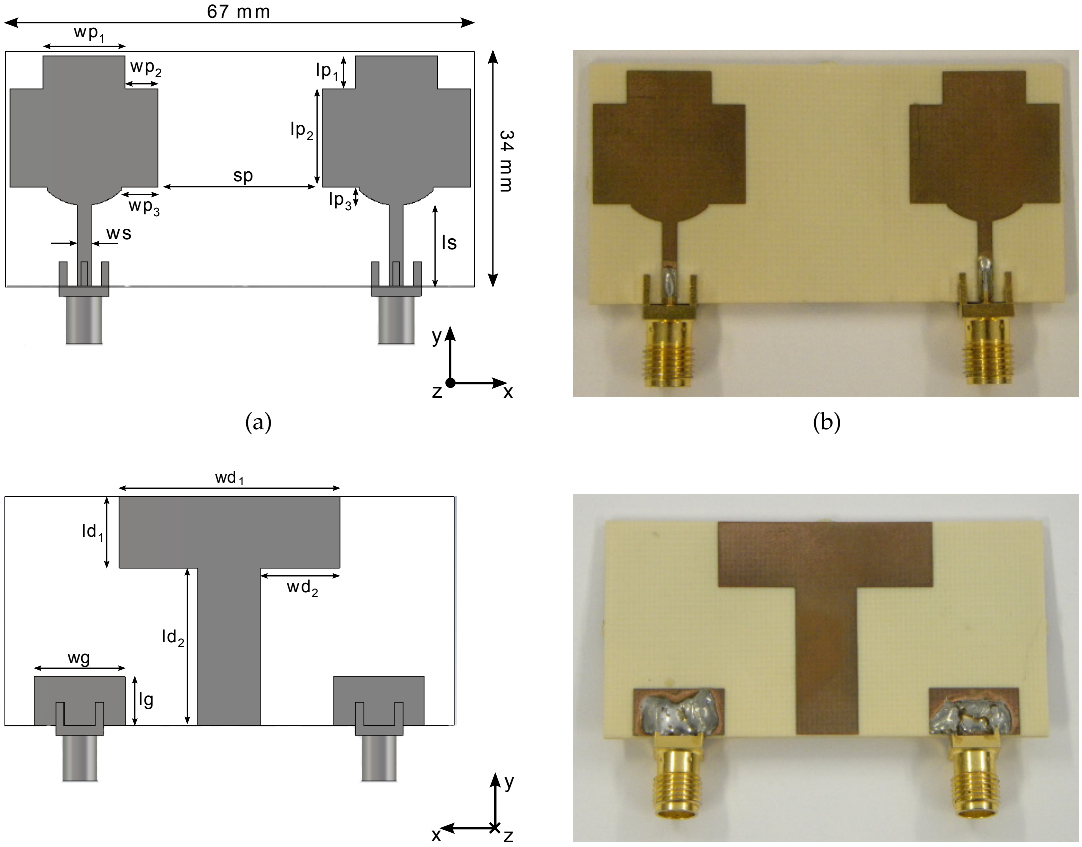
5.2.1 *Patch Antenna*

The design of the antenna structure that complements the integrated radar transceiver is based on two identical printed monopoles for transmission and reception functionality. The requirement for each antenna element of operating on the large wideband from 2 to 16GHz is achieved by means of a combined circular/rectangular shape of the radiating patches, as shown in Fig. 73. In particular, the semicircular part acts as a tapering section for better impedance matching all over the bandwidth to the 50Ω microstrip feeding line. In order to obtain a compact design, the two monopoles are placed very close to each other on the same face of the substrate. To minimize the unavoidable mutual coupling between the antennas, a T-shaped decoupling structure is introduced on the back of the laminate. The geometric parameters wd_1 and ld_1 control the isolation between the two radiating patches in the lower part of the operating band, namely, from 2 to 9GHz, while the geometric parameters wd_2 and ld_2 control the isolation in the upper part of the spectrum, for frequencies higher than 9GHz. Optimization of all the parameters was performed through simulation employing the CST Microwave Studio software.

A prototype of the antenna is shown in Figs. 73(b-d). The prototype was fabricated on a Roger RO4003c laminate, featuring a thickness of 1.524 mm, a dielectric constant of 3.55, and a loss tangent of 0.0027.

The antenna structure was experimentally characterized by using a two-port Agilent N5230A PNA-L network analyzer. The measured reflection and transmission coefficients of the two-element antenna are shown in Fig. 74 and compared to simulation results. The agreement between measurement and simulation is very good for frequencies below 8.5GHz, while at higher frequencies, discrepancies due to soldering and fabrication imperfections are clearly visible. In any case, the measured input matching is lower than -10dB over the entire frequency range of operation with the exception of a small hump at 2.9GHz ($|S_{11}| = -5$dB). Moreover, the antenna-to-antenna isolation is greater than 20 dB for frequencies higher than 3.3GHz, a performance that allows to directly connect the antenna structure to the integrated transceiver.

The simulated antenna radiation pattern on the magnetic plane ($x - z$ plane in Fig. 73, the plane facing the illuminated target) is shown in Fig. 75 for several frequencies. The radiation pattern is fairly omnidirectional, as required by the operation of the antenna within the array.



(a) (b)

(c) (d)

Figure 73: Layout of the antenna structure. Top layer with transmitting and receiving radiating elements (a-b) and Bottom layer with decoupling structure and partial ground plane (c-d). Dimensions are: $wp_1 = 10$ mm, $wp_2 = 4$ mm, $wp_3 = 4$ mm, $lp_1 = 4$ mm, $lp_2 = 12$ mm, $lp_3 = 2.1$ mm, $ws = 1.7$ mm, $ls = 9.9$ mm, $sp = 20$ mm, $wg = 11.5$ mm, $lg = 6.25$ mm, $wd_1 = 28$ mm, $wd_2 = 10$ mm, $ld_1 = 9$ mm, $ld_2 = 20$ mm.

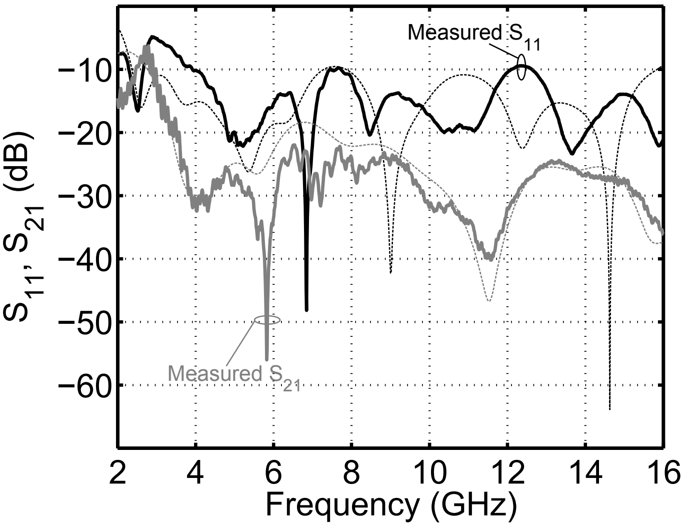


Figure 74: Measured (solid line) and simulated (dashed line) magnitude of reflection (S_{11}) and transmission (S_{21}) coefficients.

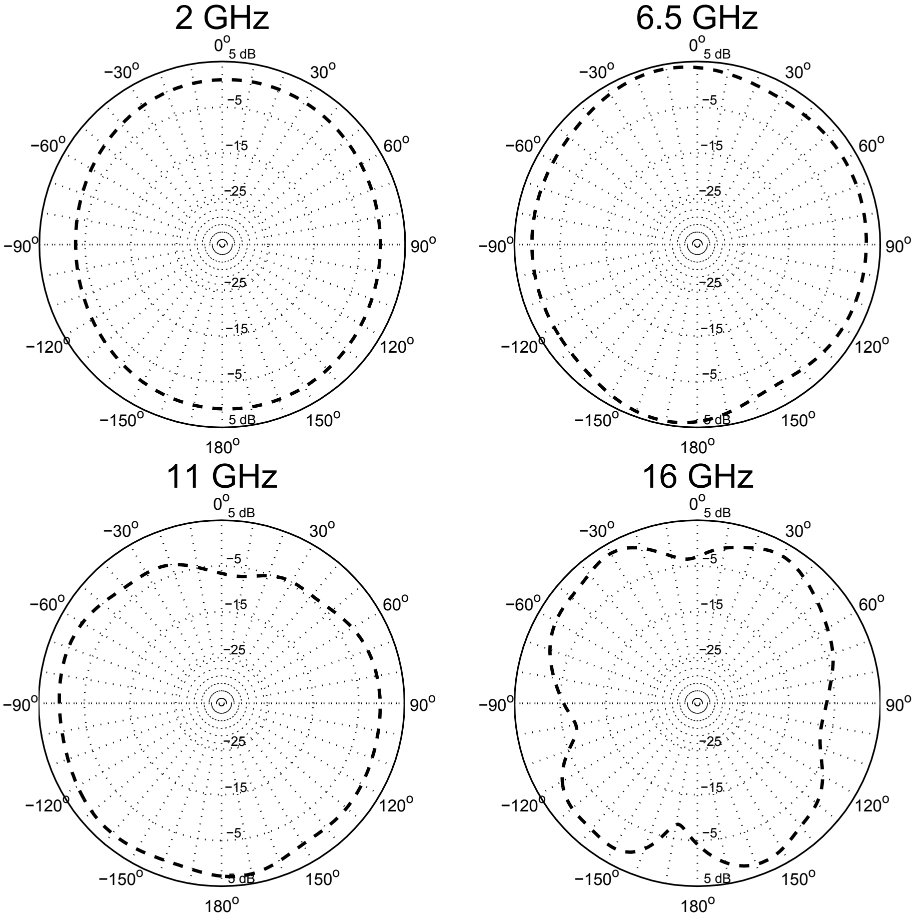


Figure 75: Simulated antenna radiation pattern on the $x-z$ plane (cf. Fig. 73).

5.2.2 *Preliminary Imaging Experiments*

Several tests have been carried out to assess the functionality of the presented integrated radar transceiver together with the planar antenna structure as an effective imaging tool.

As a first test of the correct operation of the system, the backscatter off a metallic plane is measured. The plane is displaced 4.1cm from the antennas and a full-span measurement, consisting of 155 frequency points, is performed. Fig. 76 shows the normalized synthetic time domain pulse obtained after an Inverse Fast Fourier Transform. The pulse duration of 63ps corresponds to a resolution of 9mm in the air and 3mm inside the body due to the reduced phase velocity [52]. Moreover, the peak centered at 275ps indicates the correct distance (two times the distance) between the antennas and the metal plane.
The metallic plane is then placed at different distances from the antennas to characterize the ability of the system to properly detect the distance. The measured displacement from a reference plane placed at 4.6cm away from antennas are shown in Fig. 77(a) and compared to ideal positions. The measurement accuracy is always better than 5mm, as highlighted in Fig. 77(b).
To complete the preliminary tests, a 3.5mm metallic bead has been used as a point scatterer to assess the ability of the radar to detect even small objects. The measurement setup used for this test is the same as in a real imaging context and therefore it will be explained in detail in the next section. The resulting point spread function is shown in Fig. 78. The absence of artifacts makes the transceiver suitable for the detection of small objects.

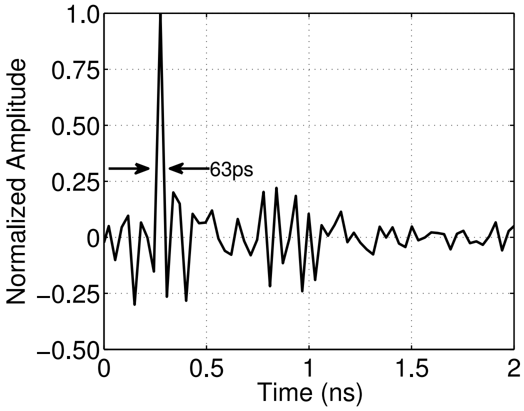
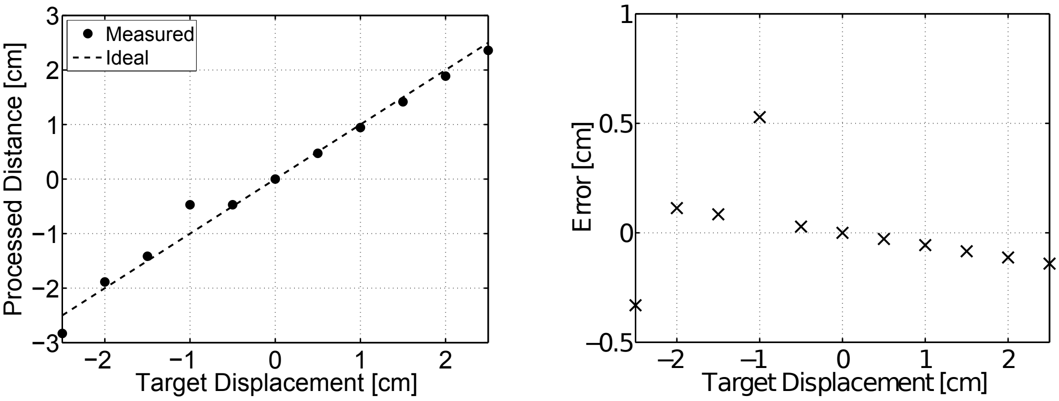


Figure 76: Measured synthetic time-domain pulse scattered off a metallic plane.



(a) (b)

Figure 77: Measured displacement of a metallic plane with respect to the reference plane (a) and measurement accuracy (b).

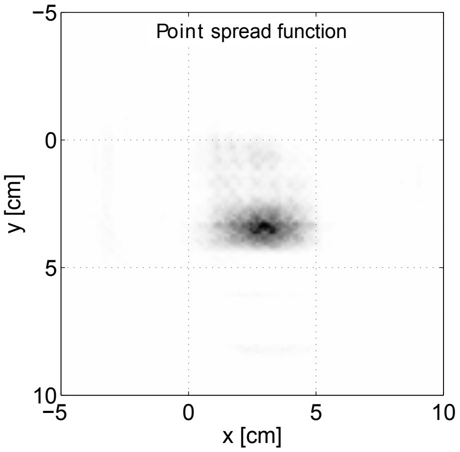


Figure 78: Measured radar image of a 3.5mm metallic bead. The $x-y$ plane is the same plane as the antennas.

5.2.3 *Breast Cancer Imaging Experiments*

This section describes in detail the procedures and results of a realistic breast cancer imaging experiment. For this purpose, a phantom mimicking the actual breast electrical proprieties is realized. It contains two small water-targets which emulate the neoplastic tissue. Results presented in Section 5.2.3.3 assert that the proposed radar transceiver can be effectively used as a breast cancer imaging tool.

5.2.3.1 *Breast Phantom*

Microwave imaging for breast cancer detection seeks to identify the presence and location of relevant tumor targets [25]. Accordingly, a physical breast phantom is realized to conduct experiments on breast cancer detection (Fig. 79). The phantom mimics the electrical properties of the breast tissues and tumors over a wide range of frequencies.
The material modeling the healthy tissue is a mixture of glycerine, double distilled/deionized water, ethylene glycol, polyethylene powder, and agar [7]. The recipe is easy to make, consistent, non-toxic and has been extensively tested over more than two years [7]. The absence of biological materials (pork fat, rabbit muscle, etc.) increments the lifetime of the phantom. Additionally, a bactericide can be used to prevent bacterial contamination.
Two enclosures of different diameters filled with tap water mimicking two tumor targets are buried inside the breast phantom. Tumor target "A" and "B" have a diameter of 6 and 9mm, respectively. With respect to the origin of the measurement setup, which is placed at the center of the phantom in the same $x-y$ plane of the antennas, tumor "A" and "B" are placed at coordinates ($x = -45\text{mm}$; $y = 30\text{mm}$; $z = 70\text{mm}$) and ($x = 15\text{mm}$; $y = 10\text{mm}$; $z = 70\text{mm}$) respectively.
The breast phantom is completely placed into a plastic container and its dimensions are, approximately, 11x11x3cm.

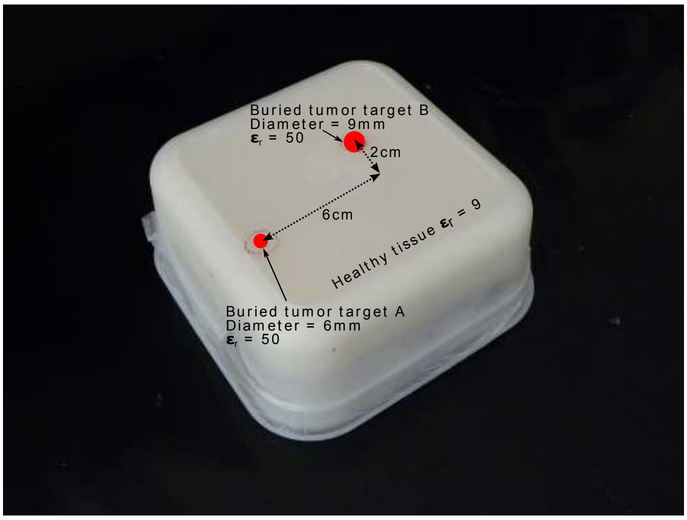


Figure 79: Photograph of the breast phantom placed in a plastic container.

5.2.3.2 *Measurement Setup and Calibration Technique*

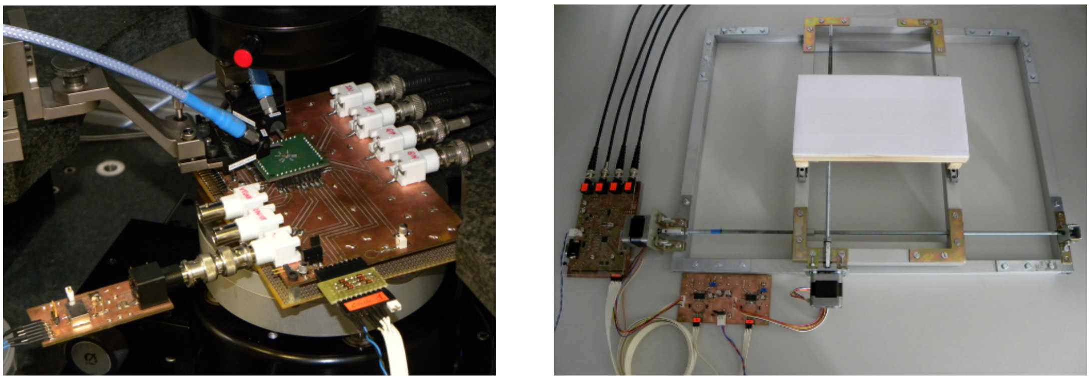
A high resolution radar image is performed by transmitting a wideband pulse and receive the backscatter signal. In a stepped frequency continuous wave approach, however, a very short pulse is obtained by means of an IFFT over a set of narrowband measurements. The measurements accuracy is the key factor in determining the final resolution of the image. In this context, the measurement setup and data handling play a fundamental role.

In the proposed system, the transceiver is assembled in a chip-on-board fashion on a small FR4 PCB connected to a bigger board containing all the needed components and connectors. All pads are bonded, with the exception of RF pads, which are probed (Fig. 80(a)). The transceiver input (LNA) and output (TX buffer) GSG pads are connected through RF cables to the RX/TX antennas placed outside the shielded RF probe station and connected to a solid support. The breast phantom is placed on a wood plane support and moved by high-precision stepped motors over a custom metal frame, allowing an ISAR configuration. The higher the synthetic array dimension and number of measured points, the higher the cross-range resolution and processing gain [8] [37]. As a trade-off between accuracy and measurement time, we choose a synthetic array of 22cm by 15cm at 1cm steps. For each of the $23\text{x}16 = 368$ positions, a set of 155 narrowband measurements, from 2 to 16GHz, are performed. The core of the measurement setup is the full-custom PCB described in Sec. 4.1. It is used to move the phantom in the $x - y$ plane, program the transceiver, measure the differential TIAs outputs and transmit the data to a laptop for the imaging generation. Notice that no data transfer occurs while the ADC is measuring. This avoids possible data corruption caused by the serial interface clock. Fig. 80(b) shows all the components here described while Fig. 81 shows the measurement setup during one imaging experiment.

In order to cope with the receiver and ADC offset, which are critical impairments for a direct conversion architecture, the measurement is made of two parts. First, the switch embedded in the transmitter polyphase filter is turned off. This allows to measure all the offsets due to components mismatch, local oscillator feedthrough, self mixing, and transmitter-to-receiver leakage through the substrate of the integrated circuit, as well as the ADC intrinsic offset. Second, the transmitter output buffer is turned on and the scene is effectively illuminated. The first measurement is then subtracted from the second one to obtain a calibrated response.

A further calibration procedure is required to be able to discriminate the reflections due to the measurement setup and the surrounding environment. The procedure is similar to the "match/short" calibration usually performed on VNAs. A background acquisition (corresponding to the "match" measurement) is first carried out by performing a measurement with no target on the support. This data will be subtracted by the raw data obtained when the target is present. A metallic plane is then placed 4.6cm away from the antenna structure. This corresponds to a "short" measurement, and allows to identify the reference plane of the radar system [3].

Before obtaining a final image, a last calibration step is required. In fact, since the output of each antenna of the array is dominated by the large skin backscatter, it needs to be removed without corrupting the useful tumor signal. To do that, a calibration signal can be generated for each antenna by averaging the time response of any other antenna [54]. This signal is then subtracted from the raw data as explained in Sec. 2.4.



(a) (b)

Figure 80: SKuRAD2 housed in the RF probe station (a) and all the components of the measurement setup (b).

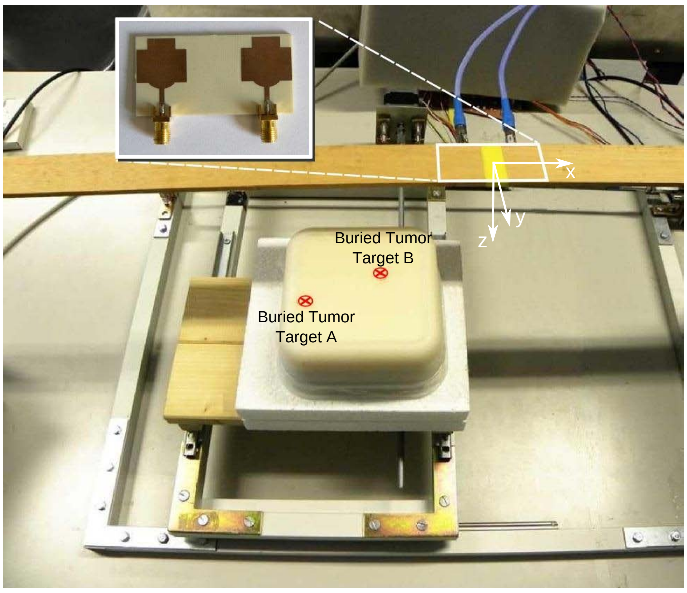


Figure 81: Photograph of the measurement setup during one imaging experiment.

5.2.3.3 *Imaging Results*

Using the measurement setup described in the previous section, a realistic breast cancer imaging experiment has been performed on the realized breast phantom. The target is placed on a wood plane moved by high-precision stepped motors and the antennas are installed on a rigid support over it. For each target position, the transceiver makes a full span measurement of the backscattered signals. Results are then transmitted to a personal computer and elaborated with Matlab.

A selection of significant images extracted by post-processing the raw data and corresponding to different planes are reported in Fig. 82. Fig. 82(a) shows the image of the $x-y$ plane at a distance $z = 7cm$ from the antennas. Dashed circles indicate the correct tumors positions. As shown, the two tumors are successfully detected, well confined and located at the correct position.

An image of the same plane obtained by using a commercial VNA in place of SKuRAD2 is reported in Fig. 82(b). The comparison between the obtained images shows that the last one is less confined and the tumors are not correctly located. This result may be affected by the lower dynamic range of the VNA with respect to SKuRAD2. In fact, taking into account the system dynamic range specification [2] together with the IF bandwidth and the transmitted power, the instantaneous VNA dynamic range results more than $20dB$ lower than SKuRAD2.

Fig. 83(a) shows the resulting phantom image over the $x-z$ cross section at $y = 10mm$. It clearly highlights the presence of tumor "B" while a shadow of tumor "A" is still visible due to its proximity in the y dimension. The measured radar image on the $y-z$ cross section for $x = 15mm$ is shown in Fig. 83(b). Only tumor "B" is visible in this case as tumor "A" is located $60mm$ away from the selected plane. However, a spurious trail of tumor "B" is also visible.

These results suggests that a dedicated high-dynamic range transceiver like SKuRAD2 can significantly improve the quality of the obtained image with respect to commercial VNAs, which are currently used in breast imaging system prototypes.

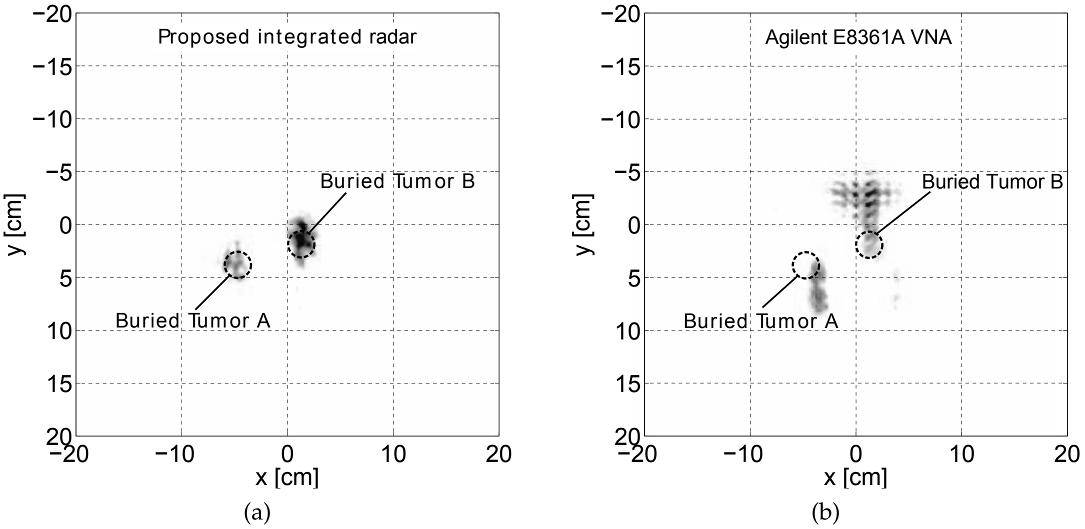


Figure 82: Measured radar image of the breast phantom with two buried tumors on the $x-y$ plane at a distance of $7\mathrm{cm}$ from the antennas. (a) Image obtained with the proposed microwave radar. (b) Image obtained with a commercial VNA. The real A and B tumors location is indicated by dashed circles and is ($x = -45\mathrm{mm}$; $y = 30\mathrm{mm}$) and ($x = 15\mathrm{mm}$; $y = 10\mathrm{mm}$), respectively.

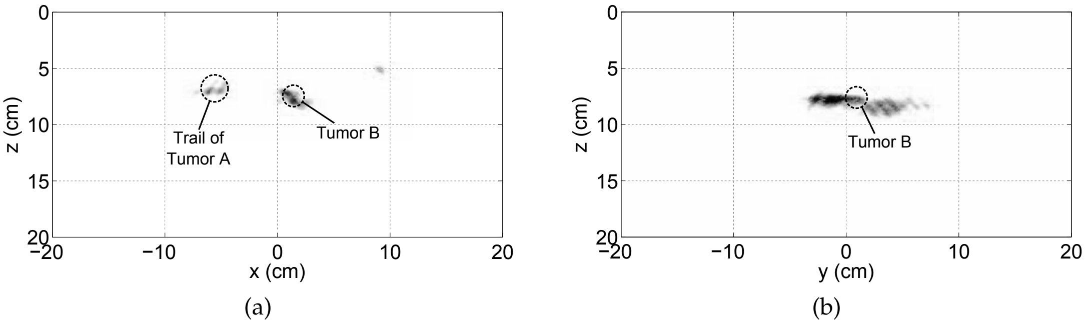


Figure 83: Measured radar image on the $x-z$ plane for $y = 1\mathrm{cm}$ (a) and measured radar image on the $y-z$ plane for $x = 1.5\mathrm{cm}$.

Part III

WIDEBAND BUILDING BLOCKS FOR PHASED ARRAY RADAR IN BICMOS TECHNOLOGY

6

SYSTEM OVERVIEW

Modern silicon technology offers transistors with very high transition frequency, more than 200GHz both in CMOS and SiGe. While being extremely fast, these transistors suffer from several limitations that affect their analog and RF performances. The low supply and breakdown voltages as well as the increased intrinsic noise of ultrascaled transistors limit the available output power and the receiver dynamic range.

However, some possibilities exist to enhance the performance of a system. The second part of this thesis, for example, presents the design of a high performance transceiver that, leveraging the stepped-frequency approach, achieves a dynamic range in excess of 100dB. Another approach that can be used to increase the overall performance of a transceiver is based on multiple antenna systems. A Phased Array (or timed array) configuration is a special case of such systems. It leverages the multiple antenna arrangement to obtain a higher Signal-to-Noise ratio (SNR) and hence a larger dynamic range [32]. Another feature is that in such systems it is possible to change the radiation pattern of the antenna array, useful both for radar and wireless communication systems.

To get more insight on Phased Array systems, consider the architecture shown in Fig. 84, that consists in a complete phased array receiver (it is worth to notice that the same considerations can be applied to a transmitter too). Here, the complete system is made by N different paths, each composed by a Variable Gain Amplifier (VGA) and a variable delay element. A linear antenna array composed by N equally-spaced antennas is connected to each receiver path. Notice that the choice of a linear antenna array is not unique. Other configurations are possible, both in 1 or 2 dimensions. The output signal is then obtained by summing together the contribution of each receiver.

As shown in Fig. 84, when a plane electromagnetic wave arrives at the antenna array at an angle α between the wave front and the array, the received signal of each antenna is shifted in time due to the difference in propagation path length. The delay difference ΔT between the signals of two adjacent paths is

$$\Delta T = \frac{d}{v} \sin \alpha, \tag{25}$$

where d is the physical spacing of the antennas and v is the propagation velocity of the electromagnetic wave in the medium. In the same conditions, the time delay ΔT_{tot} experienced by the last signal with respect to the one received from the first antenna is

$$\Delta T_{tot} = (N-1)\frac{d}{v}\sin\alpha, \tag{26}$$

where N is the total number of adjacent paths. Adjusting the time delay introduced by each path, a time-domain re-alignment of each signal is obtained. As a result, the time-delayed signals from the antenna array add coherently while the noise adds incoherently. This, valid as long as the antenna spacing is sufficient enough to consider uncorrelated the noise of each antenna from that of the other antennas, results in an improvement of the SNR [32].

From another point of view, a phased array architecture allows to change the radiation pattern of the antenna array. With a certain delay setting for each path, the system can be programmed to enhance the signal coming from one direction or to notch out signals coming from another direction. This feature is extensively used in phased array radars to electronically scan the volume around the antenna, reducing the scanning time and avoiding any mechanical displacement of the antenna. In a wireless communication system, instead, this feature allows to focus the irradiated power toward the desired receiver improving the SNR and hence increasing the maximum data-rate for a fixed Bit Error Rate (BER). Additionally, this feature is used to implement wireless link with a high degree of security level. In fact, if the receiver is placed in an angular position different from the correct one, the received constellation points are wrong. Thus, this makes impossible to recover the original data, even for very high sensitivity receivers [31].

Ideally, broadband variable delay elements are needed to make the signals from different paths coherent before they are combined. However, as will be better detailed out in Sec. 6.1, when the signal bandwidth is a small portion of the carrier frequency, a change of the delay can be approximated by a change of the phase shift. This simplification leads to four different system implementations depending on where the phase shift takes place. It can be implemented in the RF path (Fig. 85(a)), in the IF path (Fig. 85(b)), in the LO path (Fig. 85(c)) and in the digital domain (Fig. 85(d)). The choice of the selected architecture is accompanied by a trade-off between reliability, power consumption and implementation area.

A phase shift implemented at RF usually leads to lower power consumption since only one down-conversion and baseband is needed. Additionally, the combination of all paths in the RF domain allows to relax the linearity requirements of the IF stages due to the attenuation of large interferers coming from different positions. On the other hand, it requires a critical phase shifter implemented at RF which introduces additional losses.

A system based on the IF phase shifting architecture has the advantage of implementing the phase shift at a lower frequency with respect to that of the carrier. This solution can be simpler to implement and can use precision analog techniques [75, 57]. However, due to the presence of multiple down-conversion stages, it usually consumes more power. Moreover, IF combining means that both the LNA and the mixer experiences the full dynamic range of the input signal.

In the LO phase shifting scheme [68], the phase of the LO signal of each receiver path is changed accordingly with the phased array approach. This solution involves as many down-converters as the number of different paths. This leads, as in the previous case, to an increment of the total power consumption. The absence of the phase shifter in the signal path avoids any losses and linearity issues, however, the system bottleneck is shifted to the LO distribution network. Many power consuming buffers have to be used to drive each mixer with an appropriate LO amplitude. Moreover, a highly symmetric network is required to assure the correct phase at each mixer.

The digital phase shifting is the most flexible and power hungry implementation. It requires one down-converter as well as one ADC for each path. Due to the absence of a hardware summing block, the ADC has to feature a high dynamic range. Then, since all channels are directly sampled, the most powerful feature of this architecture is the possibility to receive, at the same time, signals coming from different angles.

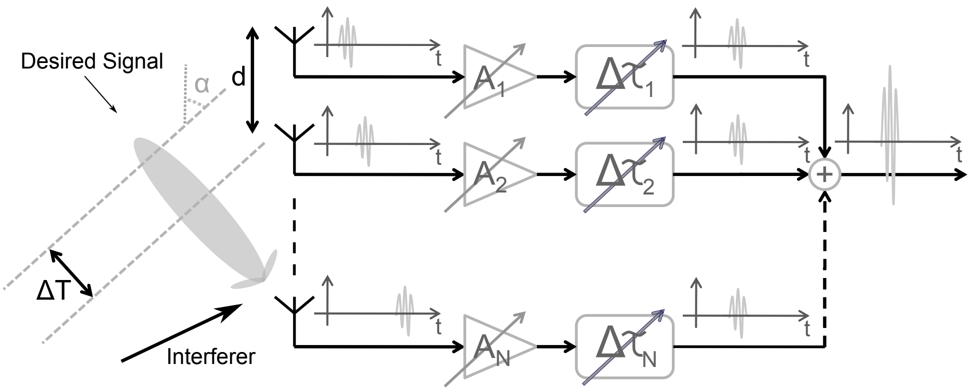
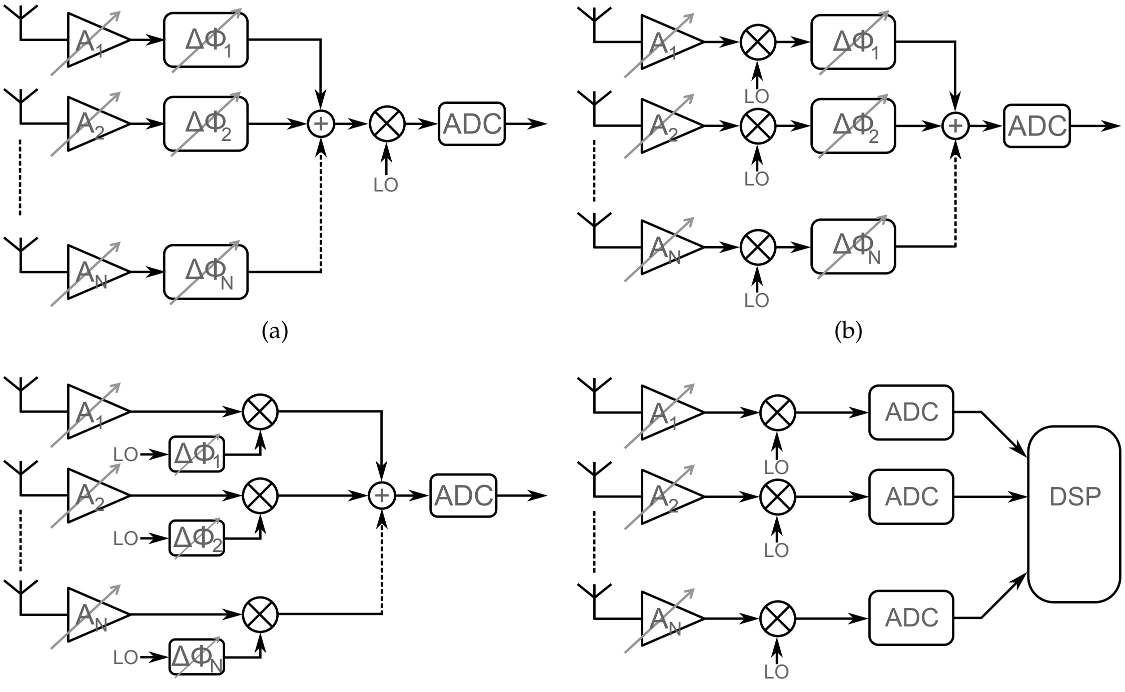


Figure 84: Simple example of a Phased Array receiver with N different input paths showing the modified antenna pattern.



(a) (b) (c) (d)

Figure 85: Simplified architectures showing the different position where the phase shift can take place. RF phase shifting (a), IF phase shifting (b), LO phase shifting (c) and Digital phase shifting (d).

6.1 PHASED ARRAY VS. TIMED ARRAY?

As stated in the introduction of this chapter, a phased array approach is based on the introduction of different time-delays in the different paths in order to re-align the received signals and add them coherently. In this context, therefore, the correct name of such systems is Timed Array (or Delayed Array) instead of phased array. However, generally, there are some implementation issues that make the design of a wideband variable time delay element difficult. Fortunately, in many practical applications, the required signal bandwidth is only a small fraction of the carrier frequency. In this scenario, for a narrow bandwidth, the time delay can be approximated by a phase shift. In the time-domain, it corresponds to a re-alignment of the phase of the carriers in the different paths. However, the modulated signals are not delayed properly. This introduces some dispersion in the modulated signals which increases the BER of a wireless communication system or reduce the radial resolution of an array-based radar [32]. Usually, if the fractional bandwidth is less than 20%, the loss in resolution and SNR is negligible [64].

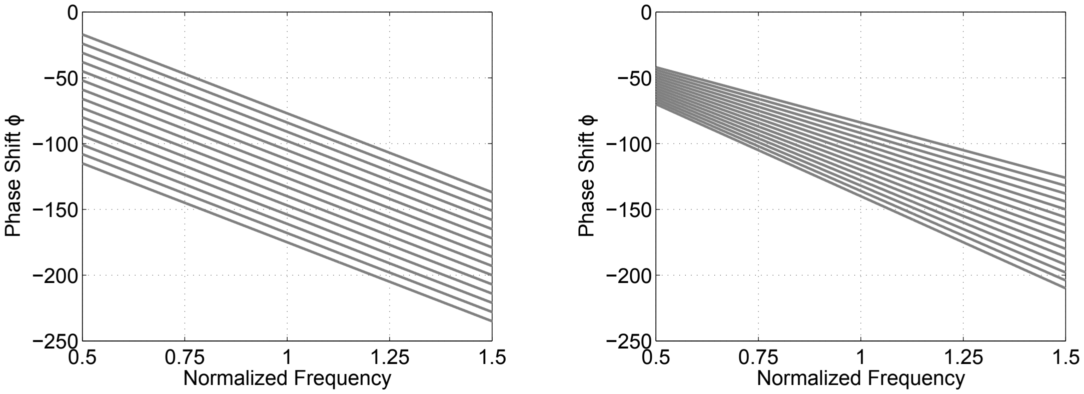
The ideal transfer function of a phase shifter and a delay element, here called True Time Delay (TTD), are shown in Fig. 86. Both of them should show 0dB loss in the frequency range of interest. Concerning the phase response, a phase shifter introduces a linear phase shift with respect to the frequency, having the same slope for each of the different shifting configurations (Fig. 86(a)). Similarly, a true time delay introduces a linear phase shift with respect to the frequency too. The big difference is that the slope of the phase is different for the different delay configurations (Fig. 86(b)). In other words, since the group delay (GD) is defined as the opposite of the slope of the phase shift with respect to the angular frequency $GD = -\frac{d\phi}{d\omega}$, a phase shifter and a true time delay show, between two configuration states, a constant phase shift difference and group delay difference, respectively.

In the real world, however, the transfer function of both the phase shifter and the true time delay is not lossless and infinitely wideband. Usually, both of them show an insertion loss that increases with frequency and change with a change in the delay (or phase) setting. Additionally, the constant time delay or phase shift difference experiences an additional ripple that can be neglected only over a small portion of the bandwidth.

Because of the different characteristics and the different intended applications, Sec. 7.1 presents the design of a wideband phase shifter and true time delay tailored for X-Band radar application. It is worth to remind that, even if a phase shifter can be used only in a narrowband context, a phase shifter with a wideband characteristic can be extremely useful if the transceiver operates over many narrowband channels.

6.2 MOTIVATION AND SYSTEM CHALLENGES

A phased array radar leverages the multiple antenna architecture to enhance the system performance. As an example, if a conventional single antenna system is replaced with a phased antenna array, the antenna pattern results electronically tunable. This feature can be employed at the transmitter side to efficiently transmit the power to the desired direction or, in a receiver context, to select signals coming from a specific point.



(a) (b)

Figure 86: Phase response of a Phase Shifter (a) and a True Time Delay element (b).

On the transmitter side, the high number of elements composing the phased array system allows an increase of the peak antenna directivity by a factor

$$D = 10 \log N, \tag{27}$$

where N is the number of elements. Similarly, since N transmitters irradiate the same amount of power, the effective radiated power is $10 \log N$ times greater than the case of a single antenna. This means that the antenna array features a total gain of $10 \log N^2$ with respect to a single transmitter connected to an omnidirectional antenna [4, 64]. This gain can also be achieved, for example, by means of a horn antenna. In this case, however, the gain cannot be steered in the desired direction, unless the antenna is mechanically steered.

In a phased array receiver, all the N received signals are added coherently, thus resulting in a power gain of $10 \log N^2$. Conversely, supposing enough spacing between antennas to consider each noise contribution uncorrelated from that of each other antenna, the noise is added incoherently. As a consequence, its power spectral density is incremented by a factor $10 \log N$. Overall, a net increment of the SNR by a factor of $10 \log N$ is achieved.

From a radar point of view, the resolution is one of its most important properties. A high resolution allows to detect small objects and to discriminate objects placed very close to each other. For a phased array radar, or, equivalently, for a timed array radar, there are two different kinds of resolution. As explained in Sec. 1.5, the slant-range resolution is essentially related to the bandwidth of the transmitted pulse. The higher the bandwidth, the shorter the pulse and therefore the higher the resolution. As visible in Fig. 87, instead, the angular resolution is directly related to the beamwidth. Assuming an uniform array of isotropic antennas, the beamwidth $\Delta\Theta$ at broadside (i.e. at a normal direction with respect to that of the antenna array) can be approximated to [64]

$$\Delta\theta \approx \frac{\lambda}{(N-1)d} = \left.\frac{2}{(N-1)}\right|_{d=\frac{\lambda}{2}}, \tag{28}$$

where N is the number of elements and d is the antenna-to-antenna spacing. Here, for simplicity, the variation of the beamwidth with the incident angle is not considered. However, it is worth to remind that both directivity D and beamwidth $\Delta\theta$ vary with the angle α (see Fig. 84), thus resulting in a reduction of the resolution for certain directions [64].

All the aforementioned properties of a phased array radar are directly related to the number of elements N. A high number of elements results in an improvement of both antenna directivity and receiver SNR. Additionally, the angular resolution is improved. This makes the choice of a highly-dense antenna array attractive. The trend is towards higher resolution, thus resulting in a higher carrier frequency and therefore even smaller wavelengths. This makes a fully discrete implementation of a high-N phased array radar impractical. As an example, a phased array implementation of a $77\mathrm{GHz}$ car radar requires an antenna spacing of only $\lambda/2 \approx 2\mathrm{mm}$.

Integrated circuits are able to satisfy both high resolution and the implementation of highly-dense antenna arrays. They allow to reduce the size of the complete system and to reduce the mismatch of the different paths. Overall, a high performance implementation is achievable. This, together with the high integration level, makes the integrated implementation an attractive solution.

An integrated solution, however, has also some drawbacks. First of all, to exploit the benefits introduced by a phased array approach, all the building blocks composing the single transceiver must have high performance. This means, essentially, low loss, low noise and high linearity. In such systems, the most critical block is the phase shifter (or, equivalently, true time delay). Considering an RF phase shifting implementation, the high demanded linearity makes a passive implementation preferable. But to keep losses low, a passive phase shifter usually implies high area consumption and therefore high implementation cost. A second challenge for an integrated solution is the mismatch and mutual coupling between different paths. Although the mismatch can be kept low with a compact layout, the interaction between the different phase shifters usually decrease with an increase of the path-to-path distance. This sets a direct compromise between area consumption, mismatch and mutual coupling. Since the mismatch and the low isolation level hamper the high resolution of the system, usually the area consumption is a second-order constraint. Other impairments affecting the resolution are the variation of the gain for different phase shifting configurations as well as the phase errors. Thus the targeted phase shifter design should have high linearity, low loss, small footprint and high resolution over a wide bandwidth.

A power combiner is used to collect and combine the signals elaborated by each path. As visible in Fig. 88, in a conventional implementation only two paths are combined at a time. This results in a total $(N-1)$ power combiners and a combiner depth of $\log_2 N$ (if, as usual, N is a power of 2). In order not to waste the additional gain introduced by a phased array architecture, this block must feature low loss. Furthermore, the large amount of required combiners sets the area consumption as an important constraint.

Sec. 7.1 and 7.2 present the design of a phase shifter, true time delay and power combiner tailored for an RF phased array architecture in the X-Band. The designs are optimized to feature low loss, wideband characteristic and low area consumption.

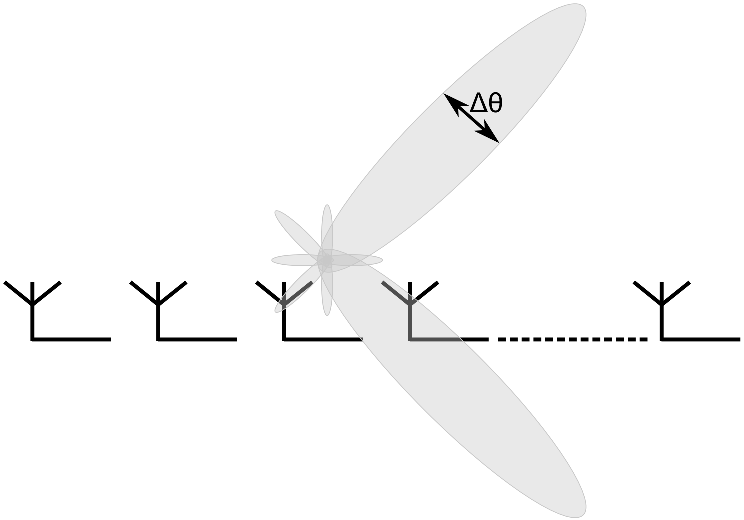


Figure 87: Definition of the angular resolution of a phased array radar.

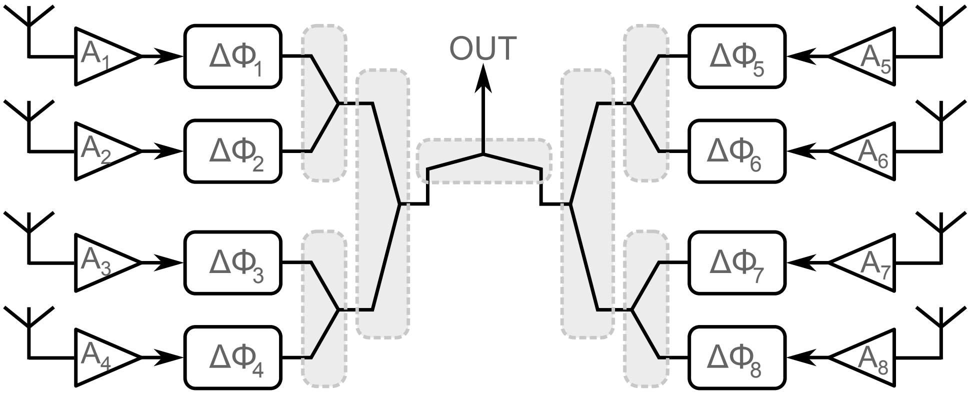

OUT
A1
A2
A3
A4
ΔΦ1
ΔΦ2
ΔΦ3
ΔΦ4
ΔΦ5
ΔΦ6
ΔΦ7
ΔΦ8
A5
A6
A7
A8

Figure 88: Example of a conventional 8-channels phased array receiver with the usual power combining scheme.

7

BUILDING BLOCK DESIGN

7.1 PHASE SHIFTER AND TRUE TIME DELAY

As explained in details in Chapter 6, a timed array radar is composed by a set of transceivers whose time delay can be programmed to compensate for the difference in the propagation path length. This results in a variable antenna pattern with several improvements on the transmitter as well as on the receiver side.

The building block that allows the time-domain translation of the different signals is called True Time Delay (TTD). Since the time delay doesn't depend on the signal's frequency, the TTD can be used even in ultrawideband systems. However, the design of a wideband high-performance true time delay is not trivial if the carrier frequency is in the order of tens of GHz. Fortunately, in many narrowband applications, the real time-delay can be approximated with a constant phase shift over a small bandwidth [32], leading to a system called phased array radar. For small arrays, and depending on the desired application, the error introduced by the phase shifter can be considered negligible as long as the fractional bandwidth is smaller than 20% [4].

Of the four different system implementations discussed in Chapter 6, the RF path phase shifting is the most simple and promising architecture in terms of low components count and power consumption. It is the best choice when the number of elements of the antenna array become large. Unlike the LO path implementation, additionally, it accommodates both narrow and wideband systems simply replacing the phase shifter with a true time delay. On the other hand, the design of the RF phase shifter/TTD may be challenging since its non-idealities directly affect the RF performances. As in the IF phase shifting configuration, one way to obtain the desired phase shift is to combine I and Q signals with different amplitudes [73, 43, 48]. However, the higher frequency with respect to the IF case makes the combination less robust and more difficult. Additionally, the presence of active devices in the RF path limits the linearity performance. For these reasons, a passive implementation is usually preferred. Common passive phase shifter designs are based on the switching between all-pass/band-pass circuits [76]. The switch, however, may introduce phase errors and reduce the linearity. Moreover, a high number of different sections are needed if the required resolution is high. To limit the number of sections with different phase shifting values, a combination of switchable low-pass/high-pass network followed by a continuously tunable circuit can be adopted [33]. To reduce the area consumption for a given phase shift value, phase shifter based on 90° hybrid coupler are presented [14, 94, 91]. The presence of the hybrid coupler, however, limits the maximum fractional bandwidth. In a purely timed array architecture, a true time delay is used instead of a phase shifter. A conventional passive true-time-delay is based on a loaded transmission line [50, 62]. Due to the distributed nature of this implementation, it occupies a large area. To keep the area consumption low, a lumped element approach can be used [19].

The proposed phase shifter and true time delay are realized with a cascade of several identical lumped elements hybrid cells. Each hybrid cell is based on the combination of a ladder and lattice structure. The ladder topology is a low-pass structure that shows an increasing group delay with the frequency. On the contrary, the lattice topology is an all-pass structure that shows a decreasing group delay with the frequency. Thus, the combination of the two structures results in a group delay compensation and an enhancement of the bandwidth.

This section is organised as follows. Sec. 7.1.1 describes the hybrid cell concept and derives the major characteristics in terms of circuit parameters. Sec. 7.1.2 describes the design of an X-band BiCMOS TTD while Sec. 7.1.3 presents a way to increase the variable group delay by adding some fixed delay structures. Finally, Sec. 7.1.4 presents the X-Band BiCMOS phase shifter design and explains the major varactor-related impairments that affect its correct operation.

7.1.1 *Hybrid Cell Concept*

Transmission lines are distributed low-pass sections showing a constant characteristic impedance that depends on the geometry only. They are used to connect two high-frequency circuits placed apart from each other and their use is mandatory when the connection length approaches the wavelength of the transmitted signal. A transmission line is a wideband structure. However, when it is used to create some microwave circuits (i.e. Wilkinsons combiners, Couplers, Circulators etc.) it occupies a relatively large area. A high level of miniaturization can be achieved by using a lumped-element transmission line. Each distributed low-pass section is replaced by an LC low-pass filter where L and C are the lumped inductor and capacitor, respectively. Here, the characteristic impedance of a line composed by a cascade of some LC sections depends on the values of the lumped elements.

Reference [49] presents a way to increase the operating bandwidth of a lumped-element transmission line for PCB purposes. It combines ladder and lattice structures to obtain a hybrid cell with a compensated group delay. Similarly, we propose a monolithic hybrid cell composed by lumped inductors and capacitors. If the capacitors are replaced by varactors, the simple transmission line can be used as a phase shifter/true time delay element with an efficient area consumption and wideband characteristics.

Let's now see more in detail the working principle of the proposed solution. As sketched in Fig. 89, the hybrid cell is realized as a combination of a differential low-pass and all-pass structure. Since the low-pass and all-pass networks show an increasing and decreasing group delay with the frequency, respectively, the resulting hybrid cell exhibit wideband delay characteristics. To get more insight about the combined structure, consider the normalized ABCD matrix

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \frac{1}{1-Z_L Y_{C2}} \begin{bmatrix} 1+Z_L(Y_{C2}+2Y_{C1}) & 2Z_L \\ 2(Z_L Y_{C1}^2 + Z_L Y_{C1} Y_{C2} + Y_{C1} + Y_{C2}) & 1+Z_L(Y_{C1}+2Y_{C1}) \end{bmatrix}, \tag{29}$$

where $Z_L = i\omega L/Z_0$, $Y_{C1} = i\omega C_1 Z_0$, $Y_{C2} = i\omega C_2 Z_0$ and Z_0 is the source/load impedance. Therefore, the differential-mode characteristic impedance Z_{0C} of a chain composed by a cascade of such cells can be obtained from

$$S_{11} = \frac{A+B-C-D}{A+B+C+D} = 0 \Rightarrow Z_{0C} = \sqrt{\frac{L}{C_1+C_2}\left[1-\frac{\omega}{\omega_c}\right]^2}, \tag{30}$$

where $\omega_c = 1/\sqrt{LC_1}$ is the cutoff angular frequency of the line. Eq. 30 clearly shows the dependence of the characteristic impedance from the circuit parameters. Particularly, a small C_1 results in a high cutoff frequency.

The use of varactors as C_1 and C_2 allows to change the characteristics of the lumped transmission line. As will be discussed in details in the following sections, if the values of C_1 and C_2 are properly chosen, the cell is able to behave both as a phase shifter (constant phase shift) or a true time delay (constant group delay). As an anticipation, if $C_1 << C_2$ the cell behaves like a phase shifter. On the contrary, if $C_1 \approx 2C_2$ the cell behaves like a delay element with a compensated group delay.

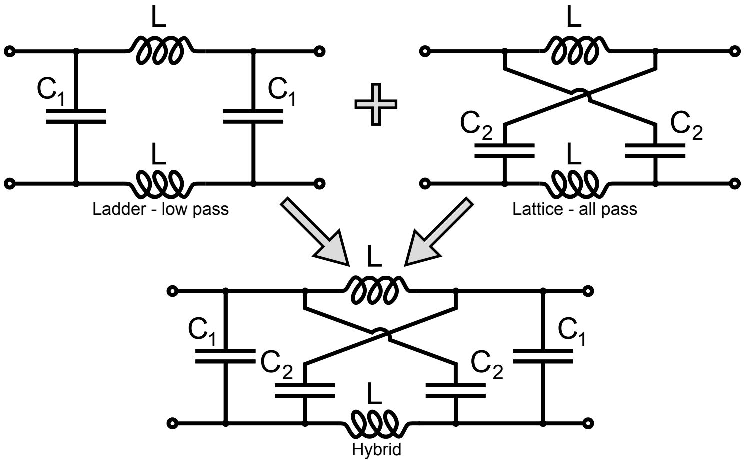


Figure 89: Creation of the hybrid cell as a combination of a ladder and lattice structure.

7.1.2 *True Time Delay Design*

As anticipated in Sec. 7.1.1, the hybrid cell is able to behave both like a phase shifter or a true time delay. Consider now the case where all the capacitors are present. From the normalized ABCD matrix of the structure (Eq. 29) one can obtain the transmission coefficient of the cell

$$S_{21} = \frac{2}{A+B+C+D} = \frac{1-Z_L Y_{C2}}{1+Z_L Y_{C2} + 2Z_L Y_{C1} + Z_L + Y_{C1} + Y_{C2} + Z_L Y_{C1}(Y_{C1}+Y_{C2})}.$$

(31)

Thus, the phase shift introduced by the single cell is

$$\phi = -\arctan\left\{ \frac{\omega\left[\frac{L}{Z_0} + (C_1 + C_2)Z_0 - \omega^2 L C_1 (C_1 + C_2) Z_0\right]}{1 - \omega^2 L (C_2 + 2C_1)} \right\}. \tag{32}$$

Finally, the group delay τ_g, defined as the opposite of the derivative of the phase shift with respect to ω, is

$$\tau_g = -\frac{d\phi}{d\omega} = \frac{\left[\frac{L}{Z_0} + (C_1 + C_2)Z_0\right]\left[1 + \omega^2 L(C_2 + 2C_1)\right] - \omega^2 L C_1 (C_1 + C_2) Z_0 \left[3 - \omega^2 L (C_2 + 2C_1)\right]}{\left[1 - \omega^2 L (C_2 + 2C_1)\right]^2 + \omega^2 \left[\frac{L}{Z_0} + (C_1 + C_2)Z_0 - \omega^2 L C_1 (C_1 + C_2) Z_0\right]^2}. \tag{33}$$

A more useful form of Eq. 33 is obtained calling $C_T = (C_1 + C_2)$ and $C_1 = \gamma C_T$

$$\tau_g = \frac{\left[\frac{L}{Z_0} + C_T Z_0\right]\left[1 + \omega^2 L C_T (1 + \gamma)\right] - \omega^2 L \gamma C_T^2 Z_0 \left[3 - \omega^2 L C_T (1 + \gamma)\right]}{\left[1 - \omega^2 L C_T (1 + \gamma)\right]^2 + \omega^2 \left[\frac{L}{Z_0} + C_T Z_0 - \omega^2 L \gamma C_T^2 Z_0\right]^2}. \tag{34}$$

When the matching condition occurs, i.e. the source/load impedance Z_0 equals the characteristic impedance of the structure $Z_{0C} = \sqrt{L/C_T}$, the group delay of the single cell can be written as

$$\tau_g = \frac{\sqrt{LC_T}\left\{2 + \omega^2 L C_T \left[2 - \gamma + (1 + \gamma)\omega^2 L \gamma C_T\right]\right\}}{\left[1 - \omega^2 L C_T (1 + \gamma)\right]^2 + \omega^2 L C_T (2 - \omega^2 L \gamma C_T)^2}. \tag{35}$$

Fig. 90 plots the group delay of a single cell when the matching condition is verified. Concerning an ideal hybrid cell (infinite quality factor for both inductors and capacitors), the best group delay compensation between lattice and ladder topologies occurs when the parameter γ approaches 0.6. In practice, the quality factor of passive devices can be small. The effect of circuit losses tends to shift the optimum γ towards higher values. As an example, taking a reasonable quality factor of $Q_L = Q_C = 15$ for both inductors and capacitors, the value of γ at which the group delay is maximally flat is $\gamma \approx 0.7$, that corresponds to a capacitance ratio of $C_1/C_2 \approx 2$. A larger value of γ results in a ripple in the group delay that, if tolerated, leads to a wider bandwidth.

As shown in Fig. 90, when γ is properly chosen, the group delay introduced by a single cell is constant from DC up to frequencies near the cutoff frequency of the structure. Hence, a simple and rapid estimation of the group delay when the matching condition occurs is

$$\tau_{g,DC} = \lim_{\omega \to 0} \tau_g = 2\sqrt{LC_T}, \tag{36}$$

which gives a rule of thumb on the selection of the component values. The larger the inductance and capacitance, the higher the group delay.

A variable delay element is able to change the group delay depending on the state of a control signal. Eq. 36 suggests that the proposed cell can do that by simply changing

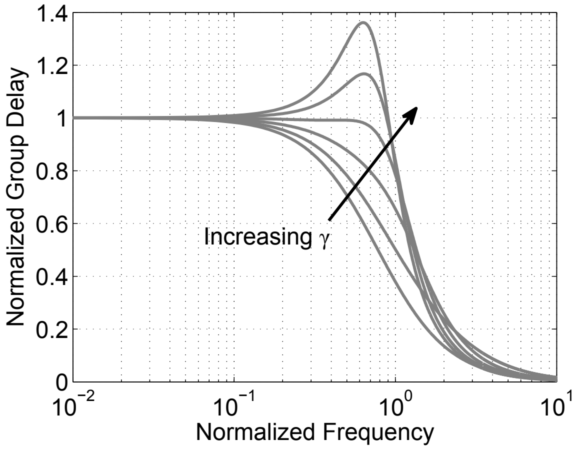


Figure 90: Normalized Group Delay of a single Hybrid cell for different values of γ in the range $[0; 1]$ (step of 0.2). X-axis has been normalized to the cutoff frequency of the structure $(1/\sqrt{LC_1})$ when $\gamma = 0.6$. No component losses have been taken into account.

the total capacitance or the inductor value. In an integrated circuit the variation of the capacitance is achieved by replacing capacitors C_1 and C_2 with varactors, whom must be driven together to maintain the optimal value of γ. However, the change of capacitors value leads to a change of the characteristic impedance of the cell Z_{0C}. Since the source and load impedances are fixed, the cell cannot be perfectly matched both when the total capacitance is minimum $(C_{T,min})$ and maximum $(C_{T,max})$. Therefore Eq. 36 and Eq. 35 are no longer valid and the group delay difference $\Delta\tau_g$ between maximum and minimum capacitance value must be derived from Eq. 34

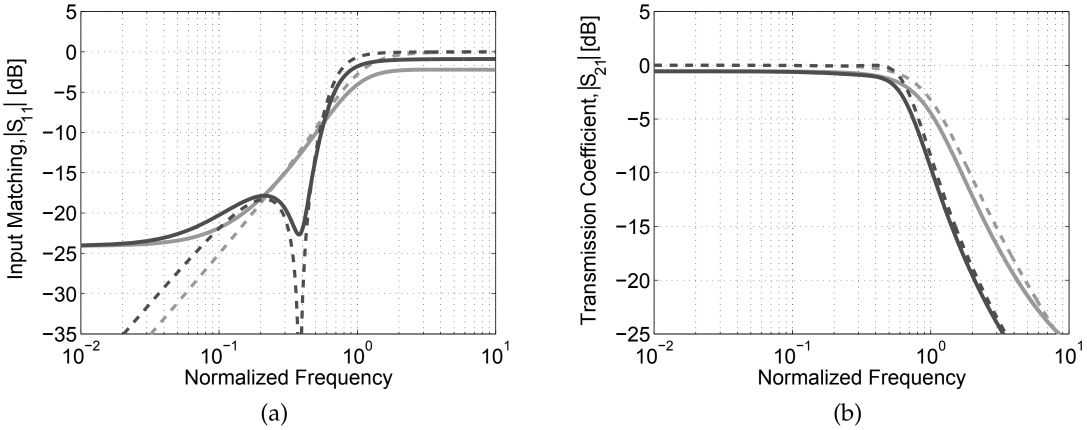
$$\Delta\tau_{g,DC} = \tau_{g,DC|C_{T,max}} - \tau_{g,DC|C_{T,min}} = (\alpha - 1)C_{T,min}Z_0, \tag{37}$$

where $\alpha = C_{T,max}/C_{T,min} = C_{1,max}/C_{1,min} = C_{2,max}/C_{2,min}$ and Z_0 is the source/load impedance. A good matching condition for both maximum and minimum capacitance value is verified when the source/load impedance Z_0 is the geometrical mean of the minimum $Z_{0C,min}$ and maximum $Z_{0C,max}$ characteristic impedance of the cell: $Z_{0,opt} = \sqrt{Z_{0C,min}Z_{0C,max}}$. In this condition, the group delay difference can be expressed as

$$\Delta\tau_{g,DC} = \frac{(\alpha - 1)}{\sqrt[4]{\alpha}}\sqrt{LC_{T,min}}, \tag{38}$$

which shows the dependence of the delay variation from the components values as well as the capacitance ratio α. A higher ratio between C_{max} and C_{min} results in a larger delay variation per cell. However, the change of the capacitance leads to a change of the characteristic impedance of the structure. As a result, a higher α causes a lower input matching which is associated with a higher insertion loss. Typically, a capacitance ratio $\alpha \leqslant 4$ is sufficient to guarantee an input matching better than -15dB.

Fig. 91 compares the $|S_{11}|$ and $|S_{21}|$ parameters of a single hybrid cell when capacitors and inductors are considered as components with finite $(Q_L = Q_C = 15)$ or infinite $(Q_L = Q_C = \infty)$ quality factor. As shown, the input matching is better than -10dB while the insertion loss is small and constant up to frequencies comparable with the cutoff frequency of the cell $f_c = 1/(2\pi\sqrt{LC_1})$. Additionally, it is worth to notice that,



(a) (b)

Figure 91: Input matching $|S_{11}|$ (a) and transmission coefficient $|S_{21}|$ (b) of a single hybrid cell in the C_{min} (light gray) and C_{max} (dark gray) states ($\alpha = C_{max}/C_{min} = 2.5$). Dashed and solid curves refer to a lossless and finite $Q_L = Q_C = 15$ case, respectively. X-axis has been normalized to the cutoff frequency of the structure in the $C_{1,min}$ state.

within the bandwidth, both insertion loss and input matching are mainly affected by the quality factor of the inductance only. With reasonable component values, the proposed cell can obtain a delay variation of more than 4ps with an insertion loss smaller than 0.5dB.

7.1.2.1 *X-Band BiCMOS Implementation*

The previous section explained the working principle of a variable delay element based on a hybrid cell architecture. Due to its wideband characteristics, its low insertion loss and its relatively simple implementation, it is a good candidate to realize a variable delay element tailored for timed array radars. This section describes the design of an X-Band true time delay implemented in a BiCMOS technology and gives some guidelines on the choice of the component values. Additionally, it presents a layout that minimizes the area consumption and the unwanted parasitics.

As explained in Sec. 6.2, a timed array radar is realized by N transceivers connected to N antennas. All the benefits of such architecture increase with an increase of the number of transceivers. Thus, a high integration is needed to keep the system compact and to reduce the implementation costs.

The variable delay element is the most important block of a timed array architecture. The proposed true time delay is based on the hybrid cell presented in Sec. 7.1.2. To implement the variable delay feature, capacitors C_1 and C_2 are replaced by MOS varactors that are driven in a digital fashion. This results in an easier delay selection and allows to take advantage of the BiCMOS technology to implement some logic or calibration without the need of area and power-hungry DACs.

As said, the designed true time delay is tailored for the operation in the X-Band. The design is a proof-of-concept only. Hence the achieved variable delay is only $\approx$ 25ps. This is not a limiting factor since a higher delay can be obtained simply cascading a larger number of cells. According to Eq. 38, to maximize the variable delay per cell, large inductors and varactors are needed. However, larger component values result in a lower cutoff frequency. Thus, an upper bound on the product LC_1 exists. Additionally, the circuit context sets the characteristic impedance Z_0, hence the ratio of the inductance and the total capacitance is fixed. In this case, $Z_0 = 75\Omega$.

The schematic of the single hybrid cell is shown in Fig. 92(a). As anticipated, the variable delay is obtained replacing capacitors C_1 and C_2 by MOS varactors. Two varactors for each capacitor guarantee two different delay levels for each cell. A larger number of delay levels is possible. However, a large number of small varactors increases the parasitic capacitances and decreases the C_{max}/C_{min} ratio. As visible in Fig. 92(b), two partially overlapped inductors take advantage of the mutual inductance to achieve the desired differential-mode inductance with a smaller footprint. To further reduce the cell area, all the varactors are placed under the transformer.

The transformer is made of a 1.5 turns pseudo-oval inductors. As will be explained in Sec. 7.1.4.1, the parasitic inductance of long traces in the varactor paths can affect the operation of the cell. To minimize this unwanted effect, the cross connection in the C_2 varactor paths is implemented at inductor-level and the connection length is minimized thanks to the oval layout of the transformer. Additionally, C_2 paths are realized by means of microstrip transmission lines. This reduces the parasitic inductance of the connections. An oval layout is also capable to reduce the total length of the structure if the cells are placed forming a linear chain. Others cell arrangements are also possible.

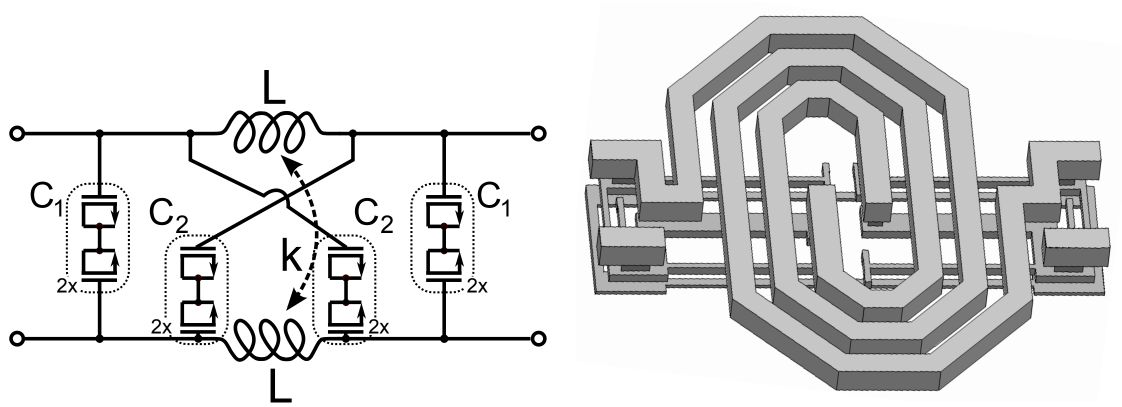
The cell occupies an area of $105\text{x}100\mu m^2$. To keep the inductor quality factor high, the trace width is $5\mu m$. Compared with a purely octagonal implementation, the oval layout does not impair the quality factor significantly. The trace-to-trace spacing is $4\mu m$ that allows to reduce the parasitic capacitance between the different inductors and hence maximize the cutoff frequency and the C_{max}/C_{min} ratio.

The parameters of the proposed hybrid cell are: a single-ended inductance of $L = 245pH$ with a quality factor of $Q_L = 13@10GHz$, a transformer coupling factor of $k = 0.24$, minimum varactor capacitances of $C_{1,min} = 12fF$ and $C_{2,min} = 8fF$ and a capacitance ratio of $\alpha \approx 2.7$. As one can observe, a smaller C_1/C_2 ratio with respect to the optimal one (as described in Sec. 7.1.2 the ideal C_1/C_2 ratio is ≈ 2) is chosen due to the parasitic capacitances of the transformer that increase the value of C_1. Taking into account these parasitics, the cell exhibit a characteristic impedance from $Z_{0C,min} = 65\Omega$ to $Z_{0C,max} = 83\Omega$. Thus the optimal characteristic impedance is $Z_0 = \sqrt{Z_{0C,min} Z_{0C,max}} = 73.4\Omega$. With these values, each cell achieves a variable delay of $\approx 2.4ps$. Thus, a cascade of at least 11 cells are needed to cover the desired variable delay of $25ps$ with a resolution of $\approx 1.2ps$. This results in a total area of $11\text{x}105\mu m\text{x}100\mu m \approx 0.12mm^2$.

7.1.3 *Extending the Group Delay Variation*

As explained in Eq. 26, a correct system operation requires a total variable delay that depends on the physical characteristics of the antenna array and on the signal incident angle. A larger antenna array requires a larger variable delay. Fortunately, a delay of few tens of picoseconds is enough for many applications. However, when a large antenna array is used, the demanded variable delay could be extremely large, even in the order of hundreds of picoseconds.

The first approach to achieve a variable delay on the order of few hundreds of picoseconds consists in cascading a large number of hybrid cells. As an example, a delay of $\approx 200ps$ is achieved by a chain of approximately 80 TTD cells. This would result in a



(a) (b)

Figure 92: Proposed true time delay cell schematic (a) and transformer layout (b). The cell dimension is $105x100\mu m^2$.

huge area consumption of $\approx 0.8mm^2$ per channel only for the true time delay. In addition, even if the insertion loss of the single cell is very small, a total loss of $30-40dB$ would occur. This makes this implementation impractical.

A coarse and fine tuning can be implemented in a true time delay to increase the effective delay variation [58]. The main idea is to cascade a switchable fixed delay block followed by a small chain of variable delay elements. This arrangement results in a lower area consumption as well as a lower insertion loss.

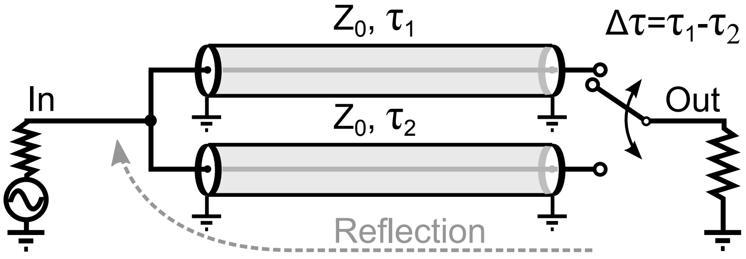
A simple way to obtain the desired behavior is to multiplex between transmission lines with different length (different group delay), as visible in Fig. 93(a). However, when a single multiplexer is placed at the output (input) of the lines, the reflected signal of the unmatched transmission line impairs the correct operation of the system. This unwanted effect may be attenuated matching the output (input) of the unused transmission line. This solution leads to an additional power consumption. Moreover, a little mismatch between the load impedance and the characteristic impedance of the transmission line generates some reflections that limit the bandwidth of the system. A configuration that avoids the aforementioned issue is visible in Fig. 93(b). It consists of a multiplexer placed both at the input and output of the transmission lines. This ensures the complete separation of the two paths and forces the signal to flow only through one delay element.

One of the major constraint in large timed array systems is the area consumption of each transceiver. In a coarse/fine TTD architecture, a continuous variable delay is achieved when the total variable delay covers one coarse tuning step with margin. The choice of the coarse delay step plays a fundamental role in minimizing the chip area. A smaller step results in a smaller variable TTD chain. However, more coarse delay steps are needed to cover the desired total delay. On the other hand, a larger step results in a smaller number of coarse tuning steps, but a larger variable true time delay chain. The final system (coarse and fine tuning elements) is designed for a total delay variation of $200ps$. A coarse tuning step of $40ps$ is a good compromise between area consumption and insertion loss of the entire structure.

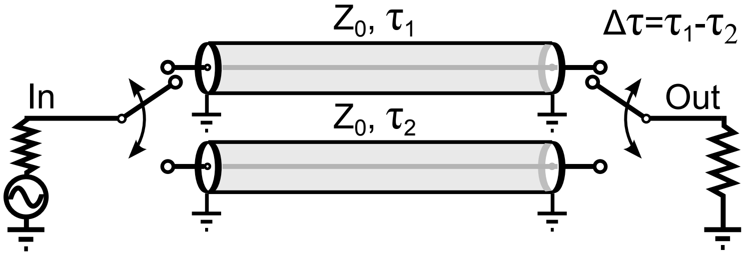
The block diagram of the proposed coarse/fine tuning delay element is shown in Fig. 94. It is composed by a cascade of two coarse delay elements (CDE) followed by a chain of hybrid cells that guarantees a variable group delay of $40ps$ (FDE). Each CDE allows to select the desired group delay from three possibilities: τ_0, $\tau_0 + 40\text{ps}$ and $\tau_0 + 80\text{ps}$. Hence, it features a maximum variable GD of 80ps with a step of 40ps.

The schematic of the CDE is shown in Fig. 95. It is composed by a single emitter-degenerated pseudo-differential pair and three parallel double-cascode paths. The biasing of the structure is programmable, such that only one path is active at a time. The fixed (but different for each path) delay element is placed between the two cascode transistors. This results in a low current consumption since the same current biases both the input and output multiplexer. A correct matching of the delay lines is mandatory to ensure a wideband operation. This is done by resistor R_1 and resistor R_2 in series with the input impedance of the upper cascode.

The smallest group delay τ_0, which is associated to the zero delay state, is obtained by means of a small differential transmission line. The 40ps step, instead, is achieved by a cascade of 2 fixed hybrid cells that use MIM capacitors instead of varactors. The cascade of 2 cells allows the use of smaller components with respect to a single cell implementation, and hence increases the cutoff frequency of the structure ($1/\sqrt{LC_1}$). The last step of 80ps is achieved by a cascade of 4 identical hybrid cells.


Z_0, τ_1
$\Delta\tau=\tau_1-\tau_2$
In
Out
Z_0, τ_2
Reflection

(a)


Z_0, τ_1
$\Delta\tau=\tau_1-\tau_2$
In
Out
Z_0, τ_2

(b)

Figure 93: Scheme of principle of a coarse-tuning delay system. Simple implementation using 1 multiplexer (a) and improved architecture that completely separates the two paths (b).

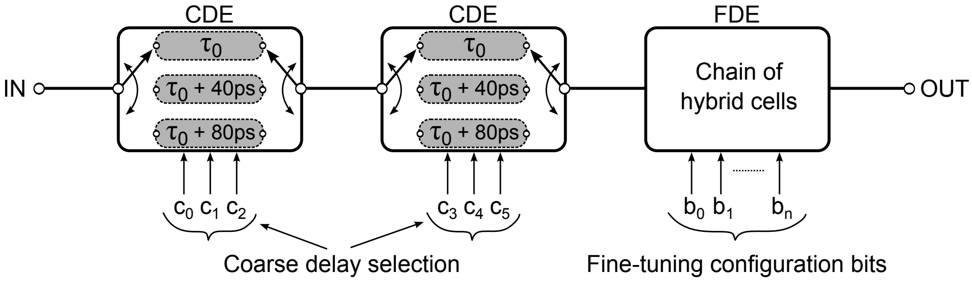

CDE
CDE
FDE
IN
OUT
τ_0
τ_0 + 40ps
τ_0 + 80ps
Chain of hybrid cells
c_0 c_1 c_2
c_3 c_4 c_5
b_0 b_1 b_n
Coarse delay selection
Fine-tuning configuration bits

Figure 94: Block diagram of the coarse/fine tuning true time delay.

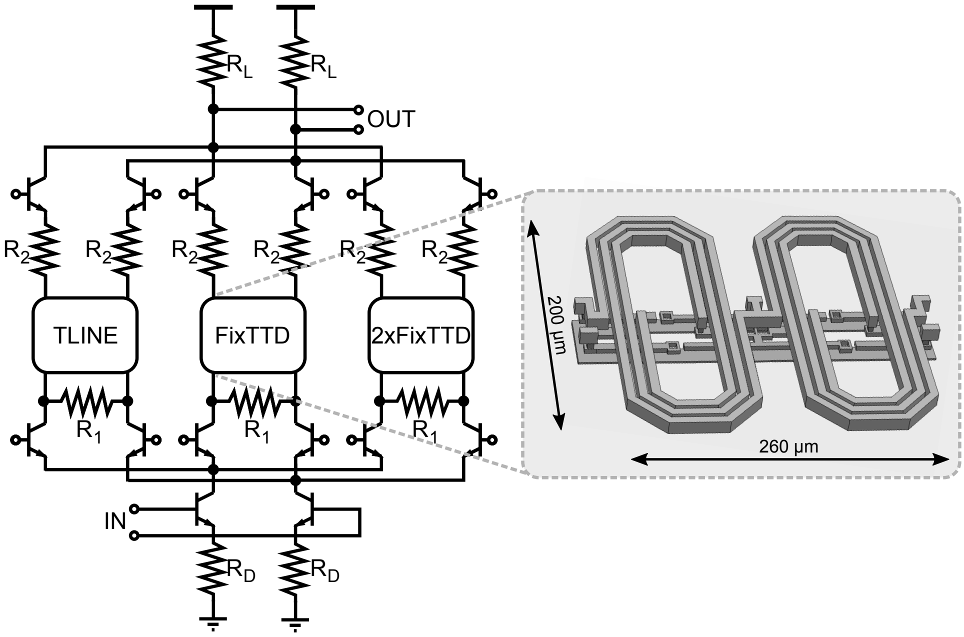


Figure 95: Schematic of the proposed coarse delay element showing the layout of the 40ps delay cell. The total area is 640x580μm^2.

7.1.4 *Phase Shifter Design*

Sec. 7.1.2 describes the working principle of the hybrid cell used as a true time delay element. However, as anticipated in Sec. 7.1.1, depending on the capacitance ratio C_1/C_2, the same cell is able to behave both as a true time delay or as a phase shifter.
Consider now the case where $C_1 = 0$ and only the capacitance C_2 is present. Under this assumption, the hybrid cell reduces to an all-pass lattice structure. From the normalized ABCD matrix of the cell (Eq. 29) one obtains the transmission coefficient S_{21}

$$S_{21} = \frac{2}{A+B+C+D} = \frac{1 - Z_L Y_{C2}}{1 + Z_L Y_{C2} + Z_L + Y_{C2}}, \tag{39}$$

where $Z_L = i\omega L/Z_0$, $Y_{C2} = i\omega C_2 Z_0$ and Z_0 is the source/load impedance. The characteristic impedance of a line composed by a cascade of several lattice cells is

$$Z_{0C} = \sqrt{\frac{L}{C_2}}, \tag{40}$$

that, compared to the hybrid solution, shows the absence of the cutoff frequency. An expression of the transmission coefficient S_{21} in terms of the circuit parameters is

$$S_{21} = \frac{1 + \omega^2 L C_2}{1 - \omega^2 L C_2 + i\omega\left[\frac{L}{Z_0} + C_2 Z_0\right]}. \tag{41}$$

Thus, the absolute phase shift introduced by a single cell is

$$\phi = -\arctan\left\{\frac{\omega\left[\frac{L}{Z_0} + C_2 Z_0\right]}{1 - \omega^2 L C_2}\right\}, \tag{42}$$

which shows the dependence of the phase shift from the circuit parameters. Like in the TTD case, a variable phase shift is obtained by changing the value of the inductors or capacitors. A simple way to do that in an integrated circuit is to replace the capacitance C_2 with a varactor. The phase difference between minimum and maximum varactor configuration is

$$\Delta\phi = \phi_{C2,min} - \phi_{C2,max} = -\arctan\left\{\frac{\omega C_{2,min} Z_0 (1-\alpha)\left[1+\left(\frac{\omega L}{Z_0}\right)^2\right]}{1+\omega^4 L^2 \alpha C_{2,min}^2 + \omega^2\left[\frac{L^2}{Z_0^2}+\alpha C_{2,min}^2 Z_0^2\right]}\right\}, \tag{43}$$

where $C_{2,min}$ is the minimum varactor capacitance and α is the ratio between its maximum and minimum capacitance value. Fig. 96 shows the phase difference of the cell, normalized with respect to its peak value, when the varactor is in its minimum and maximum capacitance value. As visible, this difference has a peak around $f_{\Delta\phi,max}$. The cell covers a fractional bandwidth of 100% or $\approx$ 30% if the tolerated phase error is 10% or 1% of the maximum phase difference, respectively. This demonstrates the wideband nature of the proposed phase shifter.

The frequency $f_{\Delta\phi,max}$ where the phase difference is maximum can be obtained by setting to zero the derivative of Eq. 43 with respect to ω. It results

$$f_{\Delta\phi,max} = \frac{Z_{0C,max}}{Z_0}\frac{1}{2\pi\sqrt{\alpha L C_{2,min}}}, \tag{44}$$

where $Z_{0C,max}$ is the characteristic impedance of the cell when the capacitor C_2 is in its minimum value. When the source/load impedance Z_0 is set to the geometric mean between $Z_{0C,min}$ and $Z_{0C,max}$, Eq. 44 reduces to

$$f_{\Delta\phi,max} = \frac{1}{\sqrt[4]{\alpha}}\frac{1}{2\pi\sqrt{L C_{2,min}}}. \tag{45}$$

The maximum value of the phase difference can be obtained from Eq. 44 and Eq. 43

$$\Delta\phi_{max} = -\arctan\left\{\frac{\frac{1-\alpha}{\sqrt{\alpha}}\left[1+\frac{L^2}{\alpha C_{2,min}^2 Z_0^4}\right]}{2\left[1+\frac{L^2}{\alpha C_{2,min}^2 Z_0^4}\right]}\right\} = -\arctan\left[\frac{1-\alpha}{2\sqrt{\alpha}}\right], \tag{46}$$

which shows that the maximum phase difference introduced by a single phase shifter cell depends on the ratio $\alpha = C_{2,max}/C_{2,min}$ only. A larger α results in a larger phase difference per cell. However, as in the TTD case, a change of the capacitance leads to a change of the characteristic impedance of the network. Hence, a lower input matching and a higher insertion loss occur. Since integrated varactors easily have a capacitance ratio larger than 2, a single cell can introduce a phase difference as large as 20 degrees.

The relationships here presented have been derived under the assumption that $C_1 = 0$. However in real integrated circuits the inductors introduce some parasitic capacitances that increase the value of C_1. Unlike the varactors used for C_2, these capacitances are fixed and contribute to add a cutoff frequency to the structure. Fig. 97 plots the normalized center frequency $f_{\Delta\phi,max}$ and the normalized maximum phase difference $\Delta\phi_{max}$ as a function of the parameter $\gamma = C_1/(C_1 + C_2)$ for different values of α ranging from 2 to 4. As visible, a higher parasitic capacitance results in a higher center frequency as compared with the ideal case. This effect is more evident when the capacitance ratio α is large. On the other hand, an increase of the fixed parasitic capacitances reduces the total available capacitance variation. Thus, as expected, the maximum phase shift per cell decreases with an increase of γ. Fig. 98 shows the fractional bandwidth at 1% error as a function of γ for different values of α. Unlike $f_{\Delta\phi,max}$ and $\Delta\phi_{max}$, for reasonable values of α the fractional bandwidth is quite insensitive to an increment of the parasitic capacitances.

To conclude this section, Fig. 99 shows the S-parameters of the single phase-shifter cell when all the component losses are considered ($Q_L = Q_C = 15$). Like in Sec. 7.1.2, Fig. 99(b) shows that the insertion loss is almost entirely dominated by the finite quality factor of the inductors. With reasonable components value, the presented cell achieves a phase difference of $\approx 20°$ with an insertion loss smaller than 0.8dB.

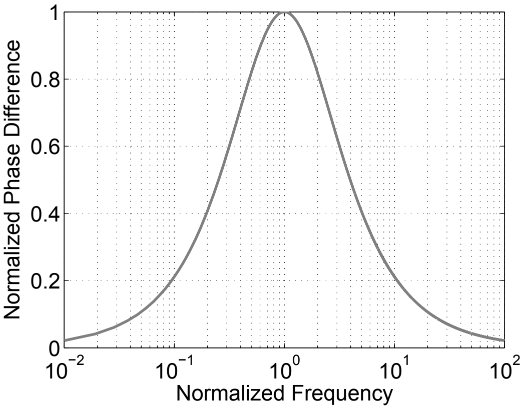
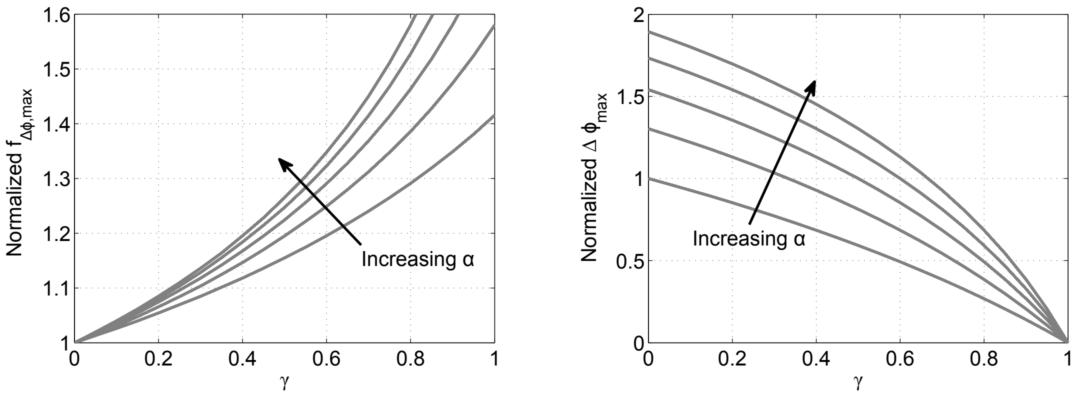


Figure 96: Normalized phase difference between two varactor configurations: $C_{2,min}$ and $C_{2,max}$. X-axis is normalized to $f_{\Delta\phi,max}$, the frequency where the phase difference is maximum.



(a)

(b)

Figure 97: Normalized center frequency $f_{\Delta\phi,max}$ (a) and normalized maximum phase difference $\Delta\phi_{max}$ (b) as a function of γ for different values of α ranging from 2 to 4. The plots are normalized to the case $\gamma = 0$ and $\alpha = 2$.

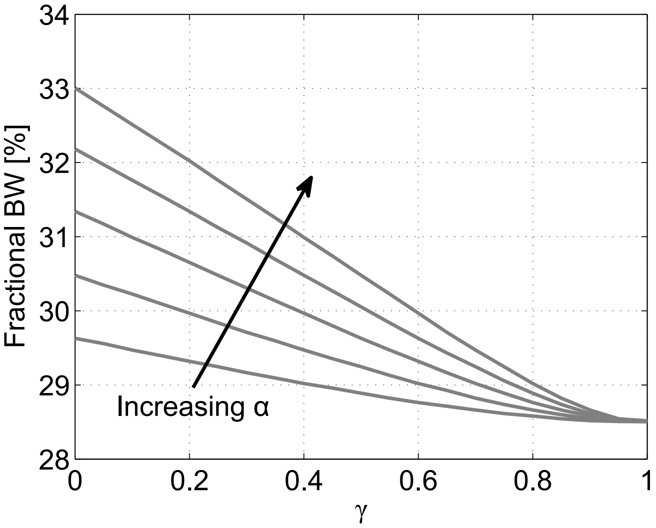
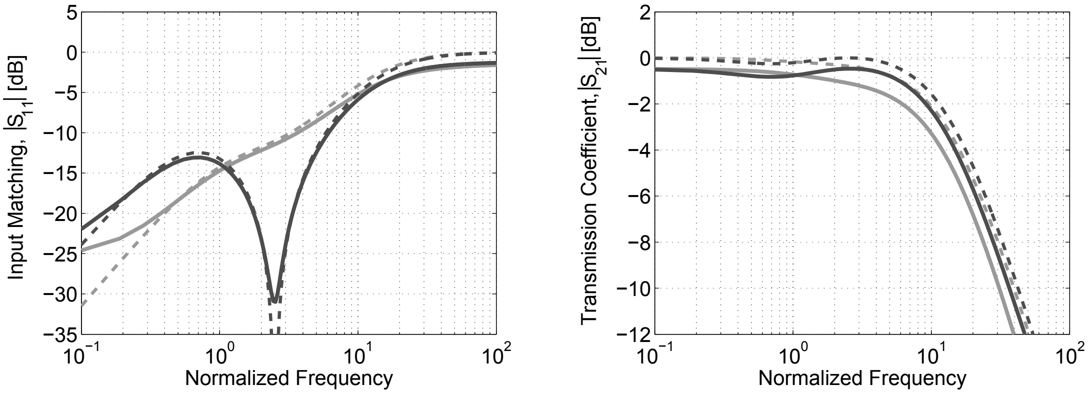


Figure 98: Fractional bandwidth at 1% phase error of a single cell as a function of γ for different values of α ranging from 2 to 4.



(a) (b)

Figure 99: Input matching ($|S_{11}|$) and transmission coefficient ($|S_{21}|$) of a single phase shifter cell when the varactor is in its minimum (light gray) and maximum (dark gray) state ($\alpha = C_{2,max}/C_{2,min} = 2.5$). Solid and dashed line correspond to a quality factor of $Q_L = Q_C = 15$ and $Q_L = Q_C = \infty$, respectively. X-axis is normalized to the center frequency $f_{\Delta\phi,max}$ of the structure.

7.1.4.1 *Effects of Varactor Parasitics*

The presented phase shifter is based on a lattice cell composed by two inductors and two cross connected capacitors. To obtain a variable phase shift, the two capacitors are replaced by two varactors. The effects of the the inductor's parasitic capacitance has already been considered in the previous section. It changes the center frequency and limits the maximum phase shift difference achieved by a single cell. Although these effects limit the system performance, they do not impair significantly the cell operation. This section explains the effects introduced by two varactor-related parasitics (i.e. the substrate capacitance and the parasitic inductor of the varactor path) and gives few guidelines to reduce their unwanted effects.

The varactor is a component that offers a variable capacitance depending on the voltage of a control signal. Many different types and configurations exist. However, this section considers two varactor types only, which are realized by a back-to-back connection of two pn junctions or two n-channel MOSFETs. In a differential nMOSFET varactor (Fig. 100(a)) the RF signal is usually applied to the gate terminals, while the control signal is applied to the drain/source terminals (the bulk terminal is grounded). Similarly, in a differential diode varactor (Fig. 100(b)), the RF signal is applied to the anode, while the control signal is applied to the cathode. As a consequence, in both of these two cases a pn junction exists between the control terminal and the substrate. This results in a voltage-dependent parasitic capacitance associated to the control line.

Let's now consider the phase shifter lattice cell of Sec. 7.1.4. Without loss of generality, consider the case where the varactor C_2 is in the minimum capacitance state ($C_2 = C_{2,min}$). The absolute phase shift introduced by a single cell at $f = f_{\Delta\phi,max}$ can be obtained from Eq. 42 and Eq. 45

$$\phi_0 = \phi|_{f=f_{\Delta\phi,max}} = \arctan\left\{\frac{1+\sqrt{\alpha}}{1-\sqrt{\alpha}}\right\}, \tag{47}$$

that is valid when $C_1 = 0$ and the source/load impedance is equal to the optimal characteristic impedance $Z_0 = Z_{0,opt}$. For example, with a value of $\alpha = 2$, the absolute phase shifting is $\approx -80^\circ$. This indicates that the signal applied across the varactors C_2 is not purely differential. For values of $C_1 \neq 0$, the absolute value of ϕ_0 changes, but the concept here described still holds.

If a non-differential signal is applied across a differential varactor, the resulting AC-voltage at the control terminal is not zero. Hence, the presence of the substrate parasitic capacitance could impair the correct operation of the circuit. In the case of a phase shifter cell, the presence of such capacitance allows the common-mode AC current to flow toward ground. As a result, the phase shift difference tends to increase with the frequency. Due to this effect, a very small and voltage-independent parasitic capacitance helps to slightly increase the operating bandwidth of the structure at the expense of a higher insertion loss. However, the varactor parasitic capacitance is a junction capacitor. Hence, its value depends on the voltage at the control terminal (i.e. depends on the phase shifting setting). This voltage-dependent parasitic capacitance results, like in the previous case, in an increasing phase shift difference with the frequency. Hence, the phase shifter becomes useless if used in a wide bandwidth. A way to reduce this effects is to minimize the varactor substrate capacitor. This may be done by changing the varactor form-factor. Unfortunately, this solution could be ineffective if the capacitance variation with the control voltage is large. To solve this issue, the varactor may be connected in the opposite way, i.e. with the drain/source terminals connected to the RF signal and the gate terminals connected to the control voltage. This leads to larger parasitic capacitances in the RF path, but, since the DC the voltage of the phase shifter cell is fixed, the voltage-dependent characteristic is removed.

In the phase shifter cell, the varactor cross-connects the two inductors. Depending on the application, the inductors may be very large. As a consequence, the varactor paths length may also be very large. Every interconnection is associated with a parasitic inductance. The longer the interconnection length, the larger the parasitic inductance. Concerning the phase shifter cell, the long connections between the inductors and the varactors result in large parasitic inductances L_{par} in series with the capacitors C_2. The effect of this inductance is manifold. First, it makes the characteristic impedance of the cell frequency dependent. Then, if its value is not too large, it reduces the effective capacitive reactance and therefore moves the center frequency $f_{\Delta\phi,max}$ towards higher values. In this case, the phase difference increases with the frequency like in the case of the varactor substrate capacitance. The worst unwanted effect, however, becomes dominant when the parasitic inductor or the capacitor C_2 become large. In this condition, the resonance frequency of the series C_2 and L_{par} may fall within the bandwidth and completely hamper the correct phase shifting operation. To minimize these effects, a reduction of the parasitic inductance in necessary. A compressed inductor layout, for example, allows to reduce the length of the varactor interconnections (Fig. 92(b) and Fig. 101(b)) without impairing significantly the quality factor of the transformer. In addition, if the interconnections are made by means of transmission lines (due to the relatively short nature, the characteristic impedance of these transmission lines is not critical), the parasitic inductance can be further reduced.

In this section, the varactor-related parasitic effects have been explored considering a phase shifter cell. A variable true time delay (Sec. 7.1.2) is based on a hybrid cell and uses varactors as C_1 and C_2. As a consequence, the same considerations here explained are also valid for the TTD case. However, this architecture is less sensitive to these effects. The first reason arise from the fact that the best group delay compensation occurs when $C_1/C_2 \approx 2$. Since C_1 is driven in a purely differential way, only the substrate capacitor of C_2 contributes to the unwanted effects. But a smaller C_2 (because of the optimum C_1/C_2) results in a smaller parasitic. To achieve a large cutoff frequency, the components value are small. A small transformer, results in a short varactor interconnection, hence a small parasitic inductance. This, together with a small C_2, increases the self resonant frequency of the C_2-L_{par} path well beyond the operating bandwidth.

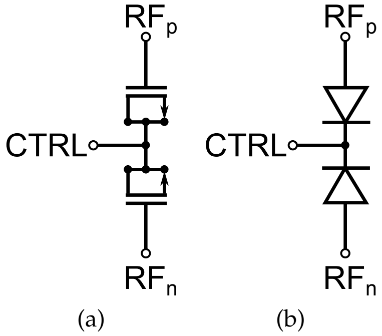


Figure 100: Usual differential connection of a MOS varactor (a) and a diode varactor (b).

7.1.4.2 *X-Band BiCMOS Implementation*

A phase shifter is used in phased array systems to change the phase of the signals in the different paths. As opposed to a true time delay, its use is limited to a narrowband implementation only. However, a wideband phase shifter is anything but useless. It may be used, for example, in systems covering more narrowband channels.

Sec. 7.1.4 presents a wideband phase shifter concept based on a lumped element lattice cell. The low area consumption together with the low insertion loss and the wideband characteristic make this implementation a good candidate for the realization of a phase shifter for a RF phased array architecture. This section presents the design of a 180°

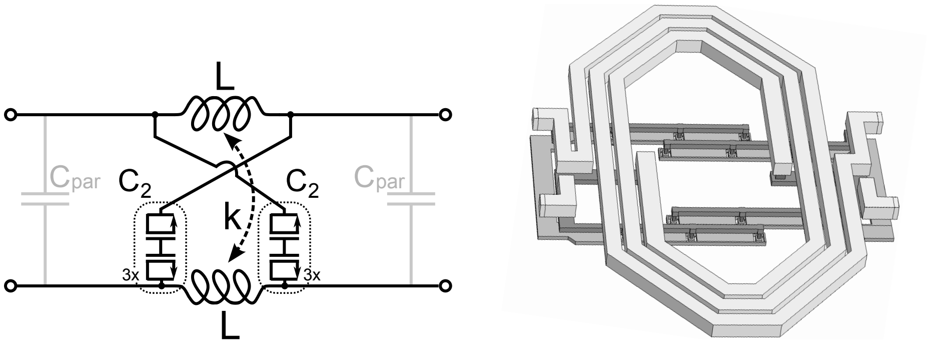
phase shifter tailored for X-band phased array radar.

The proposed phase shifter is based on the lattice cell presented in Sec. 7.1.4. The variable phase shifting feature is obtained by means of MOS varactors as C_2. The components value must be derived from the desired characteristic impedance Z_{0C} and the desired center frequency $f_{\Delta\phi,max}$. As stated in Eq. 46, in a first approximation the peak value of phase difference depends on the ratio $\alpha = C_{2,max}/C_{2,min}$ only. However, the presence of parasitic capacitances tends to decrease the effective value of α and therefore the maximum phase difference. Thus, a larger C_2 corresponds to a larger α_{eff} and a larger phase difference per cell.

The schematic of the phase shifter cell is shown in Fig. 101(a). Three parallel varactors for each capacitor C_2 ensure three different phase shifting values. Two partially overlapped inductors take advantage of the mutual inductance to achieve the desired inductance with a smaller footprint. As explained in Sec. 7.1.4.1, the substrate capacitance of the varactor, with its voltage-dependent characteristic, impairs the correct operation of the phase shifter. As visible from the cell schematic, the proposed varactors connection is unusual. A topology having the drain/source terminals connected to the RF line and the gate terminal connected to the control voltage increases the parasitic capacitance of the RF path and decreases the α_{eff} of the structure. However this solution is the key point that makes the correct operation of the phase shifter possible. As a matter of fact, this connection drastically reduces the parasitic capacitance of the control terminal and eliminates its dependence on the control voltage.

Like in the true time delay, the transformer is made of two pseudo-oval 1.5 turns inductors. The cell occupies an area of $180\text{x}260\mu m^2$. This layout allows a minimization of the varactors path length and hence a minimization of the parasitic inductance. To further reduce this parasitic, the varactor connections are made of two microstrip transmission lines.

The parameters of the proposed phase shifter cell are: single-ended inductance of $L = 680pH$ with a quality factor of $Q_L \approx 14$, a transformer coupling factor of $k = 0.6$ and a minimum varactor capacitance of $C_{2,min} = 74fF$ with a capacitance ratio of $\alpha \approx 2.7$. Taking into account the transformer and varactor parasitics, the single cell achieves a maximum variable phase shift of $\approx 20.5°$ per cell with an optimal characteristic impedance of $Z_0 = 80\Omega$. Thus, a chain of 9 cells is needed to cover the desired 180° phase shift with a resolution of $\approx 7°$.



(a) (b)

Figure 101: Proposed phase shifter cell schematic (a) and transformer layout (b). The cell dimension is $180\text{x}230\mu m^2$.

7.2 WILKINSON POWER COMBINER/DIVIDER

As detailed out in Chapter 6, a phased array architecture consists of a set of identical receiver/transmitter. Each RX/TX path can be individually programmed to adjust its relative gain and group delay. In this way, the different signals can be shifted in the time domain in order to obtain a significant change of the antenna array characteristics [32]. All the benefits introduced by a phased array architecture, however, become fruitless if at least one of its components has poor performance.

This section describes the design of an X-Band power combiner/divider based on a Wilkinson structure. This choice ensures both good matching and high isolation between the input ports. For the sake of simplicity, and unless otherwise noted, this section will consider the case of a power combiner used in a receiver chain. Notice, however, that the proposed X-Band Wilkinson can be used without any difference even in a TX chain.

7.2.1 *Impedance Transformation X-Band Wilkinson Design*

The power combiner is used to collect power from multiple sources. Usually it finds application in phased array systems both in receiver and transmitter path. The main design target is a low insertion loss, along with impedance matching at all ports. In a phased array radar, the possibility of changing the radiation pattern of the antenna results from the possibility to individually change the gain and delay of each path. Hence, a good isolation between the different path is necessary to avoid to corrupt the combined signal.

This section presents the design of a power combiner tailored for operation in the X-Band. To satisfy both input isolation and matching, it is based on a Wilkinson Power Divider. Fig. 102 shows a concept schematic of an equal-split Wilkinson power combiner/divider. It is made of two transmission line sections and a termination resistor. We will consider the case the characteristic impedance of ports 1 and 2 is equal to Z_{01}, and the characteristic impedance of port 3 is equal to Z_{03}. As a matter of fact, the two $\lambda/4$ sections perform impedance transformation, such that, to achieve the matching, one must set

$$Z_{0a} = \sqrt{2Z_{01}Z_{03}}. \tag{48}$$

Typically, $Z_{01} = Z_{03} = 50\Omega$, thus $Z_{0a} \approx 71\Omega$. However, in general, it may be useful to have the flexibility of designing the combiner for different levels of Z_0 at the different ports. This is true especially in a phased array system, where the combining stage may interface multiple phase shifters, part of different signal paths, with a common output buffer. The optimal characteristic impedance for the design of the phase shifters may be different from the best impedance environment for the amplifier. Fortunately, the Wilkinson concept has no fundamental obstacle in matching to different characteristic impedances at the various ports. In this design, all the ports are differential ones and the differential-mode characteristic impedance of the input and output ports is $Z_{01} = 60\Omega$ and $Z_{03} = 100\Omega$, respectively. Hence, $Z_{0a} \approx 110\Omega$.

In an integrated circuit, a compact area is a key element to reduce cost. At X-Band, the traditional implementation of the Wilkinson combiner using distributed transmission lines results in a large layout. As a consequence, a lumped element approach is used.

The $\lambda/4$ line section is realized as an artificial transmission line made of the cascade of two differential LC π-sections, as depicted in Fig. 103. Each π-section is equivalent to a $\lambda/8$ transmission line section, avoiding operation at the cutoff frequency of the artificial transmission line, hence widening the operation bandwidth. The inductive part is kept compact leveraging the differential arrangement used at all ports. As shown in Fig 104, two identical partially-overlapped coupled inductors take advantage of the mutual inductance to achieve the required differential-mode inductance with a smaller footprint. To avoid extra parasitics that may be introduced by connecting explicit capacitances, the required capacitance is made of the capacitive parasitics of the inductors.
The normalized ABCD matrix of the single π-section is

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1+2Z_L Y_C & 2Z_L \\ 2Y_C(1+Z_L Y_C) & 1+2Z_L Y_C \end{bmatrix}, \tag{49}$$

where $Z_L = i\omega L(1+k)/Z_0$ and $Y_C = i\omega C Z_0$ are related to the circuit parameters. Thus, the characteristic impedance of the artificial transmission line can be obtained from

$$S_{11} = \frac{A+B-C-D}{A+B+C+D} = 0 \Rightarrow Z_0 = \sqrt{\frac{L(1+k)}{C} \frac{1}{1-\omega^2(1+k)LC}}, \tag{50}$$

which suggests the use of small values for L and C in order to keep the cutoff frequency of the structure far enough from the operation frequency. This also supports the choice of using a cascade of two π-sections instead of a single one.
At the same way, the phase shift introduced by the single cell is

$$S_{21} = \frac{2}{A+B+C+D} \Rightarrow \phi = -\arctan \frac{\omega\sqrt{(1+k)LC}(2-\omega^2(1+k)LC)}{1-2\omega^2(1+k)LC}. \tag{51}$$

Finally, the solution of Eq. 51 and 50 with constraints $Z_0 = 110\Omega$ and $\phi = -\pi/4$ leads to $L \approx 440$pH, $k = 0.44$ and $C \approx 52$fF.
The termination resistor is required to provide matching for the odd-mode propagation at ports 1 and 2. Moreover, identical termination conditions for the odd and even-mode propagation result in isolation between the input ports [67]. Ideally, the termination resistor is directly connected between ports 1 and 2 (c.f. Fig. 102). However, in the proposed combiner, quite long interconnects are required between the actual port terminals and the resistor terminals, as input ports are quite spaced apart (see Fig. 104). Inductive parasitics are associated to these long interconnects, resulting in a degradation of the input matching and a decrease in isolation due to different termination conditions between the odd and even-mode propagation. To cope with this issue, small inductors have been added after the $\lambda/4$ artificial transmission line sections (see Figs. 104, 105). In the odd-mode, these inductive reactances are transformed into capacitive ones by the $\lambda/4$ impedance inverters, thus improving the matching at ports 1 and 2. In the even-mode, they are so small they negligibly degrade the matching. Overall, both matching at all ports and isolation between input ports are improved.
The proposed combiner, visible in Fig. 105, has been realized with a SiGe bipolar technology and it occupies an area of 0.12mm^2.

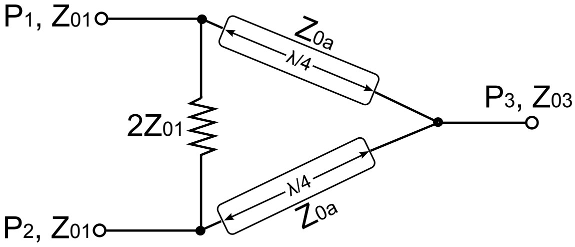

P1, Z01
P2, Z01
P3, Z03
2Z01
Z0a
λ/4
λ/4
Z0a

Figure 102: Concept schematic of equal-split Wilkinson power combiner/divider.

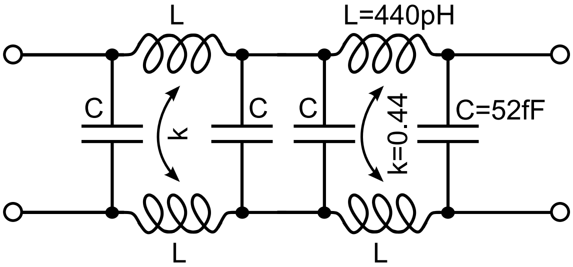

L
L=440pH
C
k
C
C
k=0.44
C=52fF
L
L

Figure 103: Schematic of the lumped-element equivalent circuit of the λ/4 differential transmission line section.

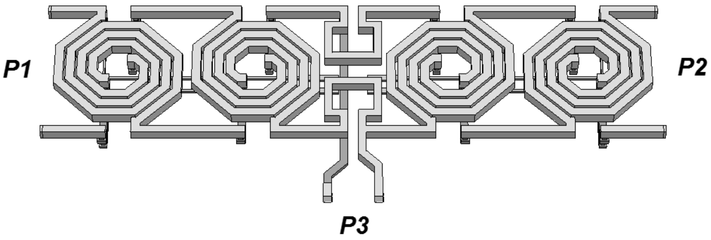


Figure 104: Layout of the proposed lumped-element Wilkinson power combiner.

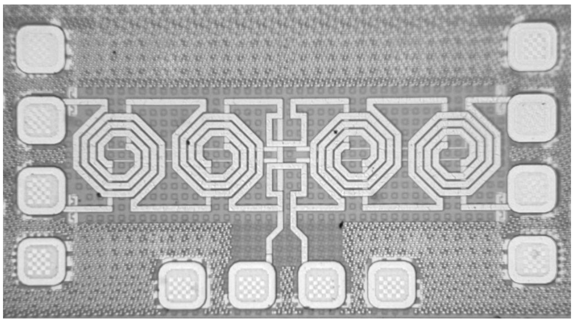


Figure 105: Chip microphotograph of the implemented lumped-element Wilkinson power combiner.

8

SIMULATION AND MEASUREMENT RESULTS

This chapter presents the simulation and measurement results of the proposed X-band structures. Unfortunately, due to the long chip fabrication time, only the measurement results of the Wilkinson power combiner are available. For the other structures (i.e. true time delay, phase shifter and true time delay extension), however, accurate simulation results will be presented.

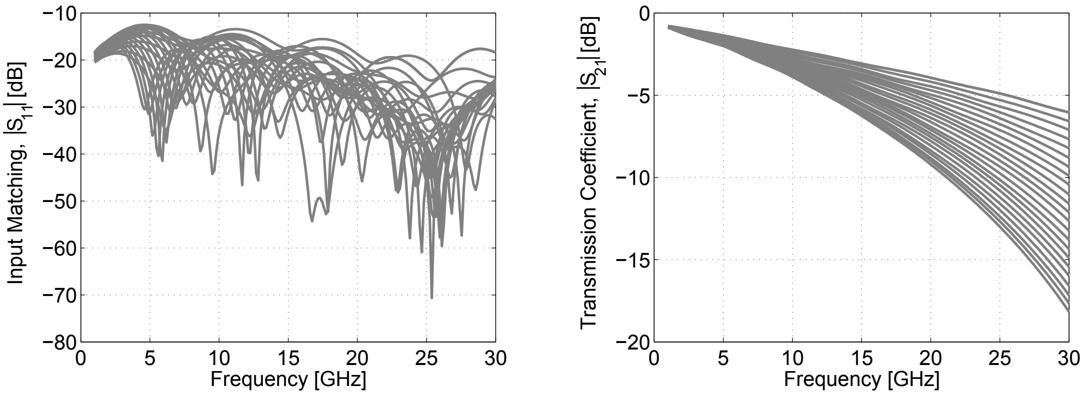
8.1 PHASE SHIFTER AND TRUE TIME DELAY

8.1.1 *X-Band BiCMOS True Time Delay*

This section presents the simulation results of the variable true time delay chain. As said in Sec. 7.1.2.1, the chain is designed for a total variable delay of $\approx 25\text{ps}$ and is realized by a cascade of 11 hybrid cells. The transformer with all the varactor interconnections has been carefully simulated by means of a 2.5D EM simulator. The variable delay characteristic is obtained by replacing every capacitor with the parallel of two varactors. This results in two different delay settings for each cell. To match the structure both in the minimum and maximum delay setting, the input and output ports have the optimal characteristic impedance of the chain $Z_0 = 75\Omega$.

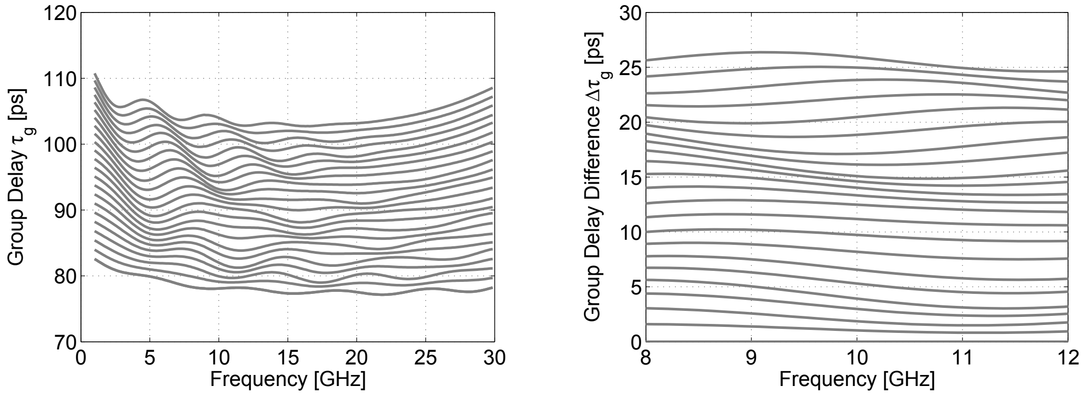
Every change of the delay corresponds to a change of the characteristic impedance of the cell. Hence, a thermometric coded bit selection is the best way to scan every delay setting. In this way, in fact, only one impedance discontinuity is present along the total chain. As a result, only one reflection occurs. Fig. 106 shows the input matching $|S_{11}|$ and the transmission coefficient $|S_{21}|$ of the chain for each delay setting over a wide frequency range from 1 to 30GHz. As visible, the chain is well matched for each delay setting and over the entire bandwidth. Around the X-band, the insertion loss (IL) is $3.35 \pm 1.4\text{dB}$.

In order to be able to process wideband signals without introducing distortion, a system must feature a constant group delay over the frequency range of interest. In a timed array radar, this requisite is mandatory to achieve the desired resolution. As a consequence, the absolute group delay introduced by the variable TTD element must feature a flat behavior for every delay settings. Fig. 107(a) shows the flatness of the absolute



(a) (b)

Figure 106: Input matching $|S_{11}|$ (a) and transmission coefficient $|S_{21}|$ (b) of the proposed 11 cells variable true time delay.



(a) (b)

Figure 107: Group delay of the proposed true time delay. Absolute group delay (a) and group delay difference in the X-band (b).

group delay of the proposed TTD as a function of the frequency for all possible delay settings. The maximum absolute group delay change is 2ps in a bandwidth from 6 to 25GHz. Hence, even if the system is designed to cover the X-band, it can be used from band C to K without an excessive deterioration of the performance. Concerning the X-band, Fig. 107(b) shows the group delay difference with respect to the case where all the varactors are in the C_{min} state. The maximum achieved delay difference is $\approx$ 25.5ps with a maximum error smaller than 1.7ps. Over the whole frequency range from 1 to 30GHz, the average group delay variation per step is 1.1ps with a standard deviation less than 0.4ps.

To assess the benefits that arise from the use of a hybrid architecture, a variable true time delay based on a simple lumped-element transmission line has been realized. To make a fair comparison, this chain is designed using the same transformer as in the hybrid solution and the total capacitance is the same. Hence they have the same characteristic impedance of 75Ω. Concerning the input matching and the insertion loss, the two results are comparable. Both chains are well matched and exhibit the same insertion loss in the X-band. However, at higher frequencies, a higher IL is observed for the lumped transmission line due to the absence of C_2 and the presence of a larger C_1. But the main difference is visible considering the delay characteristic. Fig. 108 compares the group delay difference of the two chains. Here the difference is clear: a hybrid implementation allows to enhance the bandwidth of the system.

Finally, the simulated performance of the proposed variable true time delay are compared with the state-of-the-art in Tab. 4.

Table 4: True Time Delay: Comparison with the State-of-The-Art

	[58]	[1]	[83]	This
Technology	0.25μm SiGe	90nm CMOS	0.8μm SiGe	BiCMOS
Freq. [GHz]	$20-40$	$0-8$	$3-10$	$1.8-26.5$
BW [%]	66	200	108	175
Max Group Delay [ps]	12	26	25	25.5
Delay Error [%][1]	6.4	10	40	7.8
Max. IL @ center band [dB]	11.4	3.5[2]	5[2]	5.8
Power Consumption [mW]	146	0	38.8	0
Core Area [mm^2]	0.1	–	0.23	0.12

[1] Absolute delay error in percentage of total variable delay

[2] IL @ center band stimated from given data

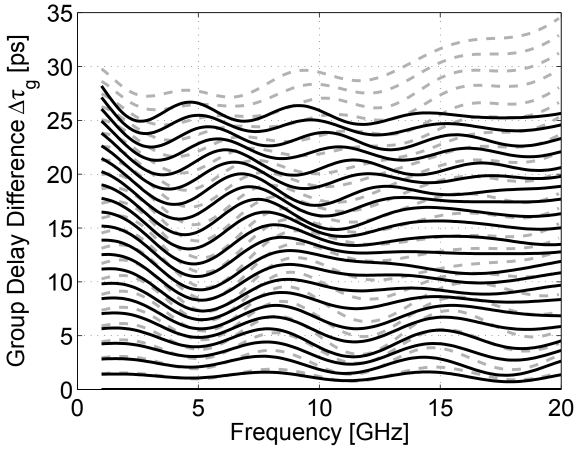


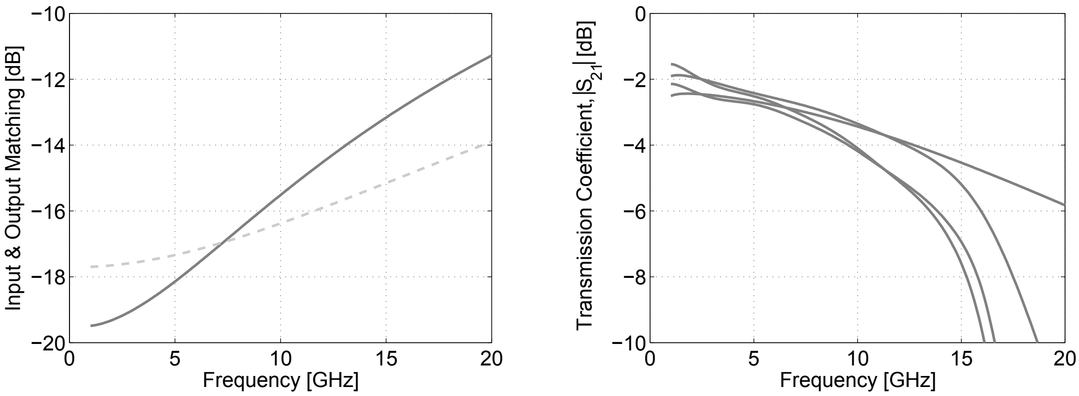
Figure 108: Comparison between the group delay difference of a true time delay based on hybrid cells (black solid line) and a TTD based on a simple lumped-element transmission line (dashed gray line)

8.1.2 *Coarse Tuning True Time Delay*

As explained in Sec. 7.1.3, the proposed solution to achieve a total variable delay of 200ps consists of a cascade of two coarse delay elements (CDE) followed by a chain of hybrid cells (FDE). The cascade of the two CDEs is designed to achieve a maximum delay of 160ps with a 40ps step. The supply voltage is 3.3V and each CDE draws a total current of 8mA. Thus, the total power consumption is $\approx 53mW$. The linearity performance of the coarse delay element is improved by the emitter degeneration resistor, hence the IIP3 is always better than $8.2\mathrm{dBm}$.

The usual timed array receiver architecture consists in a LNA followed by a cascade of a VGA and a variable TTD. If the coarse tuning delay stage is placed before the fine tuning element, the resistive matching between VGA and TTD is not necessary. For this reason, the proposed CDE exhibits a high input impedance (see schematic in Fig. 95). However, for testing purposes, two resistors have been inserted in the input stage to match the delay element with the measurement instruments. It is worth to remind that, however, these resistors will be removed in a real environment.

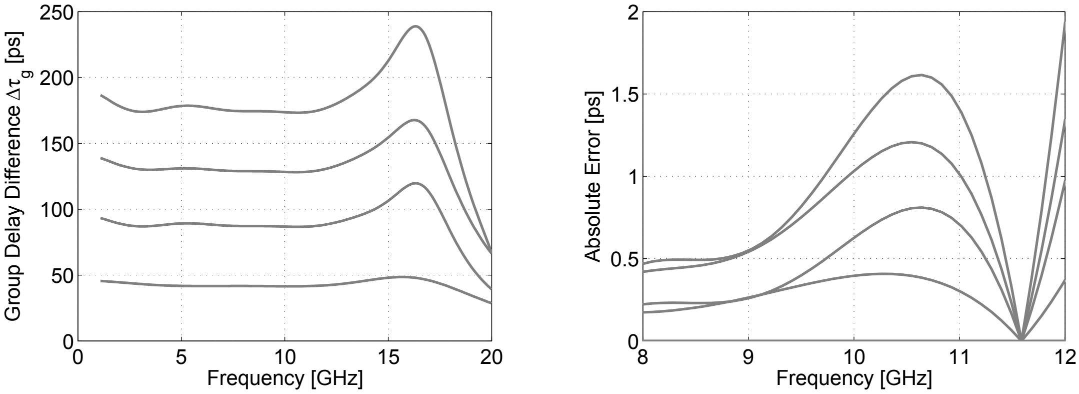
The gain and input/output matching to a characteristic impedance of 100Ω differential are plotted in Fig. 109(b) and Fig. 109(a), respectively. Around the X-band, the total gain of the cascade of two CDE is $-4 \pm 1\mathrm{dB}$ and the worst case noise figure is $\mathrm{NF}_{max} = 12\mathrm{dB}$. The delay characteristic of the two CDEs in all possible configurations is shown in Fig. 110. The maximum delay variation is $173\mathrm{ps}$ with an average delay step of $43\mathrm{ps}$. The maximum absolute delay error is less than $2\mathrm{ps}$ within the X-band. This results in a total delay variation less than 1.2% of the total delay.



(a)

(b)

Figure 109: S-Parameters of the proposed coarse tuning delay element. Input (solid line) and Output (dashed line) matching (a) and gain (b).



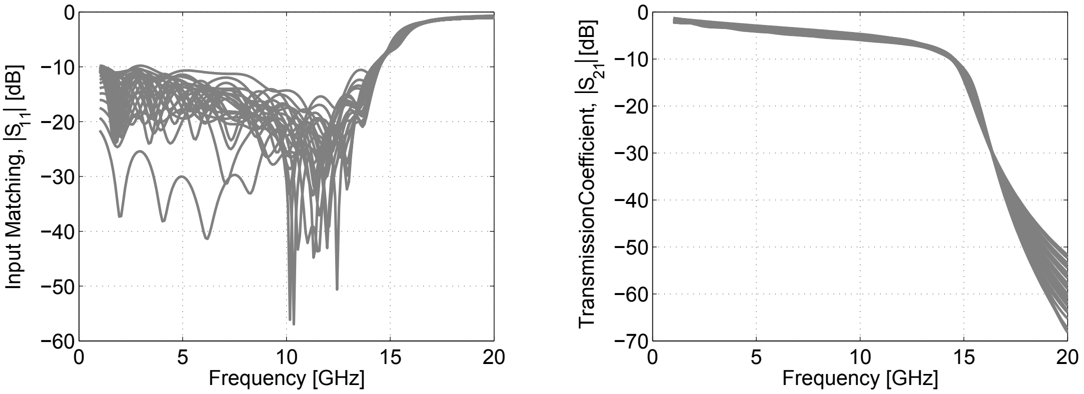
(a)

(b)

Figure 110: Delay characteristics of the proposed cascade of two multiplexers. Group delay difference (a) and delay error in the X-band (b).

8.1.3 *X-Band BiCMOS Phase Shifter*

This section presents the simulation results of the phase shifter chain presented in Sec. 7.1.4.2, which is composed by a cascade of 9 lattice cells. The single cell and the varactor connections have been simulated by means of a 2.5D EM simulator. This allows to take into account the capacitive parasitics of the transformer and the parasitic inductance of the varactor connections. Three different phase shift values for each cell are obtained by a parallel connection of three varactors. A change of the phase shift setting corresponds to a change of the characteristic impedance of the cell. Like in the true time delay, a thermometric code is used to select the desired phase shift setting. The chain is designed to achieve a total phase shift of 180° with a step of 7° and an optimal characteristic impedance of 80Ω.
Input matching $|S_{11}|$ and transmission coefficient $|S_{21}|$ are shown in Fig. 111 over a wide frequency range. In the X-band, the input matching is always better than -12dB in all phase shift states and the insertion loss is $5.3 \pm 1.5\text{dB}$.



(a) (b)

Figure 111: Input matching $|S_{11}|$ (a) and transmission coefficient $|S_{21}|$ (b) of the proposed 9 cells variable phase shifter.

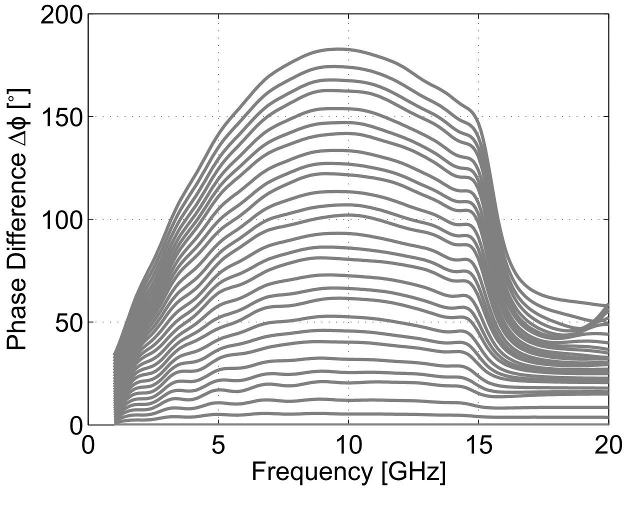


Figure 112: Phase difference of the total chain with respect to the configuration where all varactors are in the C_{max} state.

All the phase shifting states are shown in Fig. 112. From 8 to 12GHz, the maximum phase shift is 180.5 ± 2.5°. In this frequency range, the average step value is 6.6° with a standard deviation of 0.13°.

Finally, the simulated performances of the proposed phase shifter are compared with the state-of-the-art in Tab. 5.

Table 5: Phase Shifter: Comparison with the State-of-The-Art

	[34]	[5]	[48]	This
Technology	0.5μm GaAs	0.4μm GaAs	0.13μm CMOS	BiCMOS
Freq. [GHz]	C-Band	2.3 – 3.8	6 – 18	8 – 12
BW [%]	10	49	100	40
Max Phase Shift [°]	360	337.5	337.5	180.5
RMS Error [°]	2.3	3	10	2.5[2]
Max. IL [dB]	6.5	4.7	5	6.8
Power Consumption [mW]	0	0	8.7	0
Core Area [mm^2]	1.37[1]	2.6[1]	0.14	0.37

[1] Area of the complete chip including pads
[2] Absolute error

8.2 WILKINSON POWER COMBINER/DIVIDER

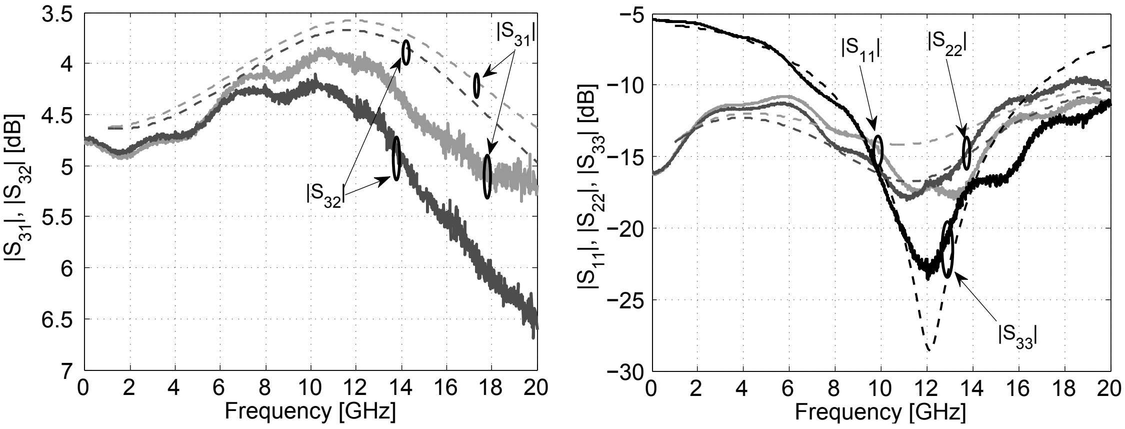
The proposed Wilkinson power combiner has been measured by means of micro probes and a 4-port Advantest R3860A vector network analyzer. A standard SOLT calibration has been performed. The S-parameters of the Wilkinson combiner have been measured in a 50Ω single-ended environment. Afterwards, the parasitic effects of the pads have been de-embedded making use of measurements performed on a pad test structure. Finally, the generalized S-parameters [67] are computed, to account for the different characteristic impedances at the various ports. The two input ports (port-1 and port-2) are designed to exhibit a differential characteristic impedance of 60Ω, while the output port must feature a differential characteristic impedance of 100Ω.

The measured and simulated transmission coefficients are reported in Fig. 113(a). We observe a quite good agreement between measurements and simulation results. Since in an ideal equal-split Wilkinson combiner the transmission coefficient (i.e. S_{31} and S_{32}) is -3dB, the measured insertion loss (IL) for the reported design ranges from 0.9 to 1.1dB in the frequency range from 8 to 12GHz. Note that the transmission from port-2 to port-3 shows a larger attenuation (up to 0.4dB larger) as compared to the transmission from port-1 to port-3. Because of the symmetry of the combiner layout, such a large mismatch is unexpected. In fact, simulations do not capture it. It can be conjectured that the mismatch is due to a different impact of the underpass required at port-3 (see Fig. 104) on the two paths, or to some artifacts in the calibration/de-embedding procedure.

Fig. 113(b) reports the measured and simulated reflection coefficients at all ports. A very good agreement between measurements and simulation results is shown. Ports 1 and 2 are matched (reflection coefficient smaller than -10dB) in the entire measurement frequency range, while port-3 is matched from 7GHz up to the higher limit of the measurement frequency range, namely 20GHz. As a result, the return loss (RL) is higher than 12dB in the whole X-band.

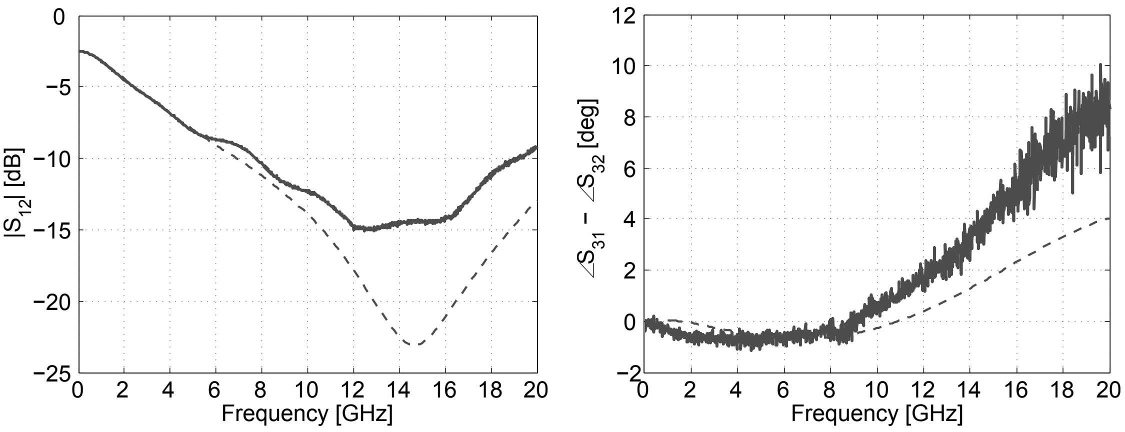
The measured and simulated isolation between ports 1 and 2 is shown in Fig. 114(a). The agreement between the measurements and the simulation is fairly good. For frequencies between 8 and 19GHz, the measured isolation is in excess of 10dB. The measured and simulated phase mismatch between the two signal paths from ports 1 and 2 to port-3 is shown in Fig. 114(b). The measured mismatch is smaller than 2° in the wide frequency range between 8 and 12GHz, such that the proposed Wilkinson combiner can effectively find application in phased arrays systems.

Finally, the measured performances of the proposed Wilkinson power combiner are compared with the state-of-the-art in Tab. 6. The performances of the proposed combiner, as well as the area consumption, are in line with the state-of-the-art, with the additional feature of supporting different characteristic impedances for the input and output ports.



(a) (b)

Figure 113: Measured (solid line) and simulated (dashed line) transmission (a) and reflection (b) coefficients.



(a) (b)

Figure 114: Measured (solid line) and simulated (dashed line) isolation (a) and phase mismatch (b) between the two input ports.

Table 6: Power Combiner: Comparison with the State-of-The-Art

	[86]	[41]	[20]	This
Technology	0.18μm CMOS	0.13μm CMOS	0.5μm GaAs	0.35μm SiGe
Freq. [GHz]	$16-27$	$22-26$	$10-24$	$8-14$
BW [%]	51	17	82	54
IL [dB]	1.0	1.4	1.4	1.4
RL [dB]	17.5	8.9	10	12
Iso. [dB]	12.2	14.8	–	10
Area [mm^2]	0.043	0.035	1.8	0.12

Part IV

CONCLUSIONS

9

CONCLUSIONS

This PhD thesis presents the design of fully-integrated high-resolution radars. The work is focused on two different, but related, topics. The first concentrates on the feasibility study together with the design of an integrated UWB radar tailored for breast cancer diagnostic imaging. The second one, instead, focuses on the design of alternative building blocks for phased array radar able to improve the total system performance while reducing the area consumption.

The first part of the PhD also focuses on the design of an IC capable of replacing the expensive laboratory instrument in a microwave imaging setup. The system specifications are obtained after a thorough system analysis. To achieve a resolution of $3mm$ inside the breast, the transceiver operates over 3 octaves, from 2 to $16GHz$. To be able to resolve the tumor backscatter, even in presence of the large skin reflection, it must feature a dynamic range in excess of $100dB$. Finally, since the imaging process is based on phase measurements, the I/Q phase error must be kept below $1.5°$ over the entire bandwidth.

The transceiver is realized in a $65nm$ CMOS technology. The chip occupies an area of $1x1.3mm^2$ and consumes $204mW$ from a $1.2V$ power supply. The receiver features a conversion gain of 36dB with an average noise figure (NF) of $7dB$, a $1dB$ compression point $\geqslant -29dBm$ and a flicker noise corner of 30Hz. The transmitter features an average output power of $-14dBm$, a minimum harmonic rejection $\geqslant 40dBc$ up to the fifth harmonic, a phase noise $\leqslant -109dBc/Hz@1MHz$ offset and an I/Q phase error lower than $1.5°$. Overall, the radar covers a bandwidth from 2 to $16GHz$ and achieves a resolution of $3mm$ inside the human body with a dynamic range of $107dB$.

Apart from the standard electrical characterization, several experiments have been carried out to assess the imaging performance of the system. The most important one consists of a real imaging experiment on a breast phantom containing two small targets. As a result, the system correctly detects the two targets and locates them in the correct position. This demonstrates that the proposed integrated radar can effectively replace the expensive laboratory instrument in a medical imaging context. To the best of my knowledge, the presented radar imager is the first full-custom integrated circuit dedicated to microwave imaging systems for medical applications, in particular for the breast cancer diagnostic imaging.

The second part of the PhD has been focused on the design of building blocks for timed array systems. A timed array system consists on a matrix of transceivers connected to an antenna array. The change of the group delay introduced by each path makes the change of the antenna pattern possible. As a result, the overall system performance is improved.

The most critical block of a timed array system is the variable true time delay (TTD). It must feature a variable and flat group delay over a wide bandwidth. To keep the implementation cost low, a compact solution is also preferred. When the system operates on a narrow bandwidth, the true time delay can be replaced with a phase shifter. Similarly, a low area consumption is one of the major constraints. To combine the signals of each path, a power combiner is needed. Here, a low insertion loss is mandatory.

A new true time delay architecture has been investigated. It is based on a cascade of lumped hybrid cells, each realized as a combination of a ladder and a lattice topology. This configuration allows to compensate the increasing group delay of the ladder cell with the decreasing group delay of the lattice implementation. As a result, the hybrid cell shows a flat group delay over a wide bandwidth. A phase shifter has also been realized. It is based on the same hybrid cell, where, however, the value of capacitors is different. In both designs, a wideband characteristic is observed with a small insertion loss and a low area consumption. A solution to increment the available delay variation is also presented. It is based on a coarse/fine tuning architecture, where the coarse delay element is based on multiplexing between transmission lines having different electrical length. This solution allows to reduce the area consumption as well as the insertion loss with respect to a solution that uses a long chain of fine delay elements (i.e. a chain of hybrid cells).

The design of the power combiner is based on a Wilkinson architecture. Hence, it features isolation between the two input ports. To keep the area consumption low, a lumped structure is adopted. As a result, the proposed Wilkinson shows a performance that is in line with the state-of-the-art, with the additional feature of supporting different characteristic impedances for the input and output ports.

To conclude, this work presents the design of state-of-the-art integrated circuits for fully-integrated high resolution radars. I hope that these efforts can effectively contribute to the design of systems able to improve the life quality and the health of people.

LIST OF PUBLICATIONS

CONFERENCE

1. Bassi, M.; Caruso, M.; Bevilacqua, A.; Neviani, A., "A $1.75 - 15GHz$ Stepped Frequency Receiver for Breast Cancer Imaging in $65nm$ CMOS", European Solid-State Circuits Conference (ESSCIRC), 2012 Proceedings of the
2. Caruso, M.; Bassi, M.; Bevilacqua, A.; Neviani, A., "A 2-to-$16GHz$ $204mW$ $3mm$-resolution stepped-frequency radar for breast cancer diagnostic imaging in $65nm$ CMOS", Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2013 IEEE
3. Caruso, M.; Bassi, M.; Bevilacqua, A.; Neviani, A., "Wideband $2 - 16GHz$ Local Oscillator Generation for Short-Range Radar Applications", ESSCIRC (ESSCIRC), 2013 Proceedings of the

JOURNAL

1. Bassi, M.; Caruso, M.; Kahn, M.S.; Bevilacqua, A.; Capobianco, A.; Neviani, A., "An Integrated Microwave Imaging Radar With Planar Antennas for Breast Cancer Detection", Microwave Theory and Techniques, IEEE Transactions on (Volume:61 , Issue: 5), May 2013
2. Bassi, M.; Caruso, M.; Bevilacqua, A.; Neviani, A., "A $65 - nm$ CMOS $1.75 - 15GHz$ Stepped Frequency Radar Receiver for Early Diagnosis of Breast Cancer", Solid-State Circuits, IEEE Journal of (Volume:48 , Issue: 7), July 2013

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