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Development and Testing of the large PMTs Front-End Electronics for the JUNO Experiment

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Abstract

One of the many challenges neutrino physics is facing is the neutrino's mass hierarchy determination. The Jiangmen Underground Neutrino Observatory (JUNO) is a new generation Liquid Scintillator (LS) detector, determined on answering this question by detecting reactor electron anti-neutrinos generated from nuclear power plants at a medium baseline, around 50 km, featuring an unprecedent energy resolution of 3% @ 1 MeV, thanks to a 20 kton of LAB LS surrounded by about 18'000 20 inches Photo Multiplier Tubes (PMT), all immersed in a water pool about 700 m underground.
The thesis introduces the physics of neutrinos flavor oscillation, as vacuum oscillations are exploited by JUNO to tackle the neutrinos mass hierarchy problem. Neutrino interactions with the JUNO detector are then explained, focusing on the *inverse beta decay* reaction for reactor anti-neutrino detection. The correlated background together with the different neutrino's sources for JUNO and its broad physics program are further described.
Afterwards, the front-end electronics to achieve JUNO's demanding requirements are investigated. An energy resolution of 0.1 photoelectron and a 16 ns window timing synchronization are just some of the necessary specifications to reach the challenging target. Hence, the concept of the Global Control Unit (GCU) has been introduced: a custom and low power hardware platform, developed by INFN-Padova/University of Padova, with intelligence on board, able to perform several different tasks such as selective readout and transmission, placed very close to the PMTs to avoid any degradation of the signals caused by long cables. The intelligence is provided by a Field Programmable Gate Array (FPGA), which is an integrated circuit, configurable after manufacturing.
After a description of the board, its FPGA configuration (commonly called *firmware*) implementation and its characterization, the GCUs functionalities have been tested on a small JUNO mock-up LS detector featuring 48 PMTs, located at the INFN National Laboratories of Legnaro and designed by the Padova JUNO group. After a brief description of the apparatus, the results obtained using the JUNO readout electronics are shown. The realization of such detector has been crucial in order to test the electronics on a real LS detector and be prepared for its final deployment in JUNO.

My involvement in the JUNO experiment started in 2018 during my Masters at the University of Padova, designing and testing a FPGA embedded trigger algorithm whose primary aim was to improve the GCU discrimination capability of low amplitude PMT pulses against the background noise. The outcome of this project has been positive, successfully implementing the core in FPGA, outperforming a simple leading-edge trigger during testing. Inspired by this work, I decided to try and be part of the JUNO collaboration by applying to the PhD program in Physics at the University of Padova.

During the first part of the PhD work I successfully characterized the GCU board, assessing the performances and the quality of the two communication links: an Ethernet link and a custom synchronous link. The synchronous link characterization required the development of a dedicated firmware, in order to retrieve the Bit Error Rate (BER) and analyze the link eye diagram. Concerning the Ethernet link, the reliability of the transmission is guaranteed by the standard, and the tests focus on the maximal throughput obtainable. Other on-board components whose design had to be validated include the external 2 gigabytes Double Data Rate (DDR) memory, where I developed a testing firmware based on the Xilinx example design for the memory interface FPGA core.
I also took care of the board reliability analysis, estimating the overall Failure In Time (FIT) of the board, using a dedicated C++ framework openly available. The front-end electronics reliability is a key aspect of the JUNO experiment, given the inaccessibility of the electronics after commissioning. With the target of electronics failure being 0.5% in 6 years, tight requirements on the GCU FIT value had to be taken into account.
The majority of my PhD work consisted in the development of the final JUNO firmware for the GCU's FPGA. I was first involved with the timing and trigger system of the GCU, developing the protocol for the synchronous link, starting from a preliminary firmware version, developed for a JUNO front-end electronics prototype architecture. In order to test the link functionalities, which mainly consist in the timing synchronization and trigger, I have also developed a back-end electronics test firmware, which will be included in the final release.
Later in the development phase, the GCU did undergo a major upgrade, mainly driven by budget constraints. This led to a complete redefinition of the synchronous link, whose protocol has to be redesigned and developed. Although being cheaper, a downside of the new synchronous transmission is being more susceptible to electromagnetic interference. To potentially solve the issue, I have developed an FPGA implementation of a Clock and Data Recovery (CDR), which benefits the link with higher immunity to electromagnetic noise.
Concerning the testing using the JUNO mock-up detector, I was responsible of the preparation of the setup, integrating the front-end with the back-end electronics. I have also been involved, together with the JUNO Padova group, in the data acquisition and analysis, whose results are presented in the final part of this work.

Sommario

Una delle grandi sfide riguardanti la fisica del neutrino riguarda l'identificazione della sua gerarchia di massa. Il Jiangmen Underground Neutrino Observatory (JUNO) è un rivelatore a scintillatore liquido di nuova generazione, determinato a trovare una risposta a questa questione ancora irrisolta rilevando anti-neutrini elettronici da reattore, generati da centrali nucleari poste ad una distanza di circa 50 km, con una risoluzione energetica senza precedenti del 3% @ 1 MeV, grazie ad una immensa massa bersaglio di 20 mila tonnellate di liquido scintillatore, attorniato da circa 18'000 tubi fotomoltiplicatori (PMT) di grandi dimensioni, il tutto immerso in una piscina d'acqua a circa 700 metri di profondità.
La tesi introduce la fisica riguardante l'oscillazione del neutrino in vuoto, fenomeno sfruttato da JUNO per studiare il problema della gerarchia di massa. Successivamente vengono introdotte le principali interazioni del neutrino con il rivelatore, incentrandosi sulla reazione di *inverse beta decay* per la rilevazione di anti-neutrini elettronici. In questa sezione vengono spiegate anche le differenti sorgenti di neutrini che l'esperimento JUNO rileverà e il segnale di fondo atteso, oltre al vasto programma di fisica del neutrino di JUNO verrà descritto.
Successivamente verrà descritta l'elettronica di front-end. Una risoluzione di 0.1 fotoelettroni e una finestra di sincronizzazione di 16 ns sono solo alcune delle caratteristiche necessarie a raggiungere i requisiti di JUNO. Da qui nasce il concetto della Global Control Unit (GCU): una scheda custom a bassa potenza, sviluppata da Università e INFN di Padova, capace di svolgere differenti funzioni, dalla trasmissione di dati alla loro analisi, grazie all'intelligenza garantita da un Field Programmable Gate Array (FPGA), un circuito integrato configurabile dopo produzione, presente su scheda. La GCU verrà inoltre posizionata molto vicina ai PMT, sott'acqua, per evitare qualsiasi possibile degradazione del segnale causato da una grande lunghezza dei cavi.
Dopo la descrizione della scheda, la configurazione della sua FPGA (chiamato comunemente *firmware*) e la sua caratterizzazione, le funzionalità della GCU vengono testate su di un piccolo rivelatore a scintillatore liquido a modello JUNO, con installati 48 PMT. Il rivelatore si trova ai Laboratori Nazionali di Lgnaro (INFN-LNL) ed è stato progettato da Università/INFN Padova. Dopo una breve descrizione dell'apparato, vengono mostrati i risultati ottenuti utilizzando l'elettronica di readout di JUNO. La realizzazione di questo rivelatore è stata cruciale, in quanto ha permesso di testare l'elettronica di JUNO su di un vero setup multicanale, acquisendo esperienza chiave per la successiva installazione sul rivelatore finale.

Il mio lavoro con l'esperimento JUNO è iniziato nel 2018 con il lavoro di tesi magistrale svolto all'Università di Padova. Questo è consistito nell'implementazione in FPGA di un algoritmo di trigger,

la cui funzione principale consisteva nel migliorare la capacità di discriminazione di segnali a bassa ampiezza rispetto al rumore di fondo causato dall'elettronica. I risultati del progetto sono stati positivi, implementando con successo l'algoritmo in FPGA, superando in performance un semplice algoritmo di trigger a soglia nei test. Stimolato dagli esiti positivi di questo progetto, decisi di provare a far parte della collaborazione JUNO, con un percorso di dottorato in Fisica presso l'Università degli Studi di Padova.
Nella prima parte del mio percorso di dottorato ho caratterizzato l'hardware della GCU, valutando le performance e la qualità di trasmissione dati dei due link di comunicazione presenti: un link Ethernet e un link sincrono custom. La caratterizzazione del link sincrono ha richiesto lo sviluppo di un firmware dedicato per la determinazione del Bit Error Rate (BER) e l'analisi del suo diagramma ad occhio. Per quanto riguarda il link Ethernet, l'affidabilità della trasmissione è garantita dallo standard, e i test si concentrano sul massimo throughput ottenibile. Altri componenti il cui design è stato necessario validare, includono la memoria esterna Double Data Rate (DDR), dove il firmware di test viene basato su un design di esempio della Xilinx per il suo "memory interface FPGA core". La caratterizzazione della scheda include inoltre la sua analisi di affdabilità, dove ho stimato il valore globale del Failure In Time (FIT) della scheda, utilizzando un framework C++ disponibile pubblicamente online. L'affidabilità dell'elettronica di front-end è un aspetto chiave in JUNO: data l'inaccessibilità dell'elettronica dopo la fase di commissioning, la percentuale massima stabilita di guasti riguardanti l'elettronica è di 0.5% in 6 anni di presa dati.
La maggior parte del mio lavoro di dottorato consiste nello sviluppo del firmware finale di JUNO per l'elettronica di front-end. Inizialmente sono stato coinvolto con il sistema di timing e trigger della GCU, sviluppando il protocollo del link sincrono, partendo da una versione preliminare del firmware, sviluppata per una versione obsoleta dell'elettronica di readout. Per testare le sue funzionalità, le quali consistono principalmente nella sincronizzazione temporale e nella distribuzione del trigger, ho sviluppato un firmware di test per l'elettronica di back-end, che sarà poi incluso nella versione finale. Durante il mio percorso di dottorato, la GCU ha subito un aggiornamento hardware importante, causato principalmente da limiti in termini di budget. Questo portò ad una completa ridefinizione del link sincrono, il cui protocollo aveva bisogno di essere ridisegnato e sviluppato. Il risultato fu un link meno costoso dal punto di vista dei componenti utilizzati, ma più soggetto a rumore elettromagnetico. Per risolvere questo problema, ho sviluppato un core da implementare in FPGA, con le funzioni di Clock and Data Recovery (CDR).
Nella parte finale del mio lavoro di tesi ho avuto la responsibilità della preparazione del setup per il rivelatore simil-JUNO con 48 PMT presso i Laboratori Nazionali di Legnaro. Ho inoltre contribuito, assieme al gruppo JUNO di Padova, all'acquisizione dati e alla loro analisi, i cui risultati sono presentati nella parte finale di questa tesi.

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Part I

Neutrinos and JUNO

1

Introduction to Neutrino Physics

Neutrinos are fundamental particles and, like quarks and photons, can not be broken down into smaller pieces. These fermions have no electric charge, are extremely light and extremely common; as a matter of fact they are the most abundant massive particle in the universe as they originate from different sources and trillions of these particles travel through a human body every second of the day. Three different *flavors* identify the neutrinos (anti-neutrinos, the neutrinos antiparticles) with their charged *leptons* counterparts: ν_e ($\overline{\nu}_e$), ν_τ ($\overline{\nu}_\tau$) and ν_μ ($\overline{\nu}_\mu$). The only ways these particles interact are through Charged Current (CC) and Neutral Current (NC) of the weak force due to their lack of *electrical charge* and *color change*; this makes the neutrinos an *elusive* particle, difficult to detect and to catch. The weak force interaction allows neutrino to pass through the atoms of massive objects, avoiding any interaction. In order to have a chance to detect them, huge detectors need to be built and intense sources of this particle need to be exploited.

The particle has been firstly thought of and proposed in 1930 by Wolfgang Pauli [1], as a possible resolution for the continuous energy spectra and missing spin in β-decay experiments. The particle was first detected in 1956 by Cowan and Reines [2], where nuclear reactor electron anti-neutrinos interact with protons in two tanks of water via the Inverse Beta Decay (IBD) reaction:

$$\overline{\nu}_e + p \rightarrow n + e^+ \tag{1.1}$$

But it was only in 1962 and 1975 that the muon neutrino [3] and tau neutrino [4, 5] were discovered, respectively. The discovery of this new particle, with the respective flavors, led to numerous other experiments in order to detect neutrinos and investigate their properties.

1.1 Neutrino Oscillations in Vacuum

The concept of flavor oscillation between neutrinos resides in the fact that neutrinos produced with a certain flavor, ν_e, ν_τ or ν_μ may be detected at later times with a different flavor. The consequence is not only that, contrary to the Standard Model (SM) [6], neutrinos are massive particles, but that these masses, which we'll call ν_1, ν_2 and ν_3, are not defined for a specific flavor state, but they are quantum superimposition of them.

The first experimental observation of this phenomenon dates back in 1960s, when the *Homestake experiment* [7] made the first measurement of the electron neutrino flux generated in the sun's core. The results were inconsistent with the standard solar model, with a flux between one third and one half of the expected value [8]. The hypothesis of a neutrino mass slightly different than zero which would introduce the possibility of flavor oscillation has been later investigated in a new series of experiments [9], in particolar the Sudbury Neutrino Observatory (SNO) which, in the 2000s, could detect all of the neutrino flavors and found no deficit in the measurements [10].

The flavor eigenstates can be obtained from the mass eigenstates with a transformation, which is assumed to be unitary:

$$\begin{pmatrix} \nu_e \\ \nu_\mu \\ \nu_\tau \end{pmatrix} = \begin{pmatrix} U_{e1} & U_{e2} & U_{e3} \\ U_{\mu 1} & U_{\mu 2} & U_{\mu 3} \\ U_{\tau 1} & U_{\tau 2} & U_{\tau 3} \end{pmatrix} \begin{pmatrix} \nu_1 \\ \nu_2 \\ \nu_3 \end{pmatrix} \tag{1.2}$$

The transformation can be expressed in terms of three rotations, with angles that we will call θ_{12}, θ_{23}, θ_{23} and *phase factors*. A distinguish shall be made whether neutrinos are *Dirac* particles (neutrino and antineutrino are two different particles) or *Majorana* particles (neutrino and antineutrino are the same particle). In the latter case, two more phases, the Majorana phases, ϕ_1 and ϕ_2, are physically observable, even though they are irrelevant for the flavor oscillation effect. Defining $c_{ij} = cos\theta_{ij}$ and $s_{ij} = sin\theta_{ij}$, the transformation matrix becomes [11]:

$$U = \begin{pmatrix} 1 & 0 & 0 \\ 0 & c_{23} & s_{23} \\ 0 & -s23 & c_{23} \end{pmatrix} \begin{pmatrix} c_{13} & 0 & s_{13}e^{-i\delta} \\ 0 & 1 & 0 \\ -s_{13}e^{i\delta} & 0 & c_{13} \end{pmatrix} \begin{pmatrix} c_{12} & -s_{12} & 0 \\ s_{12} & c_{12} & 0 \\ 0 & 0 & 1 \end{pmatrix} \begin{pmatrix} 1 & 0 & 0 \\ 0 & e^{i\phi_1} & 0 \\ 0 & 0 & e^{i\phi_2} \end{pmatrix} \tag{1.3}$$

Using the same notation, a neutrino with flavor α is described by the state:

$$|\nu_\alpha\rangle = \sum_k U^*_{\alpha k} |\nu_k\rangle \qquad (\alpha = e, \mu, \tau; k = 1, 2, 3) \tag{1.4}$$

Since the massive neutrino state $|\nu_k\rangle$ are eigenstates of the Hamiltonian, the Schrödinger equation

gives the time evolution of such states as a plain wave:

$$|\nu_k(t)\rangle = e^{-iE_k t}\,|\nu_k\rangle \tag{1.5}$$

which translates for the flavor states as

$$|\nu_\alpha(t)\rangle = \sum_k U^*_{\alpha k} e^{-iE_k t}\,|\nu_k\rangle \tag{1.6}$$

such that

$$|\nu_\alpha(t=0)\rangle = |\nu_\alpha\rangle \tag{1.7}$$

Applying the unitary properties of the transformation matrix to invert Eq. 1.4, we obtain:

$$|\nu_\alpha(t)\rangle = \sum_{\beta=e,\mu,\tau} \Big(\sum_k U^*_{\alpha k} e^{-iE_k t} U_{\beta k}\Big) \big|\nu_\beta\big\rangle \tag{1.8}$$

Hence, the superimposition of massive neutrino states $|\nu_\alpha(t)\rangle$ (Eq. 1.4) becomes a superimposition of different flavor states at $t > 0$. The amplitude of flavor transition as function of time is given by the coefficient of $\big|\nu_\beta\big\rangle$:

$$A_{\nu_\alpha\to\nu_\beta}(t) \equiv \big\langle \nu_\beta \big| \nu_\alpha(t)\big\rangle = \sum_k U^*_{\alpha k} U_{\beta k} e^{-iE_k t} \tag{1.9}$$

which gives the transition probability by

$$P_{\nu_\alpha\to\nu_\beta}(t) = |A_{\nu_\alpha\to\nu_\beta}(t)|^2 = \sum_{k,j} U^*_{\alpha k} U_{\beta k} U_{\alpha j} U^*_{\beta j} e^{-i(E_k - E_j)t} \tag{1.10}$$

Since for ultra-relativistic neutrinos we can approximate

$$E_k \simeq E + \frac{m_k^2}{2E} \tag{1.11}$$

then

$$E_k - E_j \simeq \frac{\Delta m^2_{kj}}{2E} \tag{1.12}$$

where Δm^2_{kj} is the squared-mass difference

$$\Delta m^2_{kj} \equiv m_k^2 - m_j^2 \tag{1.13}$$

For practical reason, it is more convenient to express the transition probability as a function of distance L between the source and the detector, instead of the propagation time t. Since neutrinos are ultra-relativistic particles, $L \approx t$:

$$P_{\nu_\alpha\to\nu_\beta}(L,E) = \sum_{k,j} U^*_{\alpha k} U_{\beta k} U_{\alpha j} U^*_{\beta j} exp\left(-i\frac{\Delta m^2_{kj} L}{2E}\right) \tag{1.14}$$

Eventually, the oscillation probability can be written in the following form, with "+" sign for neutrinos and "—" sign for anti-neutrinos:

$$P_{\nu_\alpha \to \nu_\beta}(L,E) = \delta_{\alpha\beta} - 2\sum_{k>j} Re[U^*_{\alpha k}U_{\beta k}U_{\alpha j}U^*_{\beta j}]sin^2\left(\frac{\Delta m^2_{kj}L}{4E}\right) \pm 2\sum_{k>j} Im[U^*_{\alpha k}U_{\beta k}U_{\alpha j}U^*_{\beta j}]sin\left(\frac{\Delta m^2_{kj}L}{4E}\right) \tag{1.15}$$

with *Re* and *Im* describing the *real* and *imaginary* part of the matrix products, respectively.

The oscillation probabilities of the channels $\alpha \neq \beta$ are usually called *transition probabilities*, whereas the oscillation probabilities of the channels with $\alpha = \beta$ are called *survival probabilities*; the latter has the following form:

$$P_{\nu_\alpha \to \nu_\alpha}(L,E) = 1 - 4\sum_{k>j} |U_{\alpha k}|^2 |U_{\alpha j}|^2 sin^2\left(\frac{\Delta m^2_{kj}L}{4E}\right) \tag{1.16}$$

1.2 Neutrino Oscillation Parameters and Experiments

Concerning neutrino oscillations, there are three oscillation frequencies, corresponding to three squared-mass differences. The oscillation probability between a given pair of flavors is a sum of oscillating terms at these frequencies with maximum excursions that are functions of the three mixing angles.

In practice, the problem can be simplified due to two circumstances:

- Two squared-mass difference are practically equal: $m^2_3 - m^2_2 \approx m^2_3 - m^2_1$. Therefore only two oscillation periods are observed.
- The two oscillation periods are substantially different. Consequently, experiments sensitive to the oscillation with shorter period do not see the longer period oscillation and, on the other hand, experiments sensitive to the longer period tends to average the signal on times that are much larger than the shorter period, losing any information.

The parameters θ_{12} and Δm^2_{21} refer to the longer oscillations period and were first measured with neutrinos from the sun, therefore the name *solar parameters*. Electron neutrinos are in fact produced from the fission processes in the sun's core, and they can oscillate to the other two flavors on their way to earth. First measurements of the solar parameters were made by SNO [10] and Super-Kamiokande (SK) [12], with further contribution from Kamioka Liquid scintillator AntiNeutrino Detector (KamLAND) [13] which, instead of using solar neutrinos, performed a disappearance experiment using electron anti-neutrinos produced by Japanese nuclear power plants.

The parameters θ_{23} and Δm^2_{23} are instead called *atmospheric*, as they were discovered with muon and electron neutrinos originated as decay products of the hadrons produced by the cosmic ray collisions with atomic nuclei in the atmosphere. The specific phenomenon has first been discovered

by SK [14] through the muon neutrino disappearance, where muon neutrinos appear in part as electron neutrinos and in part as tau neutrinos. The ν_μ disappearance has been confirmed by two other experiments: Monopole, Astrophysics and Cosmic Ray Observatory (MACRO) [15] at Gran Sasso and Soudan 2 [16] in the United States of America (USA) Other confirmations came from two long-baseline accelerator neutrino beams experiments:

- KEK to Kamioka (K2K) [17], with the neutrino source being the proton synchrotron of the KEK laboratory in Japan and SK [12] used as the far detector.
- the second experiment used the Neutrinos at the Main Injector (NuMI) beam [18] at the proton accelerator at Fermilab as neutrino source and Main Injector Neutrino Oscillation Search (MINOS) [19] as the far detector.

The third mixing angle θ_{13} has been determined with nuclear reactor anti-neutrinos and liquid scintillator detectors [20]. The measurement of the electron anti-neutrino disappearance was done over baselines between 1 km and 3 km. The main contributions came from Daya Bay [21], Double Chooz [22] and Reactor Experiment for Neutrino Oscillation (RENO) [23].

It is important to note that neutrino oscillation observations only allow measurements of the squared-mass difference, but they do not allow direct determination of the neutrino mass. This introduces one of the still open question about neutrinos: the Mass Hierarchy (MH). By defining ν_1 as the mass state with the largest admixture of electronic flavor, Δm^2_{21} is positive. Concerning the atmospheric Δm^2_{32} only the absolute value is known, therefore introducing the question of whether ν_3 is the heaviest of the three mass states, which is called Normal Hierarchy (NH) or the lightest, the Inverted Hierarchy (IH). A visualization of the MH question is shown in Fig. 1.1. Several experiments are being developed in order to solve the MH problem:

- the Jiangmen Underground Neutrino Observatory (JUNO) [24] will be the only experiment that will probe the MH problem through vacuum oscillations, instead of matter effects.
- Oscillation Research with Cosmics in the Abyss (ORCA) [25] and Precision Icecube Next Generation Upgrade (PINGU) [26] as deep-sea neutrino telescopes
- the Deep Underground Neutrino Experiment (DUNE) [27] and Hyper-Kamiokande (HK) [28], long baseline experiments with accelerator neutrino beams.

Current results from long baseline accelerator neutrino experiments like Tokai to Kamioka (T2K) [29] and NuMI Off-axis ν_e Appearance (NOνA) [30] hint towards a NH, but are not decisive.

The current best fit values for the oscillation parameters are presented in Tab. 1.1.

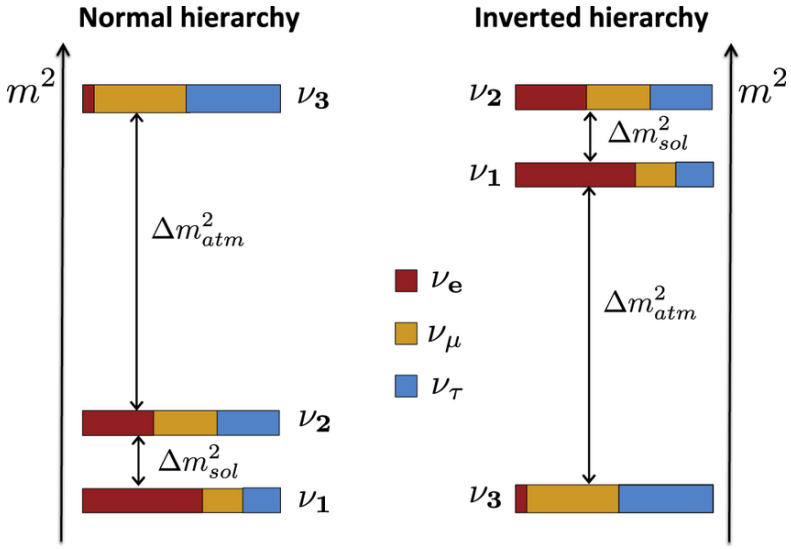

Figure 1.1: Visualization of the normal and inverted neutrino mass hierarchy. The flavor fraction for each mass state is color coded.

	Normal Hierarchy	Inverted Hierarchy
$\sin^2(\theta_{12})$	$0.307^{+0.013}_{-0.012}$	$0.307^{+0.013}_{-0.012}$
$\sin^2(\theta_{23})$	$0.545^{+0.021}_{-0.021}$	$0.547^{+0.021}_{-0.021}$
$\sin^2(\theta_{13})$	$2.18^{+0.07}_{-0.07}$	$2.18^{+0.07}_{-0.07}$
Δm^2_{21}	$7.53^{+0.18}_{-0.18} \cdot 10^{-5}\text{eV}^2$	$7.53^{+0.18}_{-0.18} \cdot 10^{-5}\text{eV}^2$
Δm^2_{3l}	$+2.453^{+0.034}_{-0.034} \cdot 10^{-3}\text{eV}^2$	$-2.546^{+0.034}_{-0.040} \cdot 10^{-3}\text{eV}^2$

Table 1.1: Latest oscillation parameters values taken from [31]. Note that $\Delta m^2_{3l} \equiv \Delta m^2_{31} > 0$ for NH and $\Delta m^2_{3l} \equiv \Delta m^2_{32} < 0$ for IH.

2

Neutrino Physics with JUNO

JUNO [24] is a multi-purpose neutrino experiment. It has been designed to give an answer to the mass hierarchy question by detecting reactor electron antineutrinos generated from nuclear power plants at a medium and equal baseline: around 50 km. JUNO will feature an unprecedent energy resolution of 3% at 1 MeV, thanks to a 20 kton Liquid Scintillator (LS) detector surrounded by 17'612 20-inches PhotoMultiplier Tube (PMT), as well as 25'600 3-inches PMTs, all immersed in a water pool about 700 meters underground (1'800 meter water equivalent (mwe)).

2.1 Neutrino Interactions

Electron reactor antineutrino will interact with JUNO LS through the IBD reaction:

$$\overline{\nu}_e + p \rightarrow e^+ + n \tag{2.1}$$

The reaction allows the detection of neutrinos thanks to the prompt positron-electron annihilation signal and the delayed neutron capture signal, which together constitutes the signature of the IBD event. The prompt positron signal generates two gamma rays of 511 keV, while the neutron capture signal is delayed on average by $\sim$216 μs, releasing a gamma ray of 2.2 MeV. Since natural radioactivity can emulate the delayed neutron capture signal, a triple-coincidence criteria in energy, time and space has to be applied to suppress the accidental background.

The neutrino energy can be inferred from the positron energy by the relation:

$$E_\nu = E_e + T_n + m_n - m_p \simeq E_e + 1.293MeV \tag{2.2}$$

where T_n is the negligibly small recoil kinteic energy of the neutron. The energy threshold of the neutrino can be calculated by taking into account that the squared center-of-mass energy $s = 2E_\nu m_p + m_p^2$ (neglecting the neutrino mass) must be bigger than $(m_n + m_e)^2$, leading to an energy threshold of

$$E_\nu^{th} = \frac{(m_n + m_e)^2 - m_p^2}{2m_p} \simeq 1.806MeV \tag{2.3}$$

The cross section can be expressed as:

$$\sigma_{IBD}(E_\nu) = 9.61 \times 10^{-44} \times (E_\nu - 1.29MeV) \times \sqrt{(E_\nu - 1.29MeV)^2 - 0.26MeV^2} cm^2 MeV^{-2} \tag{2.4}$$

Other neutrino reactions relevant in LS detectors are:

- **Neutrino-electron scattering**: a NC interaction concerning neutrino from all flavors:

$$\nu_l + e^- \rightarrow \nu_l + e^-; \;\; \overline{\nu}_l + e^- \rightarrow \overline{\nu}_l + e^- \qquad\qquad l = e, \mu, \tau \tag{2.5}$$

  Since the final state is the same as the initial state, the only effect is the redistribution of the total energy and momentum between the two particles, without any energy threshold value. Although this reaction is possible to be observed in LS detectors, it is mostly used to detect neutrinos in water Cherenkov solar neutrinos detectors.

- **Neutrino-nucleon scattering**: similar to the neutrino-electron scattering, neutrinos of all flavor can undergo CC interactions with nucleons:

$$\nu_l + n \rightarrow p + l^-; \;\; \overline{\nu}_l + p \rightarrow n + l^+ \qquad\qquad l = e, \mu, \tau \tag{2.6}$$

  Such reaction is used to detect reactor electron antineutrinos, and has been used for example in Chooz [32] and KamLAND [13].

2.2 Neutrino Sources

Being a multi-purpose neutrino experiment with a large target mass, JUNO will detect neutrinos from a variety of sources, both natural and man-made [33].

2.2.1 Natural Neutrino Sources

Some natural sources of neutrinos include:

- **SuperNova (SN) burst neutrinos**: the detection of neutrino burst from a nearby SN is a key aspect in JUNO concerning multi-messenger astrophysics research. Considering a fiducial target

Channel	Type	Events for different $< E_\nu >$ values		
		12 MeV	14 MeV	16 MeV
$\overline{\nu}_e + p \rightarrow e^+ + n$	CC	4.3×10^3	5.0×10^3	5.7×10^3
$\nu + p \rightarrow \nu + p$	NC	6.0×10^2	1.2×10^3	2.0×10^3
$\nu + e \rightarrow \nu + e$	NC	3.6×10^2	3.6×10^2	3.6×10^2
$\nu + {}^{12}\mathrm{C} \rightarrow \nu + {}^{12}\mathrm{C}^*$	NC	1.7×10^2	3.2×10^2	5.2×10^2
$\nu_e + {}^{12}\mathrm{C} \rightarrow e^- + {}^{12}\mathrm{N}$	CC	4.7×10^1	9.4×10^1	1.6×10^2
$\overline{\nu}_e + {}^{12}\mathrm{C} \rightarrow e^+ + {}^{12}\mathrm{B}$	CC	6.0×10^1	1.1×10^2	1.6×10^2

Table 2.1: Numbers of neutrino events in JUNO for a SN at a galactic distance of 10 kpc [34]. The channel type are either CC or NC.

volume of 20 kton and a typical galactic SN at 10 kpc, the total numbers of expected neutrino events in JUNO are summarized in Tab. 2.1.

- **Solar neutrinos** [35]: The Sun is a powerful source of electron neutrinos with energy of the order of 1 MeV, produced in the thermonuclear fusion reactions in the core. The main source of power in the Sun is given by tw groups of thermonuclear reactions, known as the *proton-proton (pp)* chain and the Carbon-Nitrogen-Oxygen (CNO) cycle [36]. Both result in the conversion of four protons and two electrons into a ^{4}He nucleus plus two electron neutrinos:

$$4p + 2e^- \rightarrow {}^4\mathrm{He} + 2\nu_e + Q \tag{2.7}$$

where Q represents the energy release given by the difference of the masses:

$$Q = 4m_p + 2m_e - m_{^4\mathrm{He}} = 26.7\mathrm{MeV} \tag{2.8}$$

Nowadays the studies concerning solar neutrinos are no more to prove that neutrinos are massive and oscillating particles, as other experiments have obtained compelling evidence that this is true [37, 38], but they are needed to improve the knowledge of fundamental solar physics, such as the mechanism ruling the dynamics of the Sun, the solar metallicity problem [39] and the agreement between solar models and the data from helioseismology [40, 41].

- **Atmosperic neutrinos**: Atmosperic neutrinos are generated by the interactions of primary cosmic rays, mainly composed of protons with a small percentage of heavy nuclei, with the nuclei in the atmosphere. This primary interactions generate a shower of hadrons and correlated decay products, which are called secondary cosmic rays. These decay products include neutrinos,

both muon neutrinos end electron neutrinos, through the processes

$$\pi^+ \to \mu^+ + \nu_\mu, \qquad \pi^- \to \mu^- + \overline{\nu}_\mu \tag{2.9}$$

$$\mu^+ \to e^+ + \nu_e + \overline{\nu}_\mu, \qquad \mu^- \to e^- + \overline{\nu}_e + \nu_\mu \tag{2.10}$$

The JUNO detector has a very low energy threshold compared to other atmospheric neutrinos experiments such as PINGU, ORCA and HK, and can measure atmospheric neutrinos with excellent energy resolution [42]. Thanks to its feature, JUNO is a promising detector to solve open neutrinos questions where the answer can lie in atmospheric neutrino observations, as well as improving the measurements of atmospheric oscillation parameters, such as the atmospheric mixing angle θ_{23}.

- **Geoneutrinos**: Another natural source of neutrinos is the Earth itself: electrical neutrinos are generated by radioactive beta-decay events inside the Earth, escaping the planet as matter is virtually transparent to them [43, 44].

2.2.2 Man-Made Neutrino Sources

Man-made sources of neutrinos are nuclear reactors, in which electron antineutrinos are produced in the β-decay of neutron-rich nuclei, and particle accelerators, which allow for a dedicated neutrino beam targeting a detector with a chosen baseline. As JUNO will detect reactor neutrinos, this section is not going to give further details about accelerator neutrinos.

The power generated by a reactor is mainly due to the fission of four isotopes: ^{235}U, ^{238}U, ^{239}Pu and ^{241}Pu. Each fission provides about 200 MeV of energy, together with the releasing of six $\overline{\nu}_e$'s ending up with an antineutrino yield of $2 \cdot 10^{20} s^{-1}$ for each GW$_{th}$ of thermal power.

An advantage of man-made neutrino sources in comparison to natural sources, is that the origin point of the detected neutrinos is well-known, within a few meters of uncertainty given by the fact that reactors have several cores, which is negligible comparing it to the oscillation length. This allows for full energy-dependent phase measurements of those neutrinos, a crucial point in JUNO.

Nevertheless, unlike the accelerator neutrinos, nuclear reactors emits antineutrinos isotropically, and the flux decreases rapidly with the distance. This poses a first challenge for reactor neutrino experiments, partially compensated by the relatively low energy of the neutrinos, in the order of few MeV, which implies a relatively short oscillation length. Nevertheless, a direct measurement of the reactor antineutrino spectrum will be provided by the Taishan Antineutrino Observatory (TAO) [45], which is a high resolution anti-neutrino detector which will be placed very close to the reactor.

2.2.2.1 Antineutrino Flux and Spectrum

The expected antineutrino flux from a reactor core can be modeled by [24]:

$$\Phi(E_\nu) = \frac{W_{th}}{\sum_i f_i e_i} \cdot \sum_i f_i \cdot S_i(E_\nu) \tag{2.11}$$

Isotope	Energy release per fission e_i [MeV]	Fission fraction f_i
^{235}U	202.36 ± 0.26	0.58
^{238}U	205.99 ± 0.52	0.07
^{239}Pu	211.12 ± 0.34	0.30
^{241}Pu	214.26 ± 0.33	0.05

Table 2.2: Overview of the mean energy per fission [46] and fission fraction [47] for the four different isotopes in a typical commercial reactor.

where:

- W_{th} is the core thermal power.
- f_i is the fission fraction of the four main isotopes.
- e_i is the thermal energy released in each fission of the i-th isotope.
- $S_i(E_\nu)$ is the neutrino flux per fission for the i-th isotope.

Table 2.2 lists the typical values for the energy release per fission and fission fractions per isotopes in commercial reactors.

The expected antineutrino spectrum in the detector without oscillation effects follows the following equation:

$$S(E_\nu) = \frac{1}{4\pi L^2} \cdot \Phi(E_\nu) \cdot \epsilon \cdot N_p \cdot \sigma(E_\nu) \tag{2.12}$$

where

- L is the distance from the detector.
- ϵ is the detection efficiency.
- N_p is the target proton number.
- $\sigma(E_\nu)$ is the IBD cross section.

Combining Eq. 2.11 and Eq. 2.12, the event rate in the k-th energy bin $[E_k^{min}, E_k^{max}]$ of the detector from several reactor cores is is:

$$R_k(E_\nu) = \sum_r \frac{1}{4\pi L_r^2} \cdot \frac{W_{th}^r}{\sum_i f_i^r e_i^r} \cdot \sum_i f_i^r \int_{E_k^{min}}^{E_k^{max}} S_i(E_\nu) \cdot \sigma(E_\nu) \cdot dE_\nu \cdot \epsilon \cdot N_p \tag{2.13}$$

where k is the bin index and r is the reactor core index.

Concerning the energy spectrum to be expected in JUNO, this is achievable by multiplying the neutrino energy spectrum for the four main fissile isotopes and the IBD cross-section. Assuming no neutrino oscillations, the resulting spectrum is shown in Fig. 2.1.

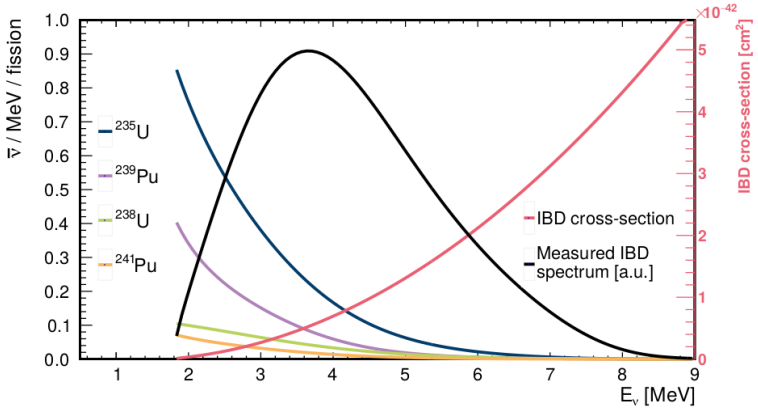

Figure 2.1: The electron antineutrino spectrum emitted by a nuclear reactor. The contributions for the fissile isotopes are parameterized according to [48] and weighted as done in [49]. The measured IBD spectrum (black) assumes no oscillation and is a visualization of the slope in an arbitrary normalization.

Overburden	Meter water equivalent	Muon flux	$< E_\mu >$	R_μ in CD	R_μ in WP
693 m	1800 mwe	0.004 Hz/m^2	215 GeV	3.0 Hz	1.0 Hz

Table 2.3: The simulated muon flux and mean energy at JUNO site. R_μ stands for muon rate, while WP stands for water pool [31, 24].

2.3 Background Sources

Different sources can mimic neutrino-like signals in the Central Detector (CD) [50]. A brief review of the different background causes is presented in the following:

- **Cosmic muons**: to reduce the cosmic muons rate entering the CD, the JUNO experimental site has been chosen to be placed under a 693.35 m (1800 mwe) vertical overburden. Simulation has been run to get an estimate of the muon rate and flux. Results are presented in Tab. 2.3.

- **Neutrons**: Neutrons are mainly produced by muons passing through the JUNO detector. Neutrons produced in the JUNO LS will be tagged with an almost 100% efficiency, while neutrons produced in water will be tagged with an 99.8% efficiency; the 0.2% inefficiency mainly comes from corner clipping muons [24]. The neutron background will be rejected by imposing a large enough veto time after the detection of a passing muon. Un-tagged neutrons (corner clipping muons and from the surrounding rock) entering the LS can produce a prompt proton-recoil signal then captured by H or C in LS, mimicking an anti-neutrino signal. The simulated rate for such event has been estimated to be $\sim$0.1/day [24].

- **Cosmogenic Isotopes**: energetic cosmic muons traveling through the LS can generate radioactive isotopes ($Z \leq 6$) by interacting with ^{12}C. In particular, ^{9}Li and ^{8}He generates the most serious correlated background, as they decay emitting both a beta and a neutron, therefore

mimicking the IBD prompt-delay signature signal. Other long-lived cosmogenic isotopes do beta decay but without the emission of a neutron. These isotopes alone can not form correlated background but can contribute the neutron-like signal if they have beta decay energy in the range of 1.9-2.5 MeV [24].

- **Natural radioactivity**: Particular care has been taken to select low-radioactivity material for the JUNO detector, but it is impossible to get the radioactivity rate down to zero. The radioactive isotopes are ^{238}U, ^{232}Th, ^{222}Rn, ^{85}Kr, ^{60}Co and ^{40}K. The radioactivity sources include the rocks around the detector hall, isotopes dissolved in water, the stainless steel, air, PMT glass, liquid scintillator itself and its container and dust/impurities. A fiducial volume cut is necessary to reduce the rate caused by external radioactivity [24, 50].

2.4 Neutrino Mass Hierarchy

JUNO is designed to resolve the mass hierarchy open question using spectral measurements of reactor antineutrino oscillations. The survival probability of the electron antineutrino can be expressed as [24]:

$$P_{\bar{\nu}_e\to\bar{\nu}_e} = 1 - sin^2 2\theta_{13}(cos^2\theta_{12}sin^2\Delta_{31} + sin^2\theta_{12}sin^2\Delta_{32}) - cos^4\theta_{13}sin^2 2\theta_{12}sin^2\Delta_{21} \tag{2.14}$$

$$= 1 - \frac{1}{2}sin^2 2\theta_{13}[1 - \sqrt{1 - sin^2 2\theta_{12}sin^2\Delta_{21}}cos(2|\Delta_{ee}| \pm \phi)] - cos^4\theta_{13}sin^2 2\theta_{12}sin^2\Delta_{21} \tag{2.15}$$

where

- $\Delta_{ij} \equiv \Delta m^2_{ij} L/4E$ where L is the baseline and E the antineutrino energy
- $\Delta_{ee} = \Delta m^2_{ee} L/4E$, where $\Delta m^2_{ee} = cos^2\theta_{12}\Delta m^2_{31} + sin^2\theta_{12}\Delta m^2_{32}$
- $sin\phi = \frac{c^2_{12}sin(2s^2_{12}\Delta_{21}) - s^2_{12}sin(2c^2_{12}\Delta_{21})}{\sqrt{1-sin^2 2\theta_{12}sin^2\Delta_{21}}}$, $cos\phi = \frac{c^2_{12}cos(2s^2_{12}\Delta_{21}) + s^2_{12}cos(2c^2_{12}\Delta_{21})}{\sqrt{1-sin^2 2\theta_{12}sin^2\Delta_{21}}}$

The ± sign on Eq. 2.15 depends on the MH, with + sign for NH and − for the IH (see Fig. 1.1). The effect is visible on the energy spectrum of Fig. 2.2, where the hierarchy information lays on the spectral distortion. In order to retrieve such spectrum and extract the MH information, an excellent energy resolution (3% @ 1 MeV), a good understanding of the energy response (better than 1%) and a large statistics ($\mathcal{O}$(100k) IBD events) are required.

2.4.0.1 MH Sensitivity and Optimization

To obtain the MH sensitivity, a lest-squares method has been employed and a χ^2 function is constructed as [24]:

$$\chi^2_{\text{REA}} = \sum_{i=1}^{N_{\text{bin}}} \frac{[M_i - T_i(1 + \sum_k \alpha_{ik}\epsilon_k)]^2}{M_i} + \sum_k \frac{\epsilon_k^2}{\sigma_k^2} \tag{2.16}$$

where:

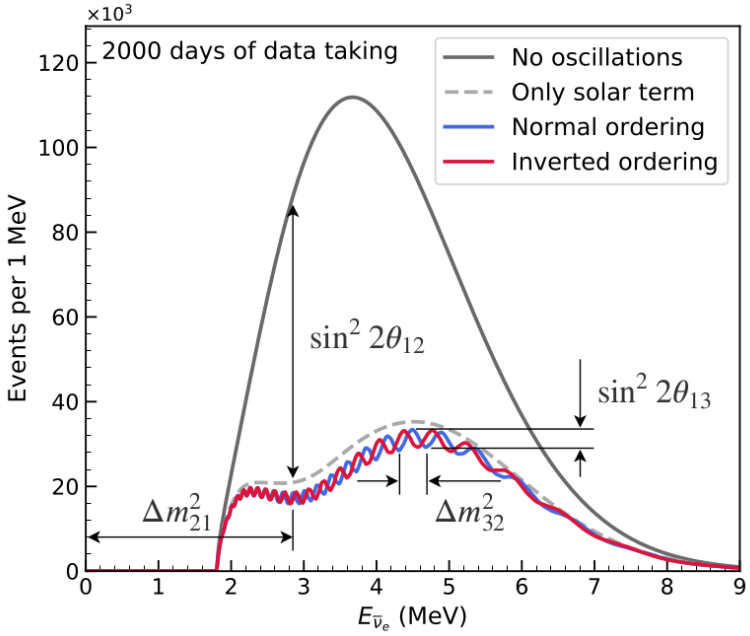

Figure 2.2: The expected anti-neutrino energy spectrum weighted by IBD cross section with and without oscillation at the JUNO experiment for NH and IH assuming 2000 days of data-taking. Dependence of the four oscillation parameters is shown. Figure taken from [33].

- M_i is the measured neutrino events in the i-th energy bin.
- T_i is the predicted neutrino events with oscillations in the i-th energy bin.
- σ_k is the systematic uncertainty.
- ϵ_k is the corresponding pull parameter.
- α_{ik} is the fraction of neutrino event contribution of the k-th pull parameter to the i-th energy bin.

The systematic uncertainties include the correlated (absolute) reactor uncertainty (2%), the uncorrelated (relative) reactor uncertainties (0.8%), the spectrum shape uncertainty (1%) and the detector-related uncertainty (1%).

The spectrum is fitted assuming the NH or the IH with the chi-squared method, and the sensitivity for the discrimination of the MH is obtained by taking the difference of the minima:

$$\Delta\chi^2_{MH} = |\chi^2_{\text{min}}(N) - \chi^2_{\text{min}}(I)| \tag{2.17}$$

where N stands for NH while I stands for IH. The same discriminator can also be used to obtain the optimal baseline (i.e., the baseline that maximizes the MH sensitivity). Fig. 2.3 shows the impact of the overall baseline length for a single reactor and of the relative baseline difference due to multiple

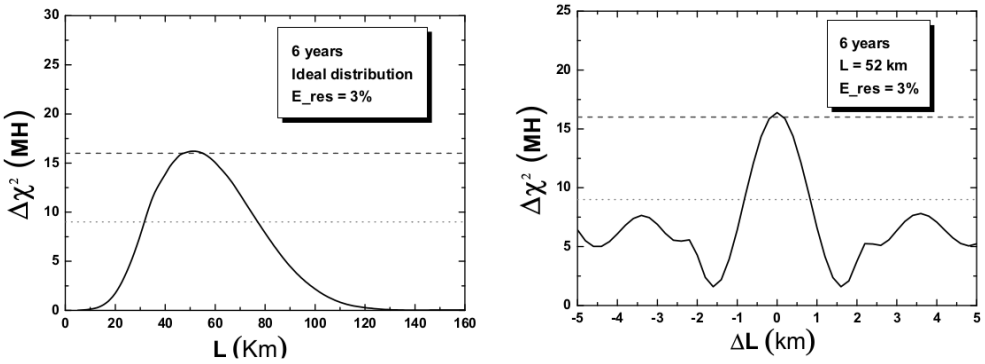

Figure 2.3: MH sensitivity as a function of the baseline length (left) and relative baseline difference from multiple reactor cores (right). Taken from [24]

	Median sens.	Standard sens.	Crossing sens.
NH	3.4 σ	3.3 σ	1.9 σ
IH	3.5 σ	3.4 σ	1.9 σ

Table 2.4: The MH sensitivity with the JUNO nominal setup of six years running [24].

reactor cores. A sensitivity of $\Delta\chi^2_{MH} \simeq 16$ is obtained in the ideal case with identical baselines at around 50 km.

Statistical studies have been performed in order to properly understand the sensitivity results. Two approaches have been followed: the Frequentist statistics approach and the Bayesian statistics approach. Tab. 2.4 reports the median sensitivity, standard sensitivity (defined as $\sqrt{\Delta\chi^2_{MH}}\sigma$) and crossing sensitivity respectively for the JUNO nominal setup, where the commonly defined standard sensitivity is very close to the median sensitivity and can be regarded as the expected sensitivity of the experiment.

On the other hand, the Bayesian statistics performs a comparison of two MH hypothesis. The posterior probability distribution function $p(MH|D,I)$ can be constructed using the prior probability distribution function $p(MH|I)$ and the likelihood distribution function $L(D|MH,I)$ as:

$$p(MH|D,I) = \frac{L(D|MH,I)\cdot p(MH|I)}{\int L(D|MH,I)\cdot p(MH|I)} \tag{2.18}$$

where D represents the data of a measurement, I the prior information on the MH hypotheses and the integration is carried out for all the oscillation parameters. Tab. 2.5 lists the probability ratio for different $\Delta\chi^2_{MH}$ values.

$\Delta\chi^2_{MH}$	1	4	9	16	25
$p(IH\|D,I)$ vs. $p(NH\|D,I)$	38% vs. 62%	12% vs. 88%	1.1% vs. 98.9%	0.034% vs. 99.966%	3.7×10^{-6} vs. 100%
$p(IH\|D,I)/p(NH\|D,I)$	0.61	0.136	0.011	3.4×10^{-4}	3.7×10^{-6}

Table 2.5: Probability ratios with respect to several typical $\Delta\chi^2_{MH} values$.

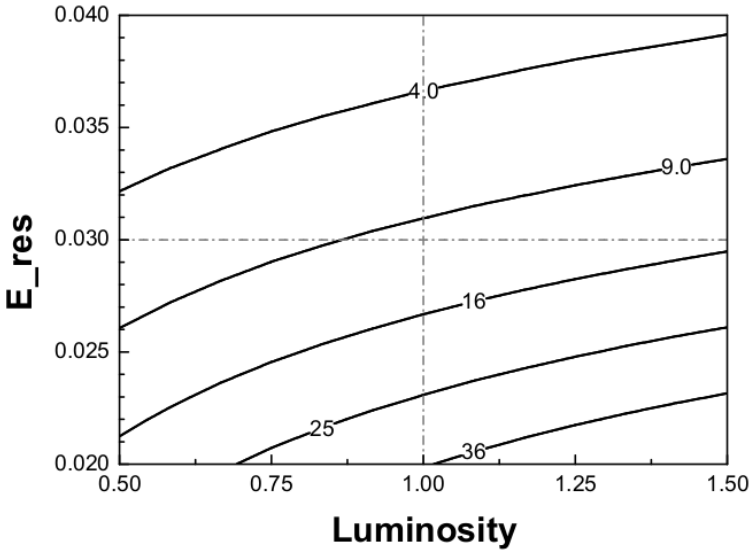

Figure 2.4: The iso-$\Delta\chi^2_{MH}$ contour plot as the function of the luminosity and the energy resolution. The dash-dotted lines stands for the nominal JUNO setup characteristics for a running time of 6 years with 80% signal efficiency [24].

2.4.1 Energy Resolution Requirements

The energy resolution is a key aspect for the MH determination, as its value determine whether JUNO will be able to precisely measure both the fast oscillations (driven by $\Delta m^2_{31} and \Delta m^2_{32}$) and slow oscillations (driven by Δm^2_{21}) at a medium baseline. Fig.2.4 is a iso-$\Delta\chi^2_{MH}$ contour plot which shows the effect of energy resolution vs. IBD event statistics (luminosity). It can be seen that, to achieve the sensitivity of $\Delta\chi^2_{MH} \simeq 16$ or $\Delta\chi^2_{MH} \simeq 25$, an energy resolution of $2.6\%/\sqrt{\mathrm{E(MeV)}}$ and $2.3\%/\sqrt{\mathrm{E(MeV)}}$ is requested, respectively, with the nominal luminosity being 1345 PhotoElectron (PE)/MeV.

In practice, not only the photoelectron statistics determines the energy resolution requirement, but other important factors such as PMT dark noise, noise due to the electronics, the detector non-uniformity and vertex resolution may have an impact. A generic approach to quantify the resolution characteristics and requirement for JUNO can be defined as [51]:

$$\frac{\sigma_E}{E} = \sqrt{\left(\frac{a}{\sqrt{E}}\right)^2 + b^2 + \left(\frac{c}{sqrtE}\right)^2} \tag{2.19}$$

where

- a represents the stochastic term governed by the overall maximization of light (i.e., through the optical coverage, the PMT quantum efficiency and features of the LS).
- b and c are non-stochastic terms controlled by the minimization of systematic effects (by an accurate calibration strategy and by cross-checking the measurements with an auxiliary PMT system).

3

JUNO

JUNO is a neutrino observatory mainly focused on reactor electron antineutrinos from medium baseline Nuclear Power Plants (NPP). As seen in Sec. 2.4, to achieve the highest MH determination sensitivity, JUNO requires equal baselines from the detector to all reactor cores, to avoid cancellation of the oscillation dephasing effect. The baseline length is fixed at about 53 km. A detailed explanation of the experimental site and detector will follow.

The JUNO project has been approved by the Chinese Academy of Sciences in February 2013 and is expected to start commissioning at the end of 2022.

3.1 Experimental Site

The JUNO experiment is located in Jiangmen, Kaiping city in the Guangdong province. A comprehensive map is shown in Fig. 3.1. The experimental site is 53 km from the Yangjiang NPP and Taishan NPP. Yangjiang NPP has six reactor cores of $2.9 GW_{th}$ of thermal power each. Taishan NPP has planned two cores of 4.59GW$_{th}$ each. The total thermal power of the Yangjiang and Taishan NPPs will be 26.6GW$_{th}$. 215 km away, in a spread of 1.1 km, is located the Daya Bay complex, consisting of the Daya Bay NPP, Ling Ao NPP and Ling Ao II NPP, each with 2 cores of 2.9GW$_{th}$. The complex will contribute about 6.4% of the reactor antineutrino events, considering oscillations [33]. Huizhou NPP is under construction, 265 km away from the JUNO site, with six 2.9GW$_{th}$ reactor cores and is expected to be ready around 2025. Apart from an additional site 300 km away, whose plans are unclear, there is no other NPP nor planned NPP in 500 km radius from the JUNO experimental site. In the absence of

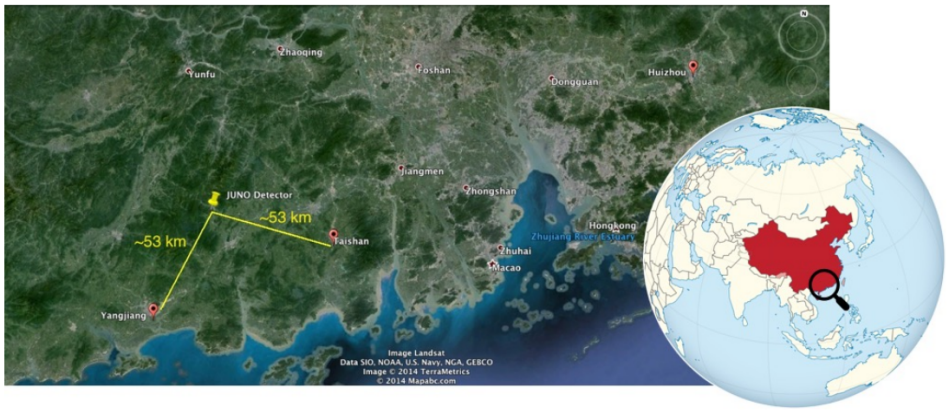

Figure 3.1: Location of the JUNO experimental site.

high mountains in the allowed area where the sensitivity to the MH is optimized, the detector will be deployed in an underground laboratory, with a vertical overburden of 693.35 m (1800 mwe). An aerial picture of the JUNO site, currently still under construction, is shown in Fig. 3.2.

3.2 The JUNO Detector

The JUNO detector includes several sub-systems interacting with each other, but with separate roles. The entire detector with the different systems are shown in Fig. 3.3

The hearth of the experiment is the CD, made up from an acrylic sphere of 35.4 m in diameter filled with 20 kton of LS neutrino active target. Everything is supported by a stainless steel truss which holds two independent PMT systems for light detection. The CD is submerged in a Water Pool (WP) which not only acts as a shield against external radioactivity, but will also be used as a water Cherenkov detector for muon veto purposes. A top tracker is also placed on top of the CD to precisely reconstruct the trajectory of muons to study and suppress the cosmogenic background [53].

3.2.1 The Central Detector

The unprecendent size and energy resolution of JUNO presents several challenges. Several aspects are needed in order the achieve the foreseen features, such as:

- High large PMT photocathode coverage, greater than 75%.
- High large PMT quantum efficienty, close to 35%.
- Long LS attenuation length greater than 20 m at 430 nm.
- High light yield of $\sim$ 10'000 photons per MeV. In combination with the photon detection system of JUNO, this translates to $\sim$ 1345 detected PEs per MeV.

Figure 3.2: Aerial photograph taken on June 23, 2019, showing the construction site of JUNO. Taken from [52].

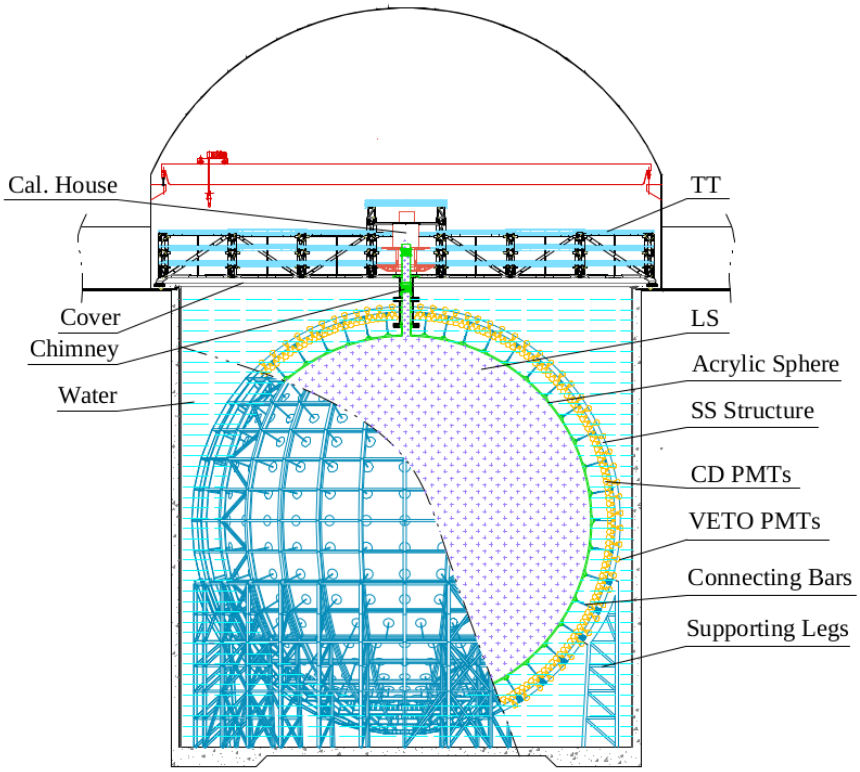

Figure 3.3: The JUNO detector [33].

The LS has a similar recipe as the Daya Bay LS without gadolinium loading [54]. Linear AlkylBenzene (LAB) is used as the detection medium due to its excellent transparency, high flash point, low chemical radioactivity and good light yield. The LS also includes Poly-Phenylene Oxide (PPO) as the flour and p-bis-(o-MethylStyryl)-Benzene (bisMSB) as the wavelength shifter. Two independent PMT system are used for photon detection: 17'612 large 20 inches PMTs and 25'600 small 3 inches PMTs. This double set is necessary to achieve the resolution requirements of JUNO (keep under control the b and c terms in Eq. 2.19).

3.2.2 Photon Detection System

The photon detection system identifies the scintillation light generated by interactions of the neutrinos with the LS. To achieve the target energy resolution of 3% @ 1 MeV, high photocathode coverage is requested, and it is provided by two independent PMT systems. The main system is the large 20 inches PMTs system, whose readout electronics is the focus of this dissertation, contributing with a 75.2% coverage. Additionally, a small 3 inches PMTs system is used for double calorimetry measurements providing and additional coverage of 2.7%.

Concerning the large PMTs, two devices have been selected for JUNO, whose requirements include high detection efficiency for scintillation photons, low dark noise rate, high gain, stable, reliable and long life-time:

- The Hamamatsu R12860-HQE is a conventional dynode PMT developed by the Hamamatsu company. The principle of operation of a dynode PMT is simple: First, the incoming photon is converted to an electron upon hitting the photocathode, due to photoelectric effect [55]. The electron (which is also called PE) is then accelerated through a series of dynode exploiting a High Voltage (HV) electric field; upon hitting the dynodes, more electrons are knocked out. This cascade effect multiplies exponentially the number of electrons until they are collected and measured as a current at the anode. The working principle is shown in Fig. 3.4. The Hamamatsu PMTs feature a Quantum Efficiency (QE) at 400 nm around 30% and a dark noise rate below 50 kHz.

- The North Night Vision Technologies (NNVT) MCP-PMT, developed in China, which incorporates a Micro-Channel Plate (MCP) in place of the conventional discrete dynodes. The MCP consists in a two-dimensional array of channels with a 6-20 μm diameter bundled in parallel. Each channel acts as an independent electron multiplier. As shown in Fig. 3.5, the PEs emitted from the photocathode enter the channels of the MCP and impinge on the inner wall, where they are multiplied by means of secondary emission. The process is repeated along the channels and finally a large number of electrons are collected by the anode as an output signal. The QE on the MCP-PMTs is about 22.86% and the dark noise rate below 100 kHz.

Photos of the two PMTs are shown in Fig. 3.6.

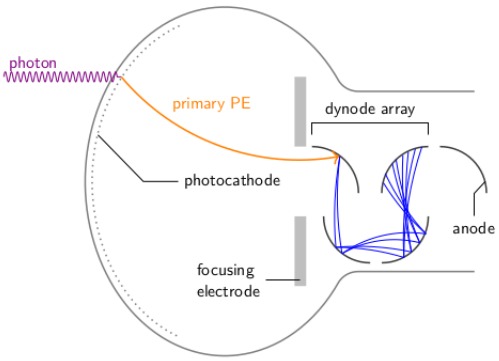

Figure 3.4: Working principle of a dynode PMT. Taken from [56]

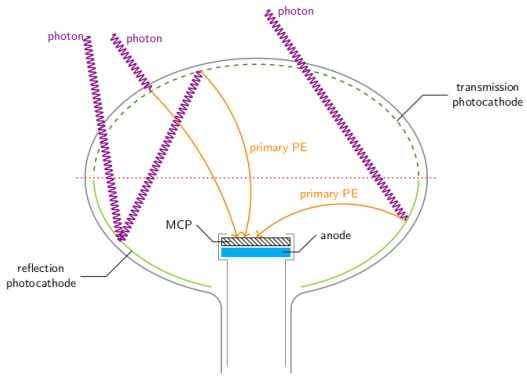

Figure 3.5: Working principle of an MCP-PMT. The reflection photocathode at the bottom part of the glass bulb allows for a second photon-electron conversion chance. Taken from [56]

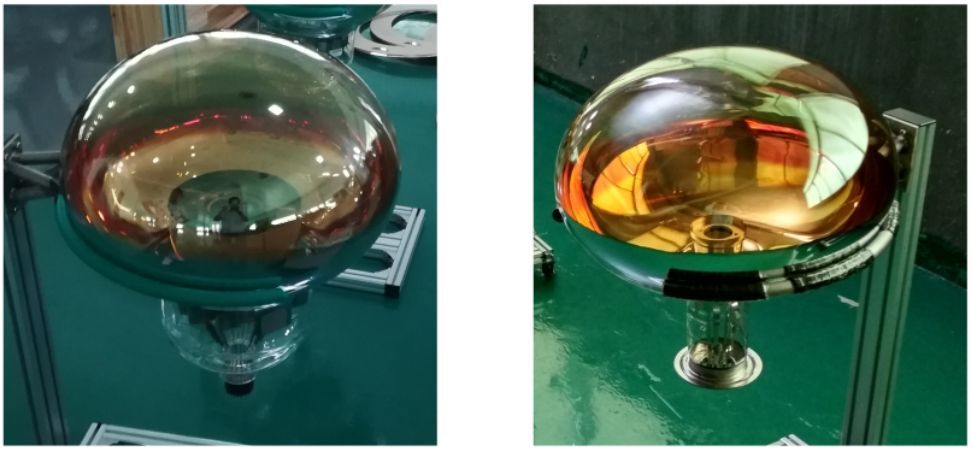

Figure 3.6: Photos of the Hamamatsu R12860-HQE (left) and the NNVT MCP-PMT (right).

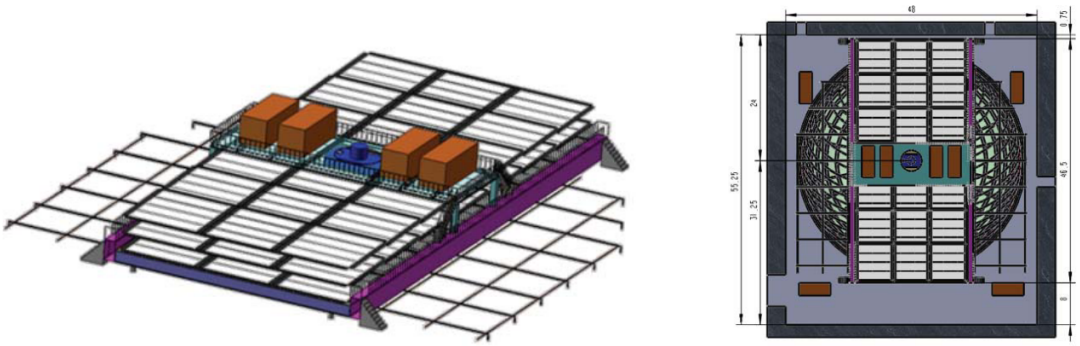

Figure 3.7: The JUNO top tracker.

3.2.3 Veto System

As seen in Sec. 2.3, the CD signal is susceptible to background coming from different sources. As the possibility of rock shielding is limited due to location constraints (see Sec. 2.4.0.1), the only possibility to control the background is an active multi-veto system [57]. Two different systems are employed: an outer veto and a top tracker.

The outer veto exploits the WP in which the CD is submerged in, to act as a water Cherenkov detector. It will feature 35 kton of ultrapure water and will be equipped with 2'400 20 inches large MCP-PMTs. The detector efficiency for cosmic muon rejection has been estimated through simulations to be $> 95\%$. Thanks to the outer veto system, fast neutron background can be limited to a rate of 0.1 event/day, combining passive shielding and muon tagging.

As the top tracker, the target tracker of the decommissioned Oscillation Project with Emulsion-tRacking Apparatus (OPERA) experiment [58] will be used, consisting of 63 walls made of plastic scintillator strips for a good detection efficiency and tracking performance (Fig. 3.7). The strips are equipped with Wave-Length Shifting (WLS) optical fibers, read by Multianode PMT (MaPMT). The walls will be rearranged in three horizontal layers to cover half of the top area. The top tracker will reduce the background rate and will perform a precise muon tracking for cosmic muon induced ^{9}Li/^{8}He study.

3.2.4 The Calibration System

To achieve the target energy resolution and energy nonlinearity, a complex calibration system has been designed for multiple source deployment covering the full CD volume [51]. As shown in Fig. 3.8, the different systems are:

- The Automatic Calibration Unit (ACU)
- The Cable Loop System (CLS)
- The Guide Tube Control System (GTCS)

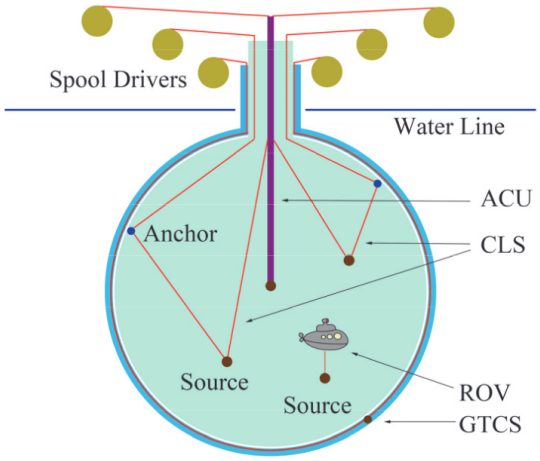

Figure 3.8: Schematic diagram of the JUNO calibration complex.

- The Remotely Operated under-liquid-scintillator Vehicle (ROV)

ACU, CLS and GTCS will be combined to deliver ^{40}K to specific positions along one plane for non-uniformity corrections, and ROV will be used for full volume scan when needed. The calibration data from the different system will play a crucial role in defining the JUNO response function, correcting the energy response uniformity. Energy linearity will be corrected by placing various sources at CD center with ACU. Energy non-linearity for positron events at CD center shall be less than 0.5% after correction [59].

Part II

The JUNO Readout Electronics

4

JUNO Readout Electronics Overview

The number of PEs generated by a single large PMT ranges from one PE for low-energy events up to thousands PEs in case of showering muons or muon bundles. In both these extreme cases, the photoelectrons arrival time profiles have to be determined and the energy of the event has to be reconstructed. The energy resolution is a key parameter for the JUNO neutrino mass hierarchy determination and the PMT readout electronics must be designed in order to comply with the requirements: for an energy release of 1 MeV in the central detector, which corresponds to an average of 1345 PEs, a 3% energy resolution is expected [34].

The JUNO readout electronics will have to cope with the signals from different PMT systems. The CD features 17'612 large PMTs, which can be considered as the main system, plus an additional independent set of 25'600 small PMTs for double calorimetry purposes. An additional set of PMTs is to be found in the WP surrounding the CD, adding an extra set of 2'400 PMTs. The reader can appreciate the challenge of the readout electronics system to extract valuable information from correlated PMT hits caused by physical events from a sea of random dark noise.

The main task of the readout electronics is to

- Receive and digitize the analog signals from the PMTs and transmit all the relevant information to the Data Acquisition system (DAQ) without a significant loss of data quality.
- Generate local trigger requests based solely on the single-PMT waveform and transmit this information upstream in order to be evaluated globally. The resulting globally-validated trigger information has then to be sent back to the Front-End Electronics (FEE) to determine the useful information to send to storage

It's development is the result of a collaboration effort from several countries and institutions: the Institute of High Energy Physics (IHEP) in Beijing, China, Tsinghua University in Beijing, China, Istituto Nazionale di Fisica Nucleare *(National Institute for Nuclear Physics)* (INFN)-Padova/University of Padova, Italy, INFN-Roma/University of Roma Tre, Italy, the Joint Institute for Nuclear Research (JINR), Dubna, Russia, among others.

After a general picture, the thesis focuses on the FEE, whose Global Control Unit (GCU) represents the main component. The responsibility for designing and developing the GCU board has been given to INFN-Padova/University of Padova.

4.1 Specifications

The electronics design, in terms of both hardware and firmware, is driven by the following key-points [34]:

- **Energy Reconstruction**: optimization of the energy measurement of $\overline{\nu}_e$, especially at the lowest energies. A basic limitation on the energy resolution arises from the statistics of detected PE and this limit must not be worsened significantly by the effect of electronics. At a photoelectron yield of 1345 PE per MeV, the achievable relative resolution is ∼3% at 1 MeV.

- **Photon Arrival Time Pattern Reconstruction**: precise reconstruction of the photon detection time pattern in the detector is essential in order to retrieve the position of the events. This is particularly important for the IBD events induced by $\overline{\nu}_e$'s, since (a) the energy response of the detector will be position-dependent and (b) precise space-time information of the events allow for an efficient detection and discrimination of prompt positron and delayed neutron events, which will support background suppression.

- **Low Dead Time and Dynamic Acquisition Rate**: the readout electronics not only has to be able to acquire neutrino events from reactor, solar, geological or atmospheric origin without inefficiency, but it has also to be designed in order to cope with short episodes of extremely high trigger rate that might be caused by neutrino bursts from a nearby galactic SN. Dependent on the distance, thousands of neutrino events are expected within a period of seconds.

4.1.1 Data Acquisition

The reconstruction of the events deposited energy will be performed by charge-integration and, despite this being technically the simplest solution, it still presents some challenges, both hardware-wise, concerning the dynamic range of the readout electronics and firmware-wise, concerning what and how the information is sent from the FEE to the DAQ. In fact, the reconstruction is complicated by the spread in the arrival time of the photons, which is caused by the fluorescence time of the LS, photon time-of-flight and photon scattering. All of these contribute to delays in the order of several hundreds nanoseconds. An additional distortion of the time-pattern will be introduced in case of cosmic muons

where the light is generated along the extended particle track, causing a delay by the time-of-flight of the muon ($\leq$ 120 ns) [34].

To reconstruct the time & energy profile of the events as efficiently as possible, and to comply with the possibility of an extreme increase in data rate, the readout foresaw three data acquisition systems:

- The *default readout* system is able to sustain data rates caused by ordinary neutrino evens (e.g. nuclear, solar, geo ... neutrinos) and relies on internal Field Programmable Gate Array (FPGA) memory. It provides the DAQ with the full digitized waveform inside a time-window. The length of the window is controllable by the user, through the slow-control software. Preliminary calculations shows that, including time-of-flight effects (e.g. for an off-center event close to the surface of the acrylic sphere or a cosmic muon) a time window of 500 ns is sufficient. Anyway a tradeoff is required since longer windows allows the storage of more scintillation light, but increase the contribution from the electronics noise. Due to the electronics noise, the potential of the baseline will vary around zero, but the integration of such baseline without a signal will not give exactly zero, scattering around zero with a width of the distribution that increases with the square root of the integration time.

- The *QT readout* system consists in a charge and time stream where an online integration of the PMT pulse is performed. The data-per-event sent to the DAQ is consistently lower compared to the default acquisition, and this allows the acquisition to sustain much higher data rates. The algorithm to deploy in FPGA for the online charge integration to best estimate the energy is still under study.

- In case of a SN burst event, a sudden increase of the neutrino event rate in the CD is foreseen, and the internal FPGA memory buffer would readily overflow. To avoid losing events, the *complementary Double Data Rate (DDR) readout* path is designed, relying on external on-board Random-Access Memory (RAM) memory modules, which are able to sustain a much higher event rate. Once the SN event is finished, the memory can be read out.

4.1.2 Triggering schemes

Different triggering schemes are integrated in the JUNO readout electronics. During data taking, the schemes that are foreseen to be used in JUNO are either global, based on the information of all channels, or de-centralized, based on self-triggering channels that send all their digitized signals (including all dark noise PE) to the DAQ. During the development, testing and commissioning phases, different triggering schemes are used for debugging purposes: they range from an external trigger scheme, where the Back-End Electronics (BEE) is triggered by an external signal forwarded to the FEE for acquisition, to a network trigger scheme, where the user can send triggers to the front-end cards through slow-control.

In case of a **Global Trigger**, the information from all PMTs are combined in order to form a global trigger decision that starts the readout of all the PMTs instrumented. To realize this trigger, a synchronous link is employed to both transfer the hit information from all the front-end boards to the

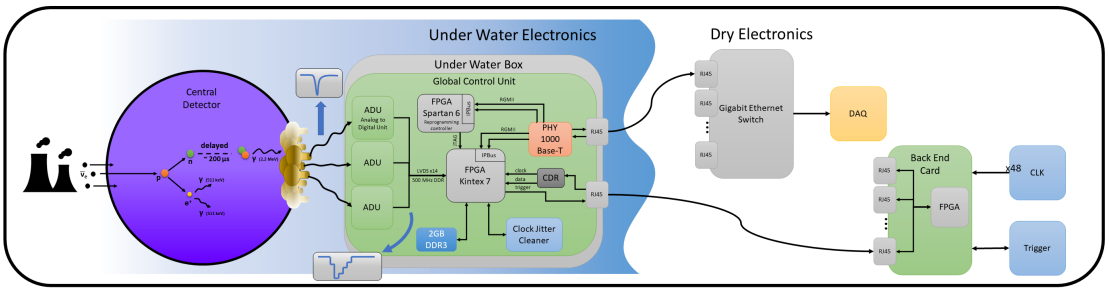

Figure 4.1: The JUNO Large PMTs Readout Electronics

Central Trigger Unit (CTU) and the global validated trigger timestamps back from the CTU to the FEE to start the readout. The global trigger scheme is used by the *default readout*, bringing advantages to the aspect of energy reconstruction as it is the only configuration that will allow the recording of waveforms for channels in which the PMT signals are below an individual trigger threshold, i.e. the detection of low-charge photoelectron. On the other hand, the use of a global trigger limits the maximum event rate, due to the necessity of sending the timestamps of the validated trigger to the FEE. This is particularly important in case of a neutrino burst from a supernova explosion, where data rates increase drastically. This is the case where the **De-centralized Trigger** is useful, as this trigger scheme is used by the *QT readout*, saving the self-triggered charge & time information in a local buffer of appropriate size that gets emptied out to the DAQ as soon as the SN neutrino-burst is over, and by the *complementary DDR readout*, saving the entire waveform on the external memory. With this trigger scheme, the threshold can be individually set for each channel, and as soon as the signal exceeds it, the digitized data is extracted for further analysis.

4.2 The Electronics Chain

For the readout electronics, a “wet-scheme” has been chosen by the collaboration, in which the FEE electronics will be submerged in the WP surrounding the acrylic sphere that contains the LS, together with the PMTs. The FEE, placed inside water-tight boxes coupled to the CD stainless steel truss, is in charge of the digitization of the PMT signal and their first elaboration, while all the digital communication with the “dry” BEE as well as with the external online farm are achieved by standard Category 5 Enhanced (Cat-5E) copper twisted cables. All the under-water cabling are protected inside a stainless steel bellow.

These Under-Water Box (UWB) manages the information of three large PMTs and are placed as close as possible to the PMTs themselves. Thus, the underwater scheme minimizes the deteriorating effects of analog signal transmission over long cables. On the other hand, underwater electronics is not replaceable during operation, increasing the requirement for the electronics reliability.

By referring to Fig. 4.1, the whole JUNO electronics works as the following:

- First of all, $\overline{\nu}_e$ generated by nuclear power plants travel through the JUNO CD. In here some

of these neutrinos will undergo the IBD reaction, and scintillation photons are generated accordingly.

- These photons are detected by the PMTs, resulting in negative pulses on the PMTs output analogue signal.
- In groups of three, the PMTs are connected to the UWB, where the first step is the digitization of the signal by the Analog to Digital Unit (ADU), which are the digitization components of the main FEE board, the GCU
- The digitized signal is analyzed by the GCU's main FPGA. The leading tasks here are the generation of primitive trigger requests and signal storage, waiting for a global trigger validation decision (in case the global trigger scheme is being used). A second "support" FPGA is present on board, but information on its tasks, as well as a more detailed description of the main FPGA's functions, are provided in Sec. 7.2.
- From the UWB, two cables connects to the "dry" electronics: (a) an asynchronous Ethernet link over Cat-5E Unshielded Twisted Pairs (UTP) cable to connect to the DAQ and (b) a custom synchronous link over Cat-5E Shielded Twisted Pairs (STP) cable to connect to the Back-End Card (BEC).
- The DAQ performs data acquisition as well as slow-control operations. The protocol used is the IPBus protocol [60], which adds a layer on top of the User Datagram Protocol (UDP), for a reliable network communication. The adopted standard is the 1000BASE-T, therefore 1 Gbps as full bandwidth.
- The synchronous link is a fixed latency link used for the timing and trigger system. The link is fully custom, but shares some features with the Timing, Trigger and Control (TTC) project developed at Conseil Européen pour la Recherche Nucléaire *(European Organization for Nuclear Research)* (CERN) [61]. The link connects the GCU with the BEE, in particular with the CTU, where all the primitive trigger requests are gathered and analyzed, and a global trigger decision is formed and sent back to the GCU. The BEE, through the synchronous link, performs also the timing synchronization through the IEEE 1588-2008 Precision Time Protocol (PTP) protocol, achieving nanoseconds timing precision [62].

4.3 Synchronization and Clock Distribution Scheme

In JUNO, the primary task of the time-based timing system is to handle an accurate time distribution and clock synchronization. More specifically, the clock system for JUNO has two major functions. It will provide:

- a standard reference frequency to all the FEE modules to support the waveform sampling and processing logic

- an accurate copy of the global time between BEE and FEE, to provide an absolute synchronized timestamp for each event to correlate, in order to extract the neutrino event and reconstruct key parameter (e.g. energy, interaction vertex etc.)

The distributed clock network applied to JUNO, up until the BEC level, is based on the White Rabbit (WR) standard [63]. The WR system is a technology originally developed by CERN and Gesellschaft für Schwerionenforschung *(Centre for Heavy Ion Research)* (GSI) for the use at accelerators. It is based on IEEE 1588-2008 PTP including two further enhancements: the precise knowledge of the link delay and a possibility of clock synchronization over the physical layer with Synchronous Ethernet (SyncE). Applying WR in JUNO will offer the following advantages [34]:

- The low-jitter recovered clock from SyncE provides a reference frequency for the electronics.
- Sub-ns phase alignment can be achieved among all nodes by phase measurement and phase compensation.
- The PTP synchronize the timestamp among all BEC nodes

From the back-end level synchronized through the WR network, the global clock signal must be distributed to the front-end cards that count the time locally. The timing system ensures that

- The clock signal is distributed from the CTU to all the GCUs, to avoid any drifting of the local counters.
- The offset between the counters with respect to the global time counter is measured and corrected.

The FEE can not exploit the synchronization features of the WR network, since the potting of underwater electronics imposes tight constraints on the number of communication channels and medium between the BEC and each GCU. The synchronous link is in charge of the timing information distribution between back-end and front-end electronics, and the adoption of WR on copper cables (Cat-5E) would nullify the benefits of the phase tracking procedure foreseen by WR, degrading its resolution.

After considering different approaches, the synchronization procedure between the back-end and front-end layer has been based on an hardware implementation of the IEEE 1588-2008 standard [64], which theoretically guarantees the synchronization between global and local clocks inside a window of ± one clock period [62].

4.3.1 The IEEE 1588-2008 PTP Protocol

IEEE 1588-2008 standard [64] defines a protocol for precise clock synchronization applicable to systems that implement a multicast communication model between the master and timing nodes. In JUNO the idea is to exploit the delay request-response mechanism measurement defined in the IEEE 1588-2008 standard to compensate for the offset error between BEE and FEE. Figure 4.2 shows the protocol implemented. $t_{1g} - t_{1l}$ is the clock offset to be measured and compensated. The offset measurement procedure is accomplished in eight steps:

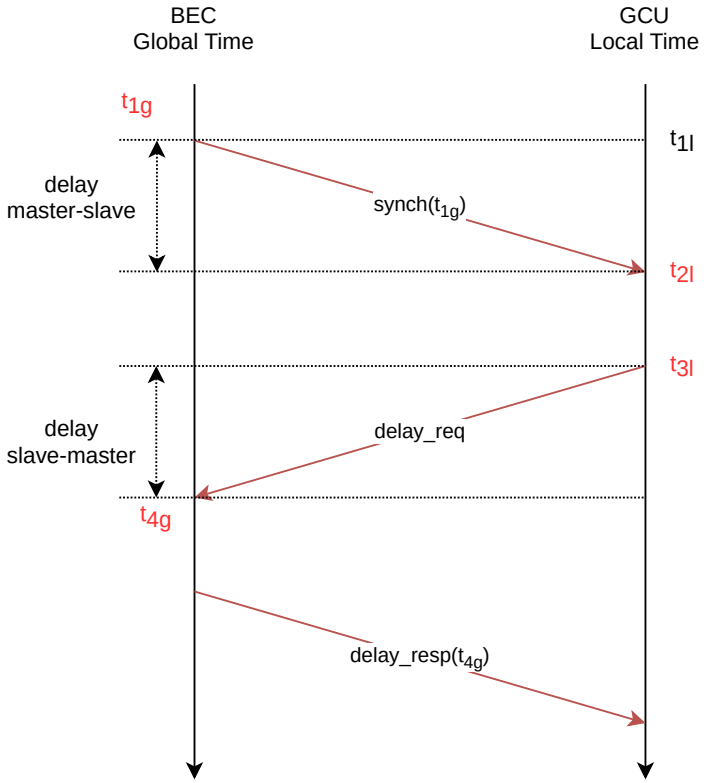

Figure 4.2: IEEE 1588 PTP offset measurement ©2008 IEEE.

1. The master records the current timestamp t_{1g} and sends to the slave a *synch* message containing the timestamp t_{1g}
2. The slave records the reception time t_{2l}. The slave computes $t_{1g} - t_{2l} = offset - delay_{ms}$ where $delay_{ms}$ is the transmission delay from master to slave.
3. The slave sends a delay request message, without payload, to the master and records the transmission time t_{3l}.
4. The master records the reception time t_{4g}.
5. The master sends back a delay message containing t_{4g} value.
6. The slave, upon receipt of the *delay_resp* message computes $t_{4g} - t_{3l} = offset + delay_{sm}$.
7. Now, with the assumption that $delay_{ms} = delay_{sm}$, the offset can be computed using:

$$offset = \frac{(t_{1g} - t_{2l}) + (t_{4g} - t_{3l})}{2} \tag{4.1}$$

8. The slave correct its clock accordingly

The master individually addresses the offset correction procedure to each slave. The procedure can be run at any time, thus ensuring clock alignment during the run of the experiment and offering the possibility to check the synchronization status of all the GCUs. Too frequent offset corrections are indicative of problems and the corresponding GCU should be brought offline for diagnosis and firmware maintenance.

4.3.2 PTP Performances and Limiting Factors

The offset correction mechanism highlights the sources of error that potentially bound the clock alignment accuracy:

- the protocol does not specify the clock frequency; lower clock frequencies lead to poorer time resolution
- Timestamping is a time critical operation. Hardware-assisted timestamping is required to achieve time synchronization in the ns range.
- The synchronization over standard Ethernet Local Area Network (LAN) rarely goes beyond the $\mathcal{O}(\mu s)$ of accuracy due to packet latency in the Ethernet network that is traffic dependent. The best performances of PTP over Ethernet are usually achieved with the Deterministic Ethernet, a communication technology that uses time scheduling to ensure a bounded and low latency transmission of the critical scheduled messages. JUNO timing system relies on a deterministic latency for each of the 20'012 channels.
- Like all message-based synchronization protocols, PTP time accuracy is degraded by asymmetry. Asymmetry usually originates from the physical medium and from the implementation of the data link layer. The assumption $delay_{ms} = delay_{sm}$ is not true in presence of asymmetry. Specifically, the time offset error is $1/2$ of the asymmetry.

4.4 Power

Each UWB needs a 36 Volt DC-power for both the GCU power and HV generation. The voltages are generated by power supplies in the cavern on top of the detector, so they are accessible and replaceable in case of failures. Each UWB is provided with dedicated low-impedance wires for power, placed inside the protecting bellow together with the two Cat-5E data links (synchronous and asynchronous link).

5

The Dry Electronics

The dry electronics is composed of the BEC, which is used to link the UWB to the trigger system, and the CTU, needed to provide the front-end with Level-1 global trigger decisions.

5.1 Back-End Card

The BEC [65] represents the first layer of the dry electronics, responsible of direct communication with the underwater electronics. It is used to concentrate the signal coming from up to 48 front-end

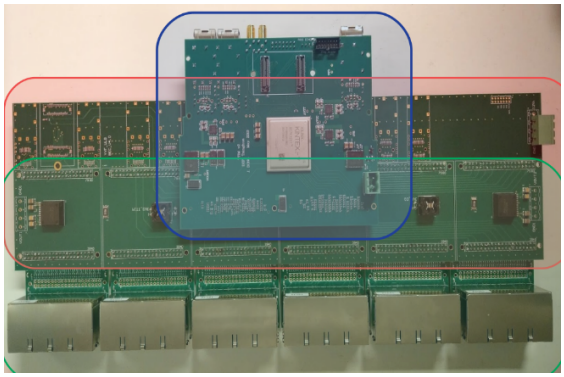

Figure 5.1: Picture of the back-end card. Trigger and Timing FMC is shown in the blue box; the red box represents the base-board and the green box contains 6 RJ45 mezzanine cards [65].

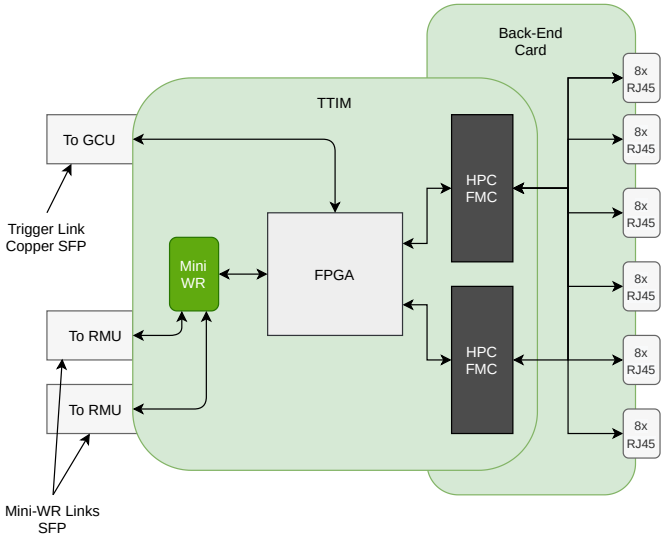

Figure 5.2: TTIM card logical scheme.

boards, providing a bridge for the timing system distribution protocol, between the WR and the IEEE 1588-2008 standard. A picture of the BEC is visible in fig. 5.1.

The BEC is made up of three components:

- The RJ45 mezzanine cards
- The base-board
- The Trigger and TIMing (TTIM) FMC.

As the name suggests, the RJ45 mezzanine cards provide the physical RJ45 connection sockets while allowing the possibility for an easy replacement in case of failure. One card is equipped with 8 connectors, therefore a single BEC can potentially connect to 6 mezzanines. The board also features cable equalizer chips for equalizing data trasmitted over long (up to 100 m) copper cables.

The base-board provides the power distribution as well as routing all the signals from the RJ45 mezzanine cards to the two FMCs connectors which are used to plug the TTIM board.

5.1.1 TTIM Card

The TTIM board is a crucial component of the trigger and timing system. It interfaces with 48 synchronous link coming from 48 different GCUs; since each synchronous link interface consists of four different input pairs for each twisted pair in a Cat-5E cable, this equals to 192 Low-Voltage Differential Signaling (LVDS) pairs per board. Besides the GCU, the TTIM connects to the Reorganize and Multiplex Unit (RMU) which eventually connects to the CTU. This connection is carried out by Bi-directional 1.25 Gbps optical links, which not only are used to forward trigger information upstream, but they are essential to retrieve the global clock and global time of the experiment as well as provide

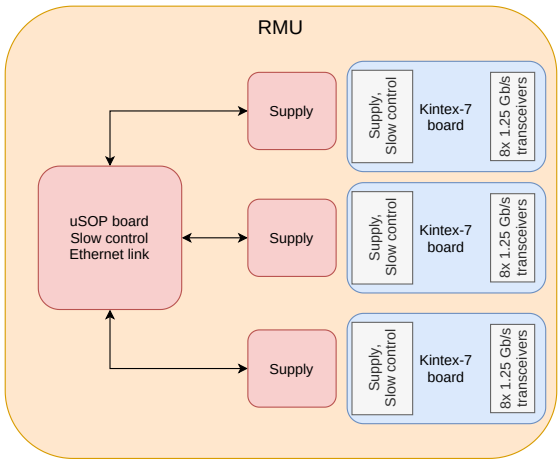

Figure 5.3: Block diagram of the RMU board. The blue modules are the mezzanine cards, the middle modules are the power distribution units and on the left side the uSOP card [67].

slow-control functionalities. The board is powered by a Xilinx Kintex-7 FPGA, a XC7K325T-FFG900 device, which ensures that all the requirements are satisfied.

To provide an easy WR node implementation, a castellated-edge connection with a Mini-WR module is foreseen [66]. A block design of the TTIM board is shown in Fig. 5.2

5.2 Reorganize and Multiplex Unit

The RMU [67] aggregates the information delivered by 20 BECs, providing a front-end trigger optical bridge. The data throughput of a single BEC output link has been estimated to be 0.5 Gbps, thus the RMU delivers a 10 Gbps output raw data throughput, with all the link running at fixed latency to the CTU.

The RMU is composed by three mezzanine cards, based on Xilinx 7-Series FPGAs, performing data concentration tasks. Each mezzanine board is equipped with 8 Small Form-factor Pluggable (SFP) cages, 7 of them provide a connection to the BEC, while the remaining one delivers the aggregated output stream to the CTU. A fixed latency data transfer protocol has been implemented, since deterministic latency is necessary in trigger systems, where the receiving end requires a predictable arrival time of the information.

Other components of the RMU consist in:

- Three power distribution units, to deliver power to the mezzanine optical link cards
- The uSOP board [68], a control unit performimg slow-control tasks. It is also needed for clock distribution, as it is connected to the WR network.

A block diagram of the RMU is visible in fig: 5.3

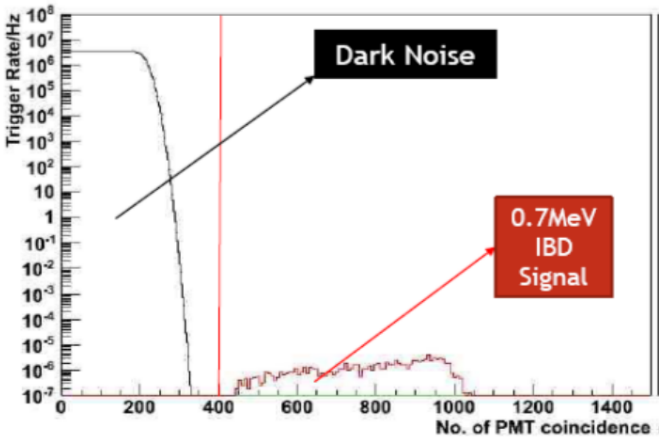

Figure 5.4: Event rate of PMT dark noise [69].

5.3 Vertex Fitting Logic and Central Trigger Unit

The main objective of the hardware trigger system will be to distinguish the thermionic emission of the PMTs, called dark noise, from the normal neutrino signal. This can very well be done by setting a certain multiplicity value; for example, Fig. 5.4 shows the calculation result of dark noise caused coincidence rate compared to the physical event rate for a fixed trigger window, dark noise rate and 15'000 tubes [69]. By setting the multiplicity threshold around 400, the dark noise coincidence events can be easily separated from IBD neutrino events that have a minimum deposit energy of 0.7 MeV. Unfortunately, this approach is not efficient considering solar neutrinos and supernova elastic scattering neutrinos, which are located at an energy range as low as 0.2 MeV and the multiplicity distribution of such event overlaps with the PMT dark noise. Approaching this low-energy range introduces difficulties for the DAQ system, as the readout rate increase significantly, requiring high bandwidth and expensive hardware.

A possible solution could come from the awareness of the vertex position information in the trigger system. Identifying the vertex we are able to concentrate the correlated PMT hits into a narrower time region, so smaller trigger window could be used, reducing the overall bandwidth and data to store on disk.

The output of 24 RMU composes the full hit information that are used for the vertex fitting. The Vertex Fitting Logic (VFL) modules are still in development, but prototypes are already being evaluated on Xilinx V5LX220 devices.

The VFLs work in conjunction with the CTU, shown in Fig. 5.5, where information from the VFLs modules are analyzed to generate the final trigger. The CTU is also needed as an interface for the calibration and veto system. Diagnostic features will also be implemented, such as random/periodic triggers as well as flow control features like throttle or scale. The CTU fan-outs the trigger information to all the RMUs and finally to all the GCUs for a global acquisition of the event.

The global time of the experiment is retrieved in the CTU thanks to the same mini-WR castellated-

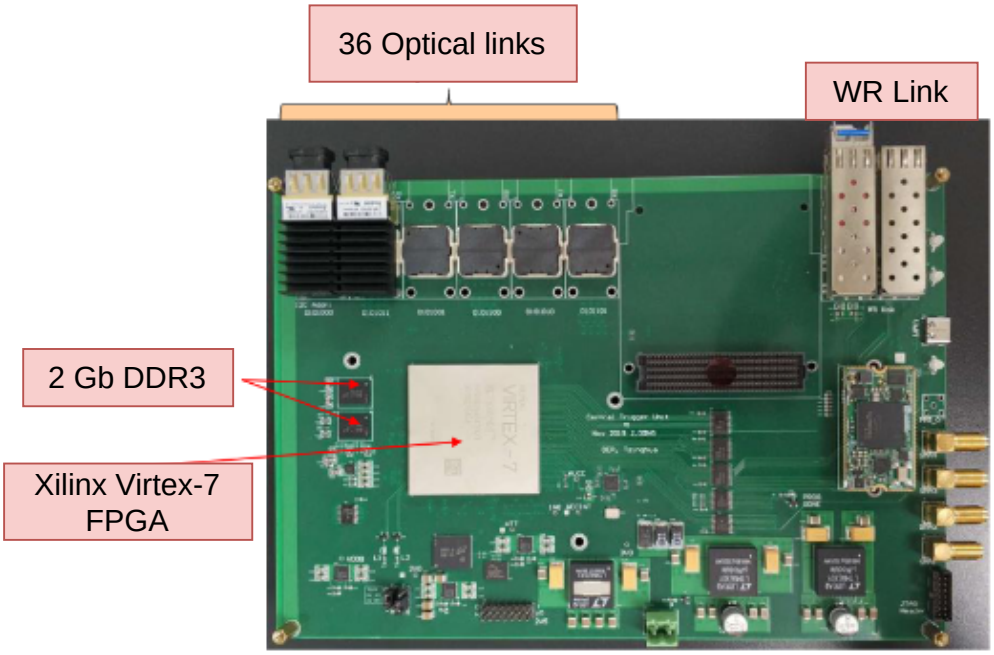

Figure 5.5: The Central Trigger Unit board.

edge module that allows to connect to the WR network.

6

The Global Control Unit Board

The GCU is the core of the JUNO readout electronics and represents the first stage in the PMTs waveform digital processing. Among many tasks, the GCU is responsible for the acquisition of digital waveform generated by three PMTs, the generation of local triggers together with the reconstruction of the charge and time and the data readout to the DAQ upon a trigger request. As the requirements for modern physics experiments are increasing, cutting-edge technology needs to be employed to face challenges such as high data rate and high capacity DAQ systems. An FPGA-based solution was foreseen to tackle the demanding tasks for the JUNO front-end electronics. A picture of the GCU board is shown in Fig. 6.1.

INFN-Padova/University of Padova is the group responsible for the GCU board. The focus of my PhD has been the characterization of the board, the development of it's FPGA configuration and a comprehensive testing. The work is detailed in the following sections and chapters.

6.1 Design Guidelines

The GCU is the first electronics board in the readout electronics chain, placed inside an UWB. The design of the GCU has been carried out following some guidelines, which results from design constraints and requirements, essentials to reach the ambitious goals of JUNO. The guidelines are the following:

- **Reliability**: The "wet" electronics cannot be accessed after liquid scintillator filling, therefore meeting the reliability criteria is a key point for the GCU. JUNO requires less than 1% of the channels failure during the first six years of operation. By assuming that half of the failures

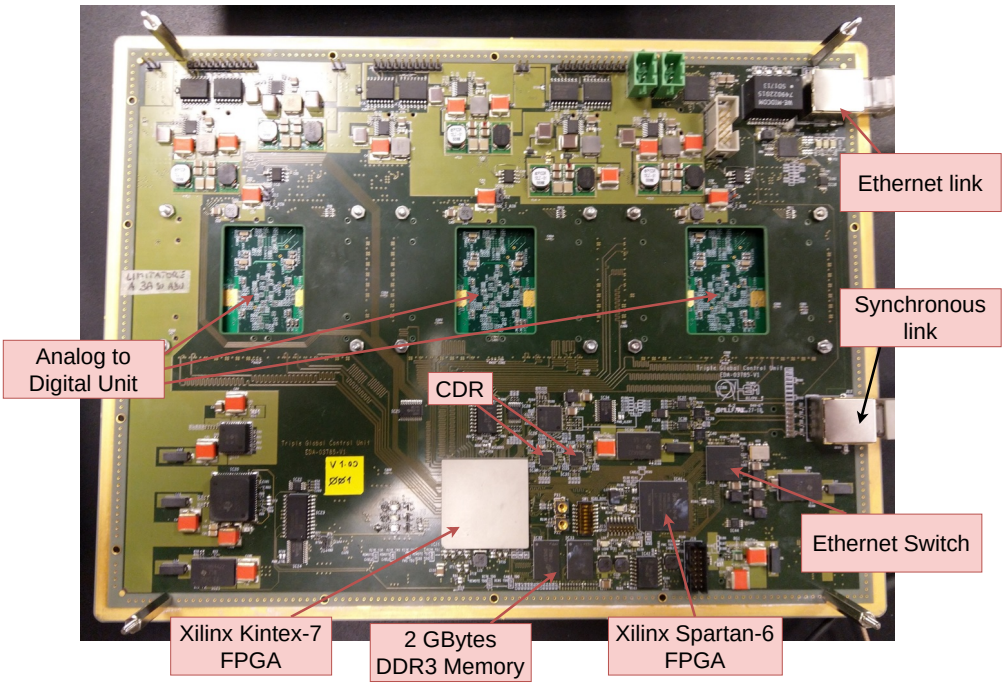

Figure 6.1: The Global Control Unit board with its main hardware component.

stem from PMTs, less than 0.5% of electronics failure is allowed. The Printed Circuit Board (PCB) design, the choice of components and the firmware design as well, have been driven by the necessity of meeting this tight reliability requirement.

- **Remote reconfiguration and debug**: The boards must always ensure the possibility of reconfiguration, even during the data-taking phase. Moreover, a fail-safe mechanism must be employed, to make sure no boards are lost due to erroneous configuration. The possibility of using standard FPGA debug techniques, such as Xilinx debug cores like the Integrated Logic Analyzer (ILA) Intellectual Property Core (IPC), should also be provided, in order to ease the commissioning phase of the experiment as well as helping in solve potential bugs that may arise later.

- **Data readout standardization**: The DAQ link, in charge of the data readout and slow-control, is based on the Ethernet 1000BASE-T standard. This allows the transmission of Ethernet frames at a rate of 1 Gbps as well as use of cables and equipment that are widely available and economical. In fact, the readout network will extensively use commercial Ethernet switch for the packet-routing from the GCUs to the DAQ servers, which will be equipped with standard Network Interface Cards (NIC).

- **High-frequency digital sampling and dynamic range**: Concerning the analog PMT signal digitization, the rise time of the JUNO PMTs is about 2.5 ns. This translates in a required bandwidth of about 400 MHz and therefore a sampling rate of 1 Gsample/s is considered appropriate. Also, the digital waveform should be able to handle a big dynamic range, from 1

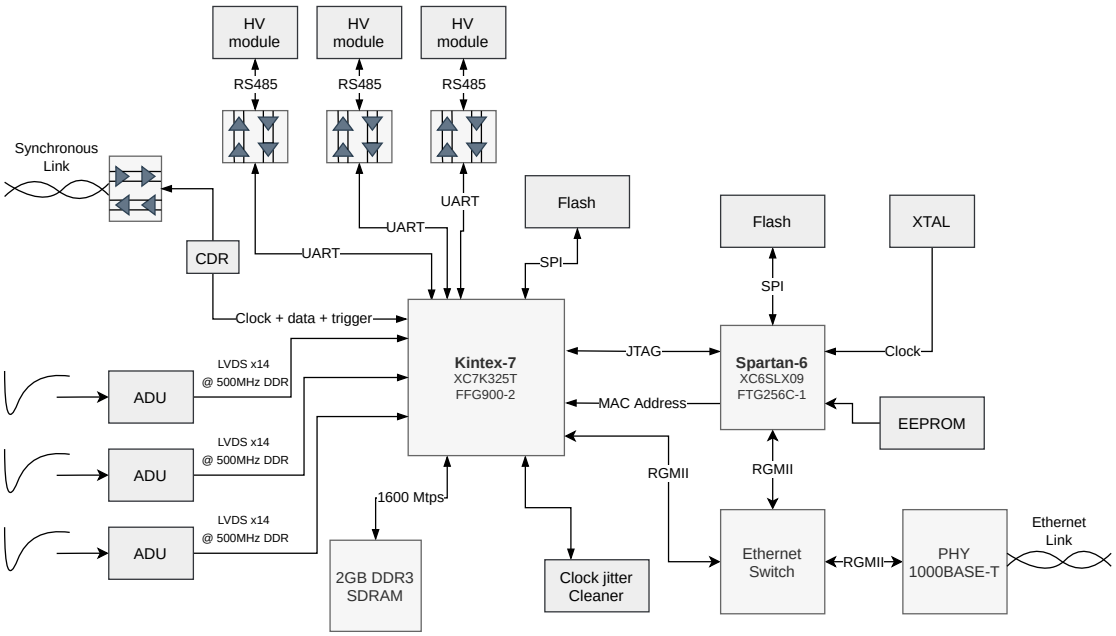

Figure 6.2: GCU board block diagram.

to 1000 PE.

- **High event-rate dynamic range**: While the main aim of JUNO is the discovery of the neutrino mass hierarchy, other unsolved questions can find their answers exploiting this un-precedent detector. One possible scenario is the detection of a SN explosion which, depending on the distance, would increase dramatically the data rate for a short period of time. The GCU must therefore be able to handle 1 KHz of data, expected during normal operation, as well as 1 MHz for very short periods of time, as expected during SN bursts.

6.2 GCU's Main Features

Figure 6.2 shows a graphical representation of the GCU board main features. All the main components and peripherals shown are intended to satisfy the list of requirements and design guidelines for the front-end readout electronics of JUNO. The core of the board is defined by the main FPGA, a Xilinx Kintex-7 [70], which represents a good trade-off between power consumption, cost, number of available Input/Output (I/O) and reliability. A second FPGA is mounted, a Xilinx Spartan-6 [71], which plays an essential role to ensure the reliability, re-programmability and the fail-safe feature of the GCU.

6.2.1 FPGA

FPGAs are integrated circuits designed to be configured many times after manufacturing. Once programmed, the chip behaves similarly of an Application-Specific Integrated Circuit (IC) (ASIC). FPGAs represents the evolution from earlier devices such as Programmable Read-Only Memory (PROM) and Programmable Logic Device (PLD). While these devices are based on fuse technology and their configuration could not change once programmed, FPGAs store their configuration information in a re-programmable medium such as Static RAM (SRAM) or flash memory.

Concerning the GCU, FPGA technology is used to manage all the task assigned to the FEE, such as PMT waveform processing, data readout and chip configuration through on-board communication buses, such Serial Peripheral Interface (SPI). Most of these task are handled by the main FPGA on-board, a Xilinx Kintex-7 XC7K325T device, in a FFG900 package. A smaller FPGA for support has been added on the GCU, a Xilinx Spartan-6 XC6SLX9T-FTG256, allowing for a fail-safe mechanism in case of reconfiguration errors, loss of communication or any firmware bug concerning the main FPGA. In fact, whereas the Kintex-7 can be easily reprogrammed even on run-time during the experiment, the Spartan-6 is only programmed once, behaving more like an ASIC as soon as it is deployed. The choice of FPGAs has been driven by several factors, like:

- Power consumption
- Cost
- Performances
- Number of available I/Os
- Reliability
- Availability on the market

6.2.1.1 FPGA Architecture

The fundamental element that makes up the FPGA architecture is the Configurable Logic Blocks (CLB). An individual CLB consists of several logic blocks, the main one being the Look-Up Table (LUT), which stores a predefined list of logic outputs for any combination of inputs; LUTs with four to six input bits are the most common. Since LUTs are implemented using SRAM, the encoded logic function can be reprogrammed by rewriting the content of the SRAM. Other typical logic blocks are multiplexers, full adders and Flip-Flop (FF). Surrounding the CLB, a system of programmable interconnects routes the signals according to the user configuration. The chip interfaces with the external world through I/O Block (IOB). The fabric embed other useful resources such as dedicated on-chip memory, called Block RAM (BRAM) and Digital Signal Processing (DSP) that the designer may or may not use for their application. All the elements of the FPGA can be used concurrently, providing immense parallelism.

In Fig. 6.3 an example of a basic FPGA architecture is shown.

The Kintex-7 family is built on a mature 28 nm process technology and provides leading integration capabilities and performances at relatively low-cost. The available user General Purpose I/O (GPIO)

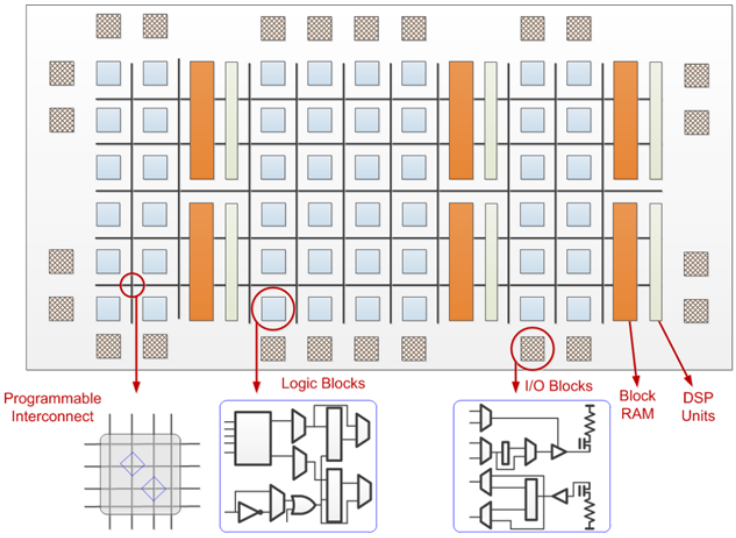

Figure 6.3: The basic architecture of an FPGA.

	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices	BRAM Blocks			Clock Management Tile (CMT)s	GTXs	Total I/O Banks	Max User I/O
		Slices	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)				
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	16	10	500
XC6SLX9	9,152	1,430	90	16	32	NA	576	2	NA	4	200

Table 6.1: GCU's FPGAs Feature Summary [72, 73].

provided by the FFG900 package are 350 High Range (HR) pins and 125 High Performance (HP) pins, enough to satisfy the requirements of the on-board peripherals. A summary on the internal resources available on both FPGAs is present on Table 6.1.

6.2.2 Analog to Digital Unit

The ADU (Fig. 6.4) represents a standalone, castellated-edge connected, custom component on the GCU board dedicated to the task of digitization of the analog PMT waveform. The ADU board has been developed in China by a joint collaboration of the IHEP and Tsinghua university, both in Beijing, China. Since three PMTs are connected to a single GCU, three ADUs are present on board.

A single ADU receives the input charge from the PMT, converts it into a voltage, digitizes the waveform and sends it to the FPGA for further processing. Before reaching the ADU's input, the signal is splitted from the HV thanks to so-called "splitter board", mounted on top of the GCU inside the UWB.

In Fig. 6.5, a block diagram of a single ADU is shown. The Front-End Chip (FEC) provides the Analog to Digital Converter (ADC)s with two signals amplified with different gain: a low gain with a

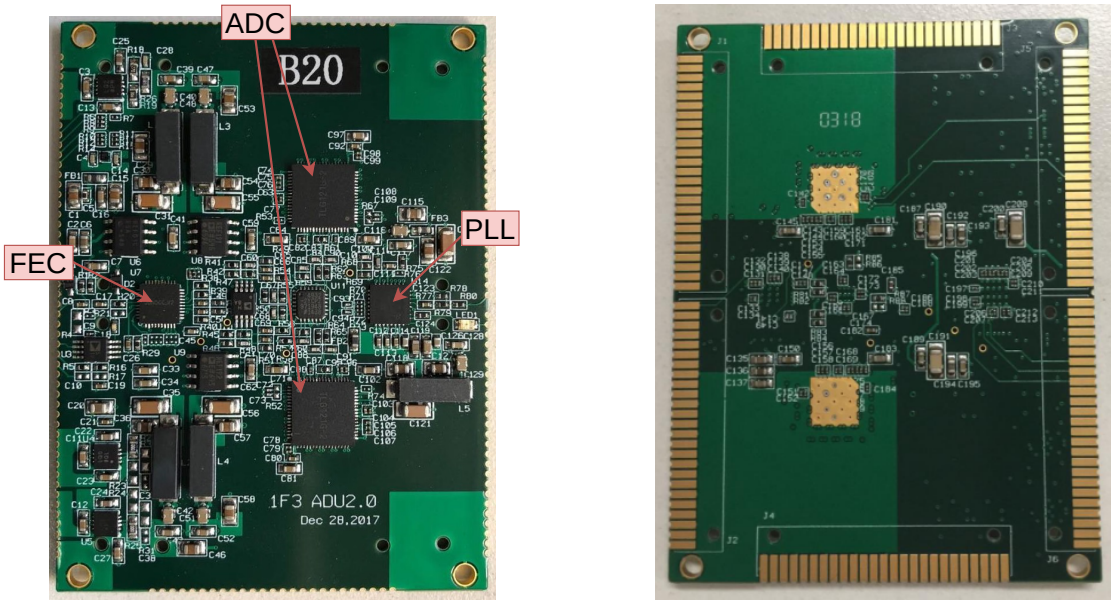

Figure 6.4: The Analog to Digital Unit board, front (left) and back (right).

dynamic range from 0 to 7.5V, equivalent to about 1000 PE, and a high gain with a reduced range from 0 to 960 mV, equivalent to 128 PE. Each ADC digitizes the analog signal at 1 Gsample/s with a nominal resolution of 14 bits. The output link uses a 14-bit DDR parallel bus, with the data synchronized to a provided 500 MHz clock. This sampling clock is generated by an external Phase-Locked Loop (PLL) mounted on the ADU. It receives the system clock of 125 MHz from the GCU and provides a low jitter (100 fs Root Mean Square (RMS)) 1 GHz clock to the ADC. Peripheral circuitry of each ADU is completed with a test pulse feature, which can generate a programmable test pulse at the input of the FEC to check the status of the full electronics chain.

Since the FPGA needs to interface with the 14-bit, 1 GSps ADC data, a Serializer/Deserializer (SerDes) tile is used within the FPGA in order to cope with the data rate (1 GSps would not be

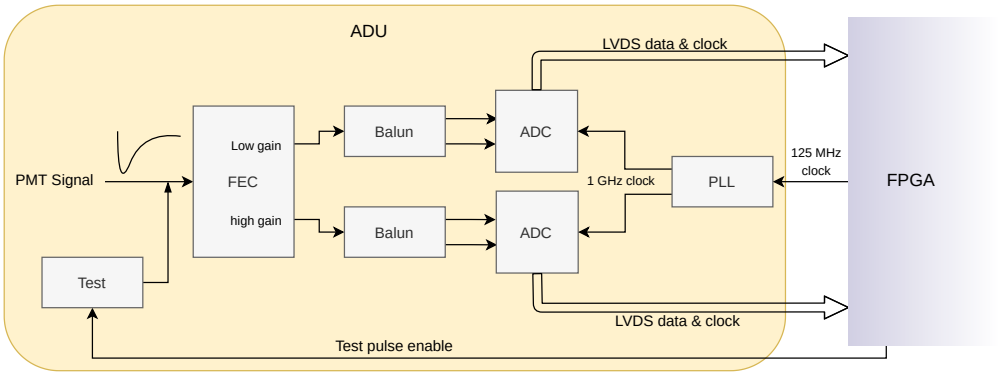

Figure 6.5: Block diagram of an ADU.

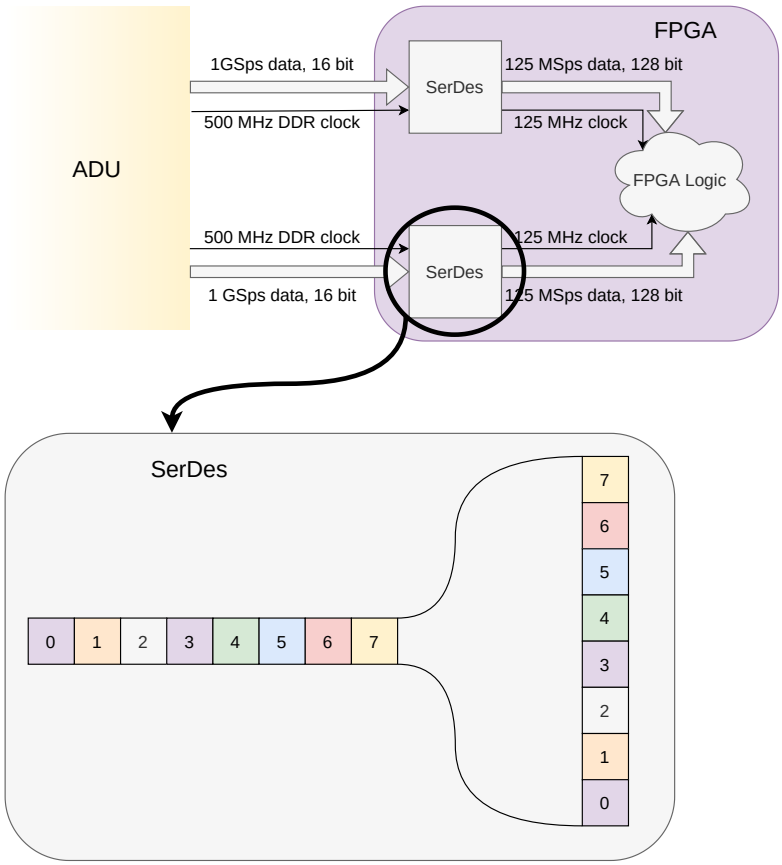

Figure 6.6: GCU - ADU interface.

sustainable by the FPGA logic). The SerDes parallelizes the incoming data 8 to 1 exploiting the 500 MHz clock provided by the ADU which features an optimal clock-data phase relationship, so 1 GSps data @ 16 bit (14 bit ADC + 2 bit for padding) are parallelized into 125 MSps data @ 128 bit. The SerDes behavior is shown in Fig. 6.6.

6.2.3 The Synchronous Link

As part of the timing and trigger system, the synchronous link provides a communication link between the FEE and the BEE with a simple, deterministic and low-latency bidirectional communication channel. The physical link is a standard Cat-5E Foiled Twisted Pairs (FTP) cable, whose twisted pairs are soldered on-board on the FEE side, and secured on the BEE with RJ-45 connectors. The length of the cables are expected to be up to 100 meters and the LVDS signals are sent to the cable and recovered on-board before reaching the FPGA thanks to a cable driver chip and adaptive cable equalizer chip, respectively. Since a single bi-directional link only uses two twisted pairs, the remaining two twisted pairs on the Cat-5E cable are kept for redundancy purposes. The link structure is shown in Fig. 6.7.

JUNO employs this link with a star topology, where the hub, consisting of a BEC above water,

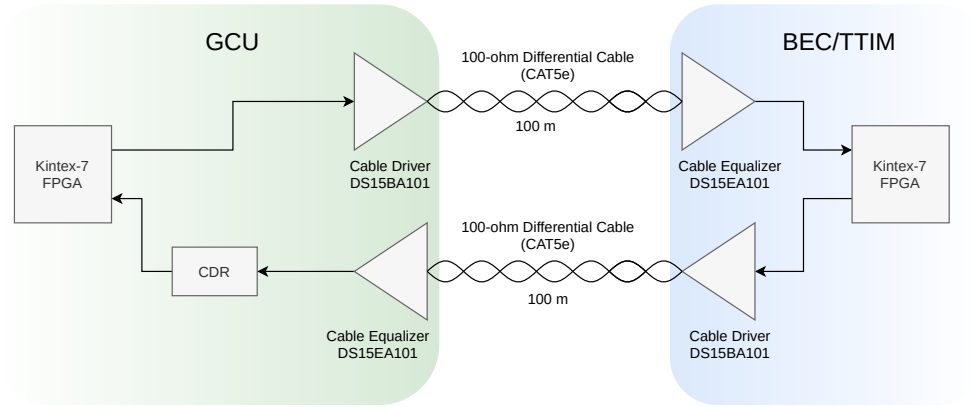

Figure 6.7: The synchronous link. The structure shown is doubled for redundancy, in order to use all four pairs of a CAT5e cable.

connects to 48 GCUs under water. The protocol used is the TTC [61].

With the same link, a digital clock signal is recovered from the BEE data stream by the FEE. Clock forwarding is essential to keep the internal, local clocks of all the GCUs synchronized to the global clock of the experiment, avoiding any drifting caused by inevitable frequency offset between different crystal oscillators.

On the GCU side, the TTC messages go through a Clock and Data Recovery (CDR) chip before reaching the Xilinx Kintex-7 FPGA. The CDR is needed to provide the embedded clock, phase aligned to the data for optimal sampling (the 180° degrees clock allows to sample at the middle of the eye). Oppositely, on the BEE side, no CDR chips are used to recover the GCU messages, and the communication must be initialized with a calibration phase, in order to ensure the correct sampling. The calibration procedure, as well as details on the TTC protocol, is described in Sec. 7.1.4.

6.2.4 The Asynchronous Data Readout and Slow Control Link

A standard commercial protocol for the data readout and slow control of the board has been a design guideline during the development of the GCU. By using standard Ethernet 1000BASE-T communication (1 Gbps) over Cat-5E UTP cables, the whole network infrastructure on site of the experiment can be easily set up using commercial equipment. Due to its great flexibility, it has been decided to use a well-known Ethernet protocol that already presents an FPGA implementation: the IPBus [60]. Developed by a CERN collaboration, the IPBus has been originally designed for controlling the trigger and readout of Micro Telecommunications Computing Architecture (TCA) (μTCA) or TCA-based hardware over Gigabit Ethernet for the Compact Muon Solenoid (CMS) experiment [74].

IPBus is a simple, Internet Protocol (IP) based control protocol. The transport level protocol which the IPBus is based on is the UDP. Mainly, UDP provides an interface for the packet sent by the internet protocol in the network layer. It does not give any message delivery guarantee or error correcting capability and is not able to resend the missing packet, thus providing a connection-less unreliable service. However UDP is very effective in some applications like real time audio video transmission,

due to its low-latency compared to other reliable services, such as Transmission Control Protocol (TCP).

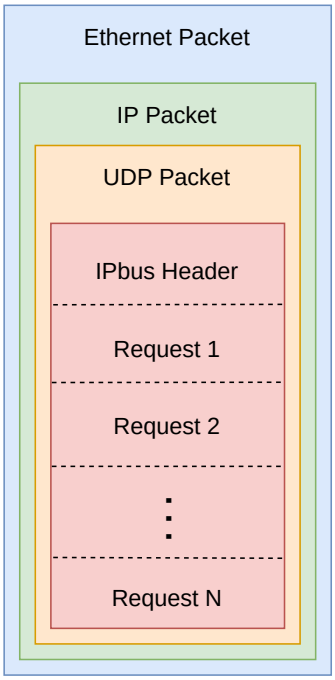

Figure 6.8: Packet format of the IPBus protocol.

To overcame limitations of UDP and provide a reliable connection, the IPBus foresees a packet header including sequential packet ID and packet type field. An IPBus packet is placed within a UDP packet which in turn is placed within an Ethernet packet, as shown in Fig. 6.8.

The IPBus suite not only includes a firmware implementation of the IPBus (more details in Sec. 7.1.1), but it also includes the ControlHub, a software application that forms a single point of access for IPBus control of each device, and the μHAL library, the Hardware Access Library (HAL) which provides an end-user C++/Python Application Programming Interface (API) for IPBus reads, writes and atomic operations.

The ControlHub is extensively used in JUNO since it allows great scalability, arbitrating simultaneous access from multiple μHAL applications to one or more IPBus nodes, and reliability, with a re-send mechanism for faulty packet transmission. Moreover, the ControlHub can accept connections from different μHAL-based application and, as well, the same machine can connect to different ControlHubs, as shown in Fig. 6.9.

Since the ControlHub is a software application, the μHAL-ControlHub communication uses TCP, which has sophisticated congestion mitigation and flow-control algorithms.

6.2.4.1 IPBus Performances

The expected performances are well documented in [60], measured in two different benchmark scenarios. Two parameters are considered:

- The latency, defined as the total round trip time taken to perform a IPBus transaction.
- The block transfer throughput, defined as the amount of data transferred or received per unit time.

The first scenario considered is the *1-to-1 block transfers*, where the block read/write operations are carried out by a single μHAL client controlling one device via ControlHub. As visible in Fig. 6.10, the median single word operation latency is approximately 250 μs. This big latency is compensated when multiple transactions are concatenated into each packet, or when large block transfers are

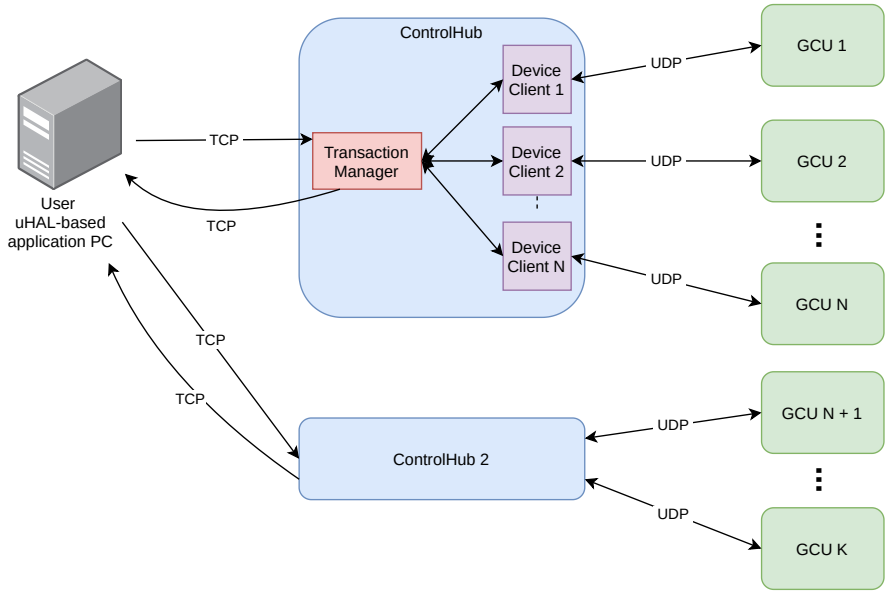

Figure 6.9: Scalability with μHAL and ControlHub.

performed, so that many packets are flying around the system at any time. By exploiting concatenation and multiple packets in flight, not only the latency is compensated but the throughput is increased by a factor of approximately 20 to 2000, depending on the transaction type, reaching more the 0.5 Gbit/s for payloads larger than 1 MByte.

A different scenario consists in *n-to-m polling*, where the performances are measured when multiple μHAL clients are polling a single word register in multiple devices via one ControlHub. The mean polling latency and the total system polling frequency are measured versus the number of devices connected; the results are shown in Fig. 6.11. Both the latency and the total polling frequency increase with the number of clients or devices in the system.

Such performances make the IPbus a suitable protocol to be adopted for data acquisition as well as slow-control, although its *pull* mechanism for data acquisition compared to the usual *push* mechanism normally adopted in DAQ systems requires some extra logic in the FPGA in order to avoid any drop in performances.

6.2.5 HV Unit and PMT Interfaces

Coupled together with the GCU inside the UWB are three custom HV unit, developed by our colleagues from the JINR in Dubna, Russia, whose task is to provide HV to the PMTs from the 24 DC supply voltage. The HV Unit (HVU) board, without its enclosure, is shown in Fig. 6.12. The module is equipped with an embedded micro-controller to monitor the operations and for configuration, interfacing with the main FPGA of the GCU through the RS-485 standard, employing optocouplers for isolation purposes. Some specifications of the HV unit can be found in Tab 6.2. The modules are plugged in a so called "Splitter Board", whose function is to decouple the HV from the analog PMT signal, sent to the ADUs

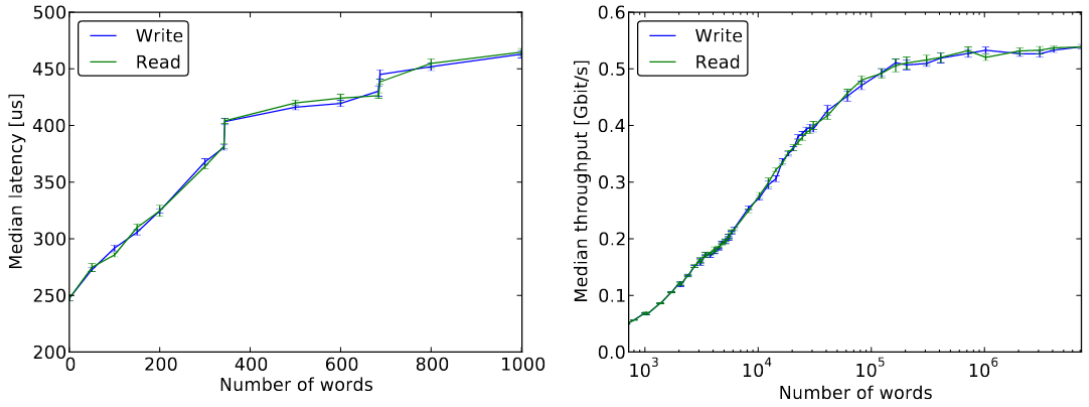

Figure 6.10: The median read/write latency and throughput as a function of depth, for one software client controlling one IPBus device, via the ControlHub [60].

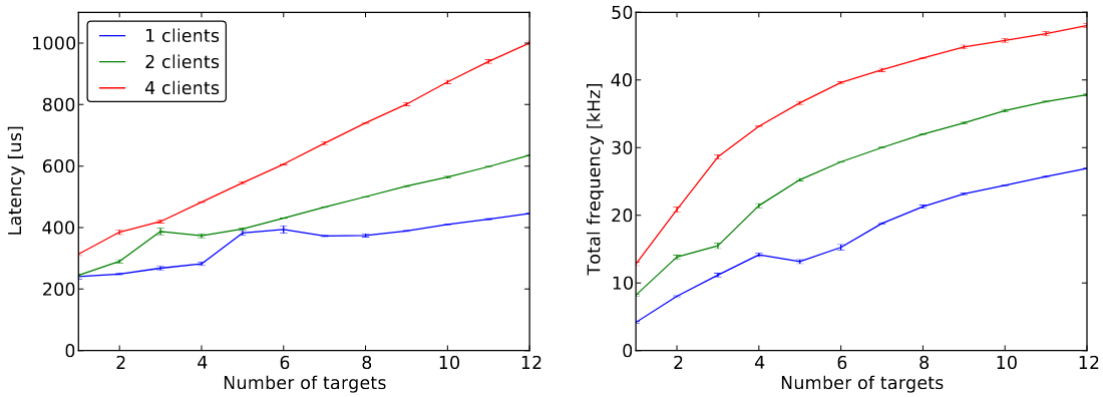

Figure 6.11: The latency and total system polling frequency for n clients each simultaneously polling a register in one of the m targets [60].

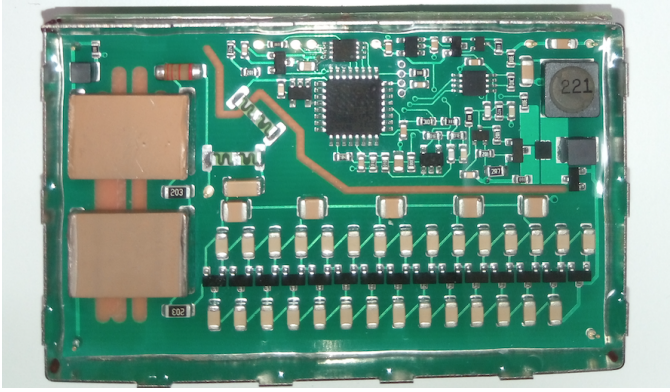

Figure 6.12: The board of a single high voltage unit without the metal enclosure.

HV range	Minimum voltage step	Ripple	HV long term stability	Temperature coefficient	Maximum output current
800 V - 3000 V	∼0.5 V	10 mVptp	0.05%	100 ppm/°C	300 μA

Table 6.2: Parameters of the high voltage unit.

for digitization.

6.2.6 Other On-board Peripherals

- **DDR3 Memory**

  As mentioned in Sec. 4.1.1, in case the event rate suddenly increases in the detector, normal readout operations through IPBus are not able to handle all the data that is required to be sent to the DAQ. Therefore, a dedicated 2 GByte DDR3 Synchronous Dynamic RAM (SDRAM) module has been added to the GCU. The memory is sufficient to store up to about 1 second of continuous data, 0.3 seconds per channel. This allows to cope with a sudden rate increase of events, e.g. a supernova explosion, and readout all the data once the event rate return to a normal level.

- **Flash Memory and EEPROM**

  The GCU is equipped with two 256 Mbit flash memory, connected one to each FPGA, and a 2 Kbit Electrically Erasable PROM (EEPROM). The smaller EEPROM memory is used to store network parameters, in particular the Media Access Control (MAC) address of both the Spartan-6 and Kintex-7. The content of the EEPROM can be accessed and modified via IPBus. The flash memories are used to store the synthesized bitstream, to automatically configure the FPGA after a power cycle. While the Xilinx Kintex-7 flash memory is foreseen to be always possible to re-configure, even “run-time”, the one connected to the Xilinx Spartan-6 should be programmed and fixed during the GCU production phase, thus the reason why the extra EEPROM memory is employed, rather than saving the MAC address on a specific address of the Spartan-6 flash memory.

- **Clock Jitter Cleaner**

  In order to improve the sampling performances of the ADCs, the clock sent to the ADUs must feature extremely low jitter characteristics [75]. For this reason, the GCU employs a jitter attenuation chip, which is capable of providing ultra-low jitter clock signals of 90 fs RMS.

  The whole clock path is illustrated in Fig. 6.13: The global clock sent by the BEC through the synchronous link is first retrieved by two FPGA’s PLL, the first set as a jitter cleaner, while the second is needed to retrieve the 125 MHz (among others) to provide to the ADUs. Before sending the clock to the ADUs, it goes through the ultra-low jitter cleaner external chip, which sends back to the FPGA the cleaned clock which is immediately forwarded to the ADC for sampling.

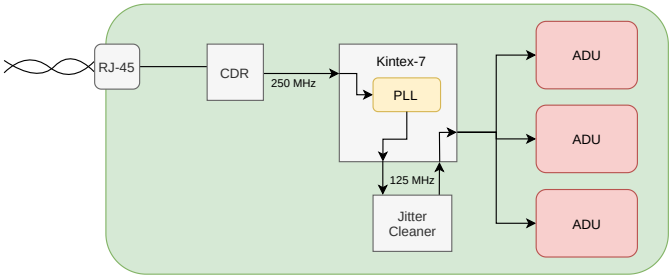

Figure 6.13: ADU's 125 MHz clock path.

- **Ethernet Switch**

  As shown in Fig. 6.2, the Ethernet switch is employed in the GCU so both the Xilinx Kintex-7 FPGA and the Xilinx Spartan-6 FPGA can connect to the network through the single Cat-5E Ethernet link. The employed chip is a 5-port automotive Ethernet switch, therefore characterized by an high reliability. The three ports that are used in the GCU design are connected to

  1. The Xilinx Kintex-7 FPGA
  2. The Xilinx Spartan-6 FPGA
  3. A Gigabit Ethernet physical layer transceiver that interfaces directly with the twister pairs of the Cat-5E cable through an external transformer.

  The switch is highly configurable, so at the start-up of the GCU an automatic configuration is needed for the switch to operate and for the GCU to be connected to the network.

7

GCU Firmware Implementation

FPGA firmware developing is a crucial step to deliver an experiment-ready front-end readout board. The FPGA is in fact the central, intelligent component that manages all the GCU peripherals, the communication links and the PMT's waveforms data processing through logic operations. A major part of my PhD program has been dedicated to the GCU's firmware development, starting from a custom pulse-shape processing technique for trigger requests generation. After that, the focus moved to the communication links, designing and implementing in FPGA the synchronous link protocol, and to the data paths, developing the *DDR readout* mentioned in Sec. 4.1.1. A comprehensive overview of the firmware is detailed in the following sections.

7.1 Kintex-7 RTL Design Overview

An overview of the Xilinx Kintex-7 hierarchical RTL design is given in Fig. 7.1. The primary tasks of the FPGA are the following:

- An interface with the six ADCs on-board. This interface is provided by the ADU blocks.
- Before sending the data packets upstream, the digital information from the PMTs needs to be stored and analyzed. The *Network Interface* sub-modules not only equip the FPGA with the IPBus protocol, but they also provide the full data path for the three ADUs data.
- The timing and trigger system of the GCU, which is implemented by the *Synchronous link* module.

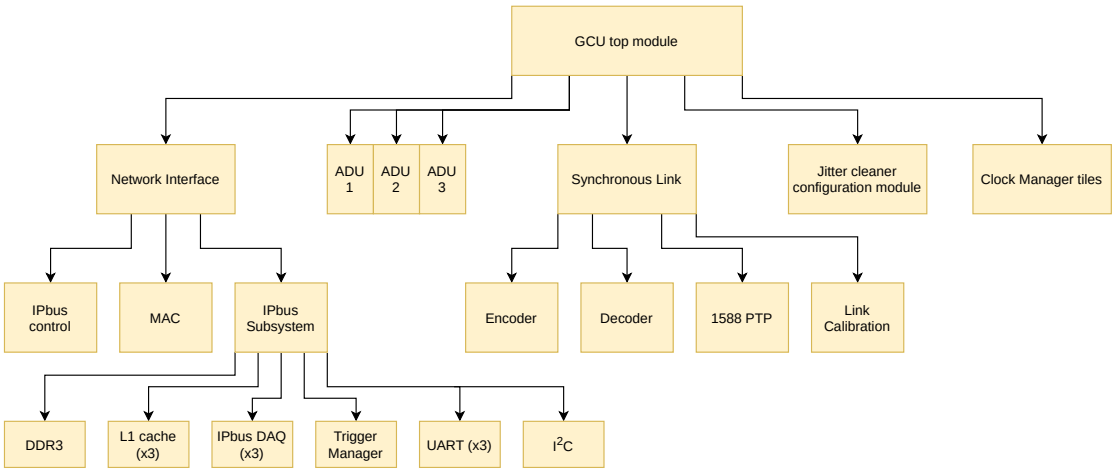

Figure 7.1: Overview of the Xilinx Kintex-7 Register-Transfer Level (RTL) design.

- The clock recovery system is equipped by means of the *Clock management tiles*, using a Mixed Mode Clock Manager (MMCM)/PLL.

- The necessary SPI configuration of the jitter cleaner chip on-board.

While most of the RTL design is based on generic Very High Speed Integrated Circuit Program (VHSIC) Hardware Description Language (HDL) (VHDL) code, some proprietary cores are used to hide to the end-user the complexity of low-level protocols. These are generated exploiting the Xilinx CORE Generator system that provides access to highly parameterized IPC, such as the Memory Interface Generator (MIG) IPC: a combined controller and physical layer interfacing the FPGA user design with DDR3 devices.

7.1.1 IPBus Firmware

The IPBus firmware [60] is an FPGA core included in the IPBus suite which provides different modules that interpret the IPBus protocol within FPGAs. The structure of the IPBus project is shown in Fig. 7.2.

The firmware is modular, with a core protocol decoder and bus master that controls the interface to the IPBus slaves. The UDP engine implements the echo request/reply semantics from Internet Control Message Protocol (ICMP), Address Resolution Protocol (ARP) for resolving IP addresses into MAC addresses and, optionally, Reverse ARP (RARP) for an IP address request at start-up.

While most of the design can be used as is, the end-user is required to add IPBus slaves according to his application. Each slave contains a set of registers that can be written and read by IPBus transactions. Extensible Markup Language (XML) files are used to specify the addresses, sub-addresses and masks of the slaves registers, and through the use of a dedicated script, a VHDL address decoder file is automatically generated and used by the bus fabric which arranges for a slave to see activity on the bus when it's being addressed. Some of the IPBus slaves instantiated in the design are:

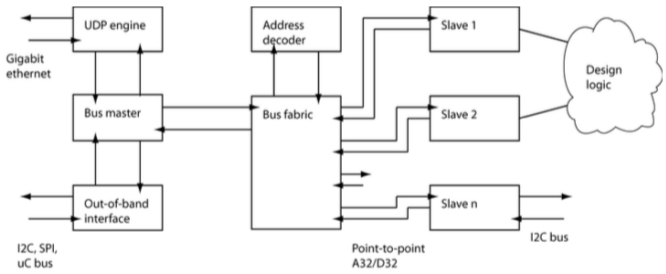

Figure 7.2: IPBus block diagram structure. Taken from [76]

- Trigger manager: the user has the possibility to change the trigger scheme at run-time, switching among the global trigger scheme, the self trigger scheme or to use the external trigger, from which the user is enabled to send asynchronous IPBus triggers to a specific channel.
- L1-cache: as described in the following section, the L1-cache is a circular buffer continuously written with raw digitized data coming from the ADUs. As soon as a trigger timestamp arrives, a selected window of data is extracted and sent to the DAQ. The IPBus slave interface of the L1-cache defines some DAQ parameters such as the length of the data window and the pre-trigger time (i.e., the time to start extracting the data before the incoming timestamp).
- IPBus DAQ: the PMT data window extracted from the L1-cache is sent to the DAQ server with dedicated IPBus slave interface. In order to check and control the readout process some extra information can also be provided to the server.
- Universal Asynchronous Receiver-Transmitter (UART): this slave serves as an IPBus-UART bridge, to communicate with the HVUs.
- Inter-Integrated Circuit (I^2C): an IPBus-I^2C bridge to read the temperature sensor chip.
- DDR3: similarly to the IPBus DAQ, this slave provides an interface for the DDR3 memory readout. While the memory is being read, data writing is blocked and will resume when the whole memory is empty.

7.1.2 Digital Data Flow

In this section the digital data flow is described, from the digitization of the PMT signal to the network readout. In Fig 7.3, the data path of a single channel is shown.

The ADU interface provides the FPGA with a 14 bit parallel bus synchronous to its sampling clock of 500 MHz DDR. The SerDes tile in the FPGA's IOB groups together 8 ADC words, padding to 128 bit, synchronizing them to a system clock of 125 MHz. The data is then splitted three ways:

- **Default path**: Data is continuously stored in a circular buffer, the *L1-cache*. This memory, internal to the FPGA, has a parameterized size. Currently it is able to store 32 μs of raw data

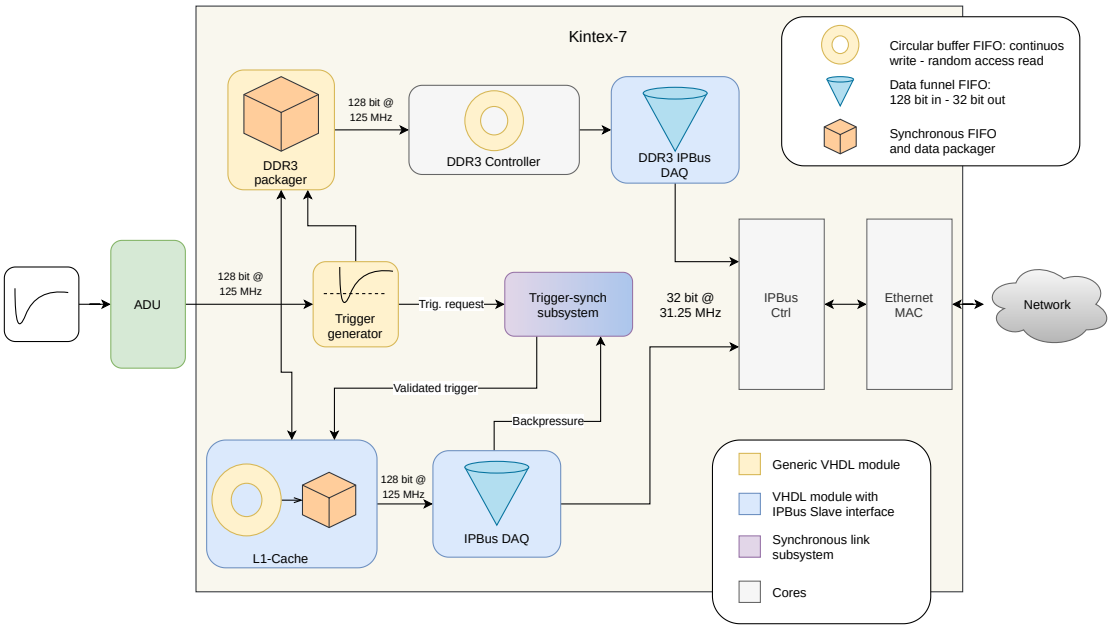

Figure 7.3: Data flow block diagram.

per channel, which is more than enough to accommodate the needed time for a global trigger validation to be issued by the CTU. As soon as a timestamped trigger arrives, a chunk of time-related data is extracted, packetized with an header and trailer that contains some metadata, and sent to the DAQ module.

The IPBus DAQ module presents a "funnel" asynchronous First In, First Out (FIFO): the data enters in blocks of 128 bit synchronous to a clock of 125 MHz and exits with a width of 32 bit at a frequency of 31.25 MHz. Clock-Domain Crossing (CDC) and data format change is necessary to comply with the IPBus slave interface for the readout. The module also includes some logic and control signals to ensure a correct and efficient transmission.

- **Complementary path**: The *high event-rate complementary path* is needed to accommodate scenarios where the trigger rate increases enormously, for witch the default path is not able to cope with, ending up losing data. This path exploits the 2 GBytes of DDR3 present on-board, which is more than enough to lodge all the interesting events originated by these "special events" (SN explosions).

  The first module is the DDR3 packager that encapsulates the interesting event with a header and a trailer. Since by design the DDR3 should be filled only in self triggering mode, no L1-cache is needed for this path. After being packetized, the data is then sent to the DDR3 controller which addresses the memory as a circular buffer. If an increase of event-rate is detected and the DDR3 content is requested by the DAQ, the writing operations are blocked and the DDR3 is emptied out by the DDR3 DAQ module. Once the whole content is read, the writing restarts automatically. Due to the *half-duplex* nature of the *complementary path*, the *default path* is

preferred in order to avoid any loss of data.

- **Trigger path**: Data are analyzed against a trigger algorithm in order to generate the primitive trigger requests. The choice of the triggering algorithm is not yet fixed, but a simple leading-edge trigger has proven to be successful in the discrimination of single PE pulses, thanks to the good performances in Signal to Noise Ratio (SNR) of the ADCs/ADUs.

  These trigger requests are forwarded both to the synchronous link and sent to the BEE for candidate validation, and to the DDR3 packager module, since only the self-triggering option is foreseen. The trigger subsystem also contains an IPBus slave, needed for the user to set the triggering scheme: global trigger, self trigger or external IPBus trigger, and the trigger threshold level. In both cases, a timestamp is sent to the L1-cache module, which is either generated locally when in self or external trigger, or retrieved from the BEE, when in global trigger mode.

  In order to avoid data corruption, when the internal FIFO reaches a certain level of occupancy, a back-pressure flag is issued from the IPBus DAQ to the trigger subsystem, so that no more triggers are issued until the FIFO goes back to an operational state.

All the IPBus transactions go through the *IPBUs Ctrl* core, that provides the interface for the slaves, and encapsulates the payload data into UDP network compliant packets. These packets are then sent to the *Ethernet MAC* module which converts the data into Reduced Gigabit Media-Independent Interface (RGMII) format to interface with the Ethernet physical layer chip.

Of the three data paths described, I have personally been responsible for designing and testing the *complementary DDR path*. The FPGA implementation for the *QT readout* described in Sec. 4.1.1 is still under development.

7.1.3 Trigger Manager

The *trigger manager* module controls both the trigger source and the trigger path for each GCU through IPBus commands. As shown in Fig. 7.4, three different control signals can be issued by the user to manage the trigger:

- **IPBus test pulse trigger**: Even though this control signal does not actually interface with the trigger manager module, it is still used to control the trigger source. In fact, the IPBus test pulse trigger allows to interact with the test pulse circuit of the ADU and generate a hardware-defined PMT-like pulse. This pulse is digitized and sent to the FPGA alongside the real PMT pulses.

- **IPBus trigger source control**: As the name suggests, this control signal allows the user to choose the source of the primitive trigger; in particular the trigger sources consists of

  – the default threshold trigger that analyzes the raw ADC waveforms.

  – an external IPBus trigger, uncorrelated to any waveform information.

  Both of these trigger sources generates a digital active-high 1-bit pulse.

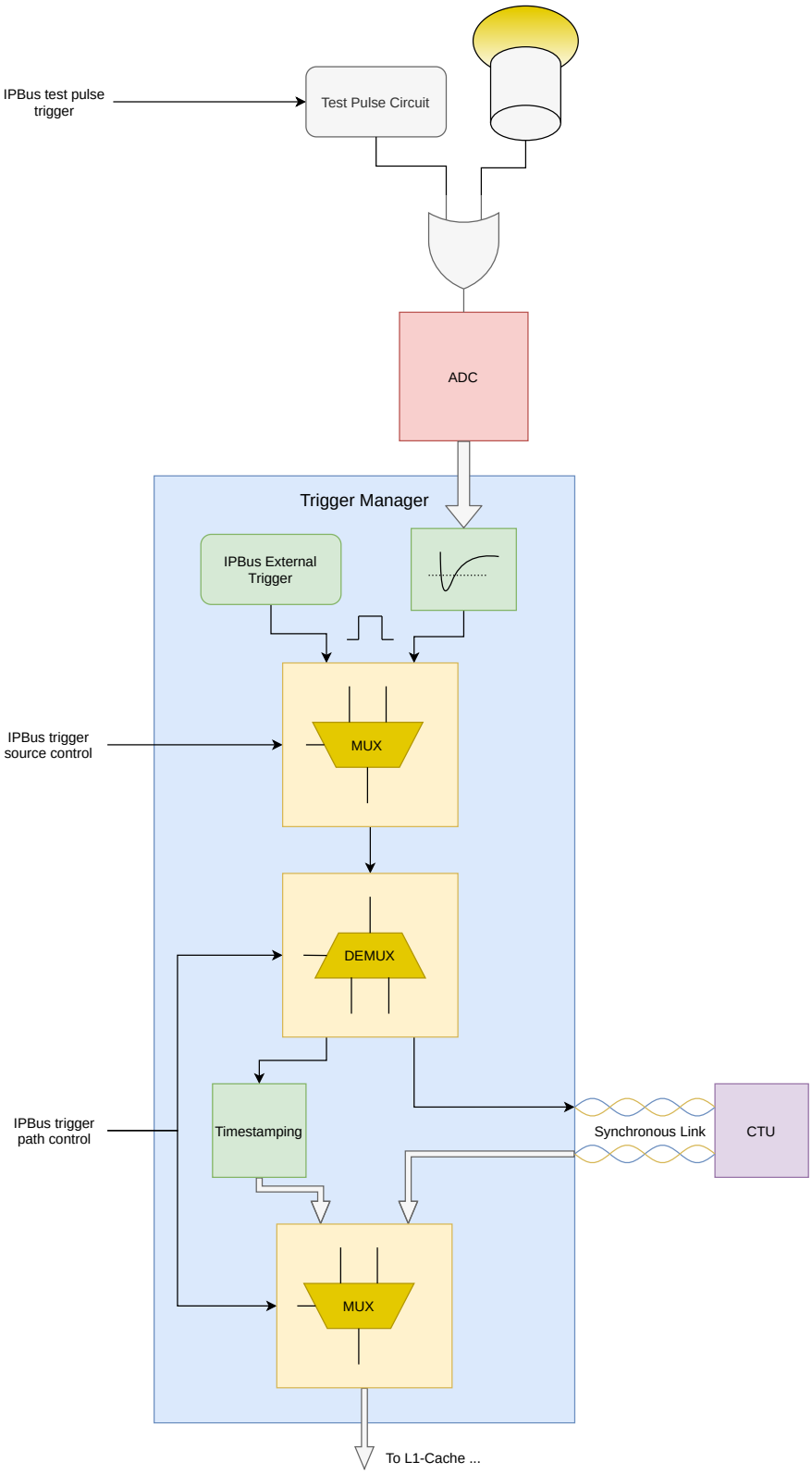

Figure 7.4: Overview of the trigger manager. Solid lines represent 1-bit signals, while wide arrows represent multi-bit vectors.

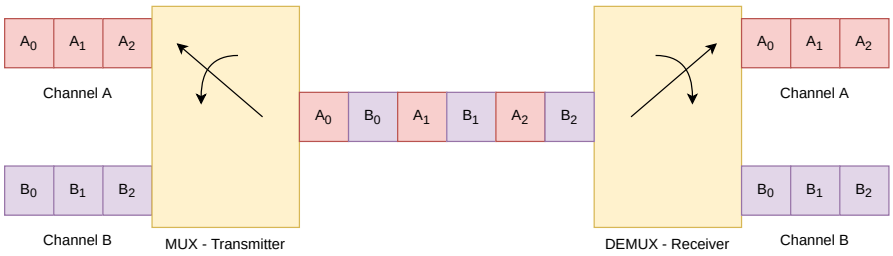

Figure 7.5: Working principle of time division multiplexing. Two separate channels are incorporated in a single link.

- **IPBus trigger path control**: Through this register the user is enabled to choose and switch between the self-trigger scheme and the global trigger scheme. If the self-trigger is chosen, the local trigger requests are immediately timestamped; on the other hand, with the global trigger scheme the timestamp is issued only upon the arrival of the global trigger validation from the BEE. In both cases, the timestamp will be sent to the L1-cache to extract the correlated data window to send to the DAQ

7.1.4 The Synchronous Link

The synchronous link protocol is based on the TTC's system concept [61]. The TTC embeds in a communication medium two communication channels through Time Division Multiplexed (TDM). The concept of TDM is shown in Fig. 7.5. Channel *A* consists in a "single-bit frame" representing local trigger request from the GCU to the BEC/TTIM system. The bit remains high (logical "1") as long as one of the three channels waveforms exceeds the user-defined threshold value. Channel *B* on the other hand, can either be broadcast commands, to distribute messages to all the TTC receivers, or individually addressed commands/data, containing address and sub-address fields to address individual systems. Both these commands are transmitted over the synchronous link using a frame format defined by the protocol. Channel *B* is also Hamming encoded for transmission reliability, with the capability of double bit error detection and single bit error correction.

The link has been initially tested with a data rate of 125 Mbps, but a line rate of 250 Mbps has also been successfully implemented [62]. The physical layer of the synchronous messages are Biphase Mark Coded (BMC) (Fig. 7.6), which is a 1B/2B encoding scheme, therefore reducing the actual throughput to half of the channel capacity, but allowing the link to embed the clock within the data for a very efficient remote clock recovery.

The structure of the broadcast and individually-addressed frames are schematically represented in Tab. 7.1 and 7.2, respectively, with a header bit (FMT) that indicates the type (logical "0" for broadcast frames and logical "1" for individually-addressed frames) and start (logical "0") and stop (logical "1") bits to define the boundaries. The address space selection bit (E) is used by the TTC protocol to instruct the addressed receiver either to execute an internal operation or to make the received command externally available, and it is not used in JUNO.

START	FMT	CMD/DATA <7:0>	CHCK <4:0>	STOP
0	0	dddddddd	eeeee	1

Table 7.1: Structure of the broadcast command frame.

START	FMT	TTCrx ADDR <13:0>	E	1	SUBADDR <7:0>	DATA <7:0>	CHCK <6:0>	STOP
0	1	ttttttttttttt	i	1	ssssssss	dddddddd	eeeeeee	1

Table 7.2: Structure of the individually-addressed command frame [77].

7.1.4.1 Clock Forwarding

As mentioned in the previous section and in Sec. 6.2.3, the JUNO timing system foresees the global clock signal to be distributed to the FEE nodes as encoded information in the TTC messages, through a BMC. The local clock in any GCU is a copy of the global clock recovered from the data stream generated by the master (the BEE). The clock recovery is based on a CDR IC that extracts the timing information from data transitions, whose minimum density must be guaranteed by a suitable protocol. This makes the slave immune to medium and long term frequency drifts that manifest as a linearly increasing phase difference and a cumulative error on the local time count [62].

7.1.4.2 PTP Digital Design Overview

A simplified overview of the digital circuit that implements the offset correction mechanism described in Sec. 4.3, is given in Fig. 7.7. This timing system requires the availability of a sender and at least one receiver and a full duplex communication channel among them. The choice of the communication medium bounds the maximum admissible distances between master and slave nodes. In JUNO, the proposed design is based on Cat-5E FTP cables, therefore setting the maximum distance to about 100 m, given the support of the cable driver-receiver couples employed by the synchronous link. The expected data rate of 250 Mbps is well in the range of the HR general purpose I/O pin capability of the chosen FPGA, thus freeing the design of the communication physical layer from the usage of dedicated

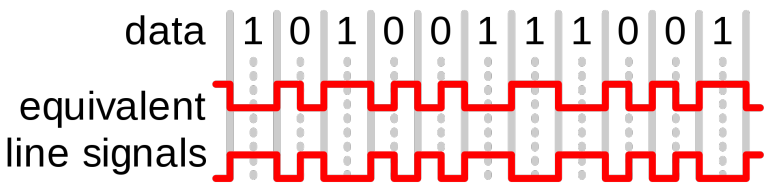

Figure 7.6: An example of BMC: Gray vertical lines, full and dotted, represent the two clock ticks per bit period. In the shown variant of the encoding, 0 is represented by a transition and 1 is represented by no transition. The two line signals shown differ in their polarity; the one occurring on the line depends on the preceding line state.

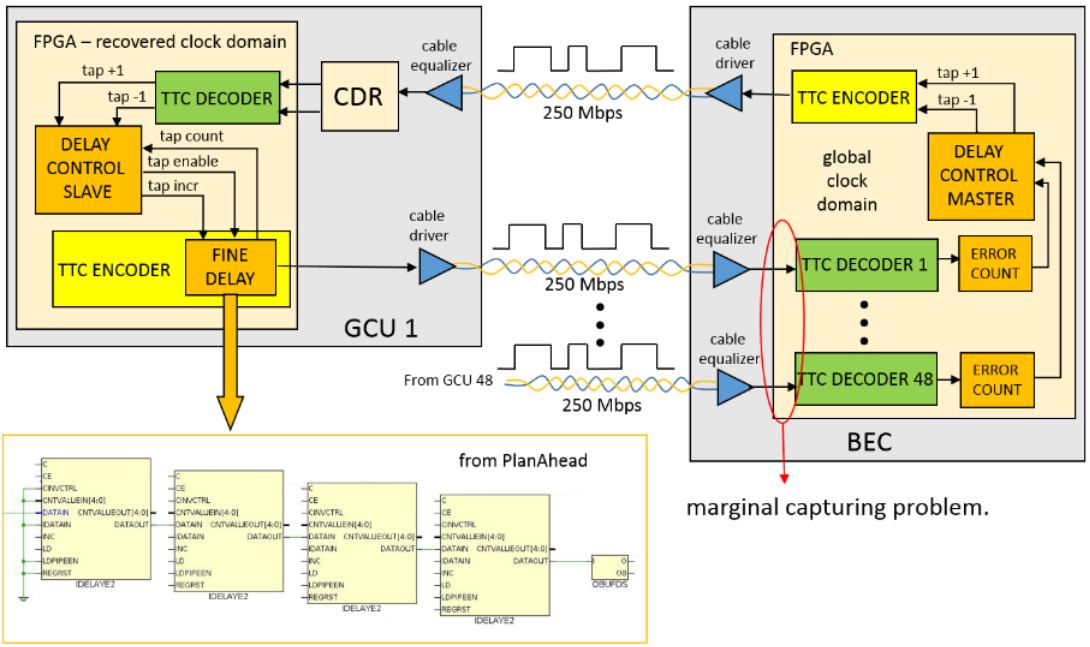

Figure 7.7: Digital implementation of the serial data stream synchronization [62].

transceivers, with a consequent reduction of power consumption. While the global clock is provided to the BEE through the WR network, the same clock is forwarded to the FEE via synchronous link and recovered through the CDR IC. The synchronous messages system has no handshaking mechanism, therefore the PTP master and slave cores implement a watchdog that takes back the Finite State Machine (FSM) to idle state in case that a message is not correctly delivered and the offset correction procedure stalls.

The PTP master scheduler follows a round-robin algorithm to address the synchronization procedure to the timing receiver nodes sequentially. The synchronization cycle is periodical.

7.1.4.3 Link Calibration

To establish a reliable communication over this synchronous link, the problem of marginal capturing has to be addressed. Marginal capturing happens when data is captured without the sufficient setup and hold time in the receiver, thus leading not only to metastability problems [78], but more importantly, to erroneous data sampling.

As shown in Fig. 7.7, in the FEE the CDR chip automatically locks on the input data stream and tracks the phase of the input data in order to shift the recovered clock to the best sampling point minimizing the possibility of having the marginal capturing phenomenon.

In the BEC side, the synchronous link system consists of 96 incoming data streams (48 synchronous link, doubled for redundancy); using a CDR chip for each link generating 96 different clock domains is not feasible. Techniques normally adopted to minimize the probability of metastability in digital

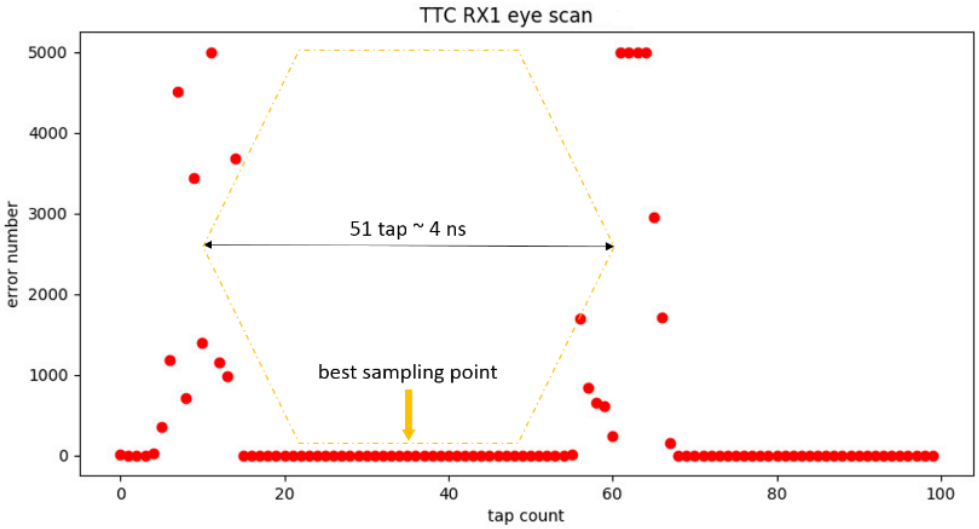

Figure 7.8: Bathtub plot of the LVDS serial data stream capturing [62].

designs, like synchronization registers, are not a possible solution when the important information lies in a sequence of bits. The issue has been addressed using a cascade of four programmable fine delay primitives, IDELAYE2 (ODELAYE2 primitives cannot be cascaded because their output drives the corresponding IOB and cannot be routed to the internal FPGA logic). Each IDELAYE2 primitive is a 31-tap wraparound selectable delay with a calibrated tap resolution of 78 ps, which is the largest tap delay the hardware can give. This fine delay block is placed at the output of the synchronous link encoder in any front-end board, and its tap count is remotely incremented/decremented from the master calibration procedure running in the back-end. The data stream input to the backend FPGA is delayed incrementally in steps and the data frame error count versus the tap count is measured. The information about the eye opening thus obtained is used to set the best sampling point as illustrated in Fig. 7.8. The error count is retrieved thanks to Hamming code error detection capability. The clock synchronization procedure can not start until this calibration is completed and the channel is error free. Establishing a reliable bidirectional communication between the master and all the timing receiver nodes is essential in a 20'012 channels setup.

7.1.5 Pulse-Shape Processing for Trigger Requests

As explained in Sec. 4, the JUNO detector and electronics require an evaluation of single PE signals from the PMTs; in these conditions, the signal amplitude is comparable to the electronics background noise. Therefore, I have developed a dedicated trigger algorithm, aiming for an improvement in single PE pulses detection and trigger efficiency.

The technique, based on pulse-shape elaboration, is often used for X-Ray or germanium detectors signals to retrieve the energy from the signal pulses [79], and it has been adapted to cope with the fast JUNO PMTs pulses. The full paper concerning this development can be found at [80].

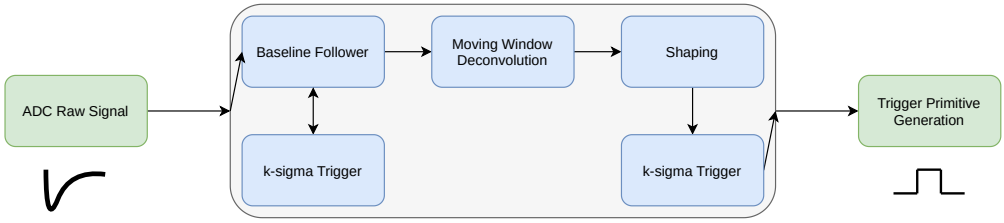

Figure 7.9: Overview of the online, devonvolution based, pulse-shape analysis.

Fig. 7.9 is an overview of the pulse-shape-based trigger algorithm, consisting in a 4-module pipeline. Initially the algorithm dynamically tracks the baseline value through the *baseline follower* module, avoiding possible bias caused by PMT pulses thanks to the *k-sigma trigger* module. After the baseline subtraction, the resulting waveform undergoes a *Moving Window Deconvolution (MWD)*, which extracts the energy value of the pulses, returning it through a step function amplitude. After a low pass filtering performed by the *shaping* module, a second *k-sigma trigger* module delivers the final primitive trigger. I have implemented the algorithm in the GCUs Kintex 7 FPGA, elaborating the PMTs 14 bit, 1 GSps digitized data stream coming from the ADU, synchronized to 500 MHz clock DDR. To cope with the FPGA's frequency limitations, only 1 out of 4 samples are taken into consideration, filtering the stream with a low-pass polyphase decimator filter [81] to avoid aliasing issues.

7.1.5.1 Baseline Follower and K-σ Trigger

The *baseline follower* module has been developed to average out the high frequency amplitude noise and follow the low frequency baseline modulation. The dynamical quantities evaluated for every sampling period are:

$$B(t_i) = B(t_{i-1}) + \frac{1}{\tau_b}[R(t_i) - B(t_{i-1})] \tag{7.1}$$

$$\sigma(t_i) = \sigma(t_{i-1}) + \frac{1}{\tau_\sigma}[D(t_i) - \sigma(t_{i-1})] \tag{7.2}$$

where t_i is the discrete sampling time, $R(t_i)$ is the raw signal, $B(t_i)$ the baseline, $\sigma(t_i)$ the standard deviation of the noise and $D(t_i)$ the absolute value of the deviation from the baseline of the raw signal: $D(t_i) = |R(t_i) - B(t_i)|$. τ_b and τ_σ, expressed in nano-seconds, are time constants that reflect the dynamics of the evaluated quantities.

To correctly evaluate the baseline of the raw stream, any pulse must be recognized in order to freeze the baseline computation until its end. This job is carried out by the *k-σ trigger* module which dynamically evaluates the deviation of $D(t_i)$ from the baseline in units of $\sigma(t_i)$.

7.1.5.2 Moving Window Deconvolution

One of the main advantages of the adopted trigger scheme is to be able to discriminate noise spikes from real PMT pulses, even in the case where both of them exceed a certain threshold. The MWD algorithm [82] is used to exploit the characteristic fast rising edge and a simil-exponential decay of the PMT signal to improve the detection efficiency.

From an exponential decay signal, starting at the time $t_0 = 0$, we can model its amplitude at the time t by the expression

$$A(t) = \begin{cases} N \exp\left(-\frac{t}{\tau}\right) & t \geq 0 \\ 0 & t < 0 \end{cases} \tag{7.3}$$

where τ is the decay constant and N the maximum amplitude. We can now define a new function $U(t_k)$ with $t_k > 0$, expressed in terms of the initial amplitude N as

$$\begin{aligned} U(t_k) &= A(t_k) + N - A(t_k) \\ &= A(t_k) + N\left(1 - \exp\left(\frac{-t_k}{\tau}\right)\right) \\ &= A(t_k) + \frac{1}{\tau}\int_0^{t_k} A(t)dt \\ &= A(t_k) + \frac{1}{\tau}\int_{-\infty}^{t_k} A(t)dt \end{aligned} \tag{7.4}$$

where the last step expanding the integral from 0 to $-\infty$ is permitted because the amplitude $A(t_k)$ is zero for $t_k < 0$. $U(t_k)$ aims to obtain an Heavyside step function multiplied by the initial amplitude of the pulse N.

Adapting the equation to our signal, it is easily provable [79] that

$$U(t_k) = x(t_k) + \frac{1}{\tau_d}\sum_{i=-\infty}^{k-1} x(t_i) \tag{7.5}$$

where $\tau_d = \tau/\Delta t$ is now expressed in units of the sampling time and $x(t_k) = B(t_k) - R(t_k)$. The MWD filter is derived from differentiating the expression in eq. 7.5

$$\begin{aligned} MWD(t_k) &= U(t_k) - U(t_{k-w}) \\ &= x(t_k) - x(t_{k-w}) + \frac{1}{\tau_d}\sum_{i=k-w}^{k-1} x(t_i) \end{aligned} \tag{7.6}$$

where w represents the width of the moving window, as well as the length of the resulting plateau. In order to apply this to a PMT pulse, the first step must consist in estimating the time constant of the exponential decay: τ. If overestimated, the step function will not present a flat top, but a positive slope instead. On the other hand, if underestimated, the flat top is replaced by a negative slope. Since the step function amplitude is correlated to the pulse's energy, a wrong estimation of τ results in a

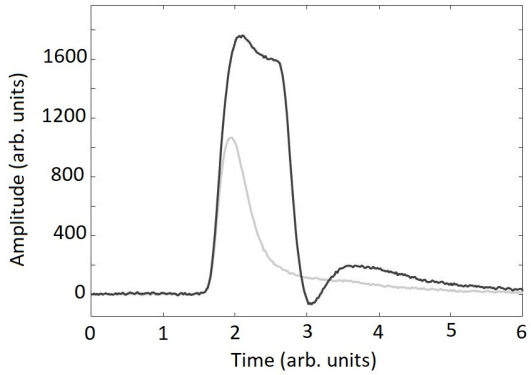

Figure 7.10: MWD module output (black line) resulting from the inverted PMT pulse (grey line).

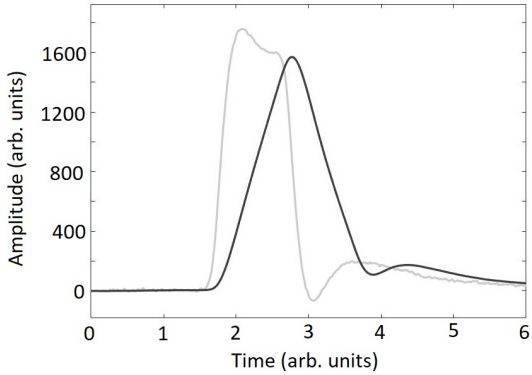

Figure 7.11: Triangular shape output (black line) generated by the Shaping module, MWD module output (grey line) as input.

wrong estimation of the energy.

7.1.5.3 Shaping Module

The goal of the *shaping module* is to average the plateau provided by the MWD to obtain a unique and well-defined value. This shaping is carried out by a simple Moving Window Average (MWA) filter. As the name suggests, the filter operates by averaging a fixed number of points from the input signal to produce one point in the output signal. This procedure is expressed by the following equation:

$$MWA(t_k) = \frac{1}{l}\sum_{j=1}^{l} MWD(t_{k-j}) \tag{7.7}$$

where $x(t_k)$, $x(t_{k-1})\dots x(t_{k-l})$ are the signal at the discrete sampled times t_k, $t_{k-1}...t_{k-l}$ respectively, $MWA(t_k)$ is the output signal at time t_k, and l is the width of the filter window, equal to the number of points in the average. Despite its simplicity, the MWA filter is optimal for a common task: reducing random noise while retaining a sharp step response.

Through this module, the user has the possibility to select between two different shapes. If l is less than w the output will be shaped as a trapeze, with a $w-l$ long flap top. Instead, if $l = w$, the shape will be the one of a triangle. The advantage of using a trapezoidal form is a greater discriminatory power because of its characteristic plateau; however, if a triangular shape is chosen, the module filtering efficiency will be maximum.

Once the module has shaped the deconvolved output, the standard deviation of the noise's high frequency component is evaluated (Eq. 7.2) in order to use a second *k-σ trigger* to provide the final trigger. An application of the algorithm to a JUNO PMT pulse is visible in Fig. 7.10, 7.11.

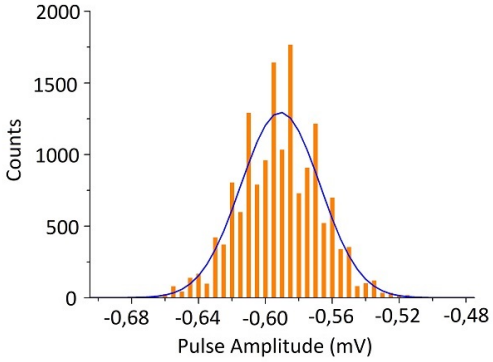

Figure 7.12: Gaussian distribution of the PMT's output pulse amplitude corresponding to a fixed LED supply voltage.

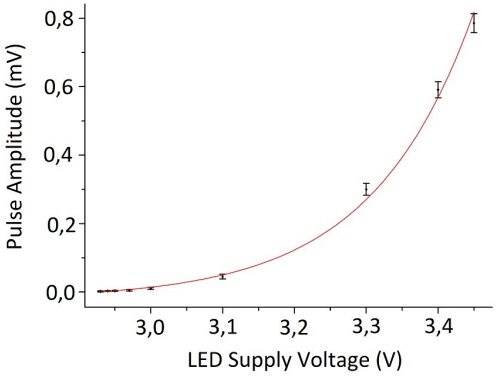

Figure 7.13: Pulse amplitude as a function of the LED supply voltage. The error bars refers to the Gaussian distribution's standard deviation.

7.1.5.4 Trigger efficiency

The proposed trigger algorithm has been tested and characterized to verify its behavior and performances once implemented in FPGA. The signal source for this test is a 20-inch Hamamatsu R12860-HQE PMT, secured inside a dark box. The signal output has been fed to the GCU, with the FPGA firmware accommodating both a simple leading edge trigger and the deconvolution-based algorithm. Inside the box, the PMT pulses originates from a Light Emitting Diode (LED), whose power is supplied by an external pulse generator. The trigger efficiency can be defined as

$$\text{Trigger Efficiency} = \text{Valid Trigger Requests}/\text{Total Trigger Requests} \tag{7.8}$$

where

- *Total trigger requests* are obtained by an unconstrained acquisition of the GCU trigger output. These trigger can be generated by the PMT dark noise, residual light penetrating into the dark-box, the LED light and electronics background noise in case of a low threshold level.
- *Valid trigger requests* are the fraction of the *total trigger requests* that overlaps with the LED pulse trigger output, supplied by the pulse generator. *Valid trigger requests* are therefore trigger requests generated only by the LED light.

Fig. 7.12, 7.13 show the relationship between the LED supply voltage and the PMT pulse amplitude. An exponential function has been fit through the data point. Finally, an efficiency scan is performed at different LED supplied voltages. The results are plotted in Fig. 7.14. As expected, as the LED supply voltage is increased, the easier it is to discriminate the PMT's pulses to the electronic's background noise and the difference on the efficiency becomes negligible. On the other hand, as the LED supply voltage decreases, the pulse's amplitude gets closer to the noise amplitude and the efficiency of the deconvolution based algorithm is greater compared to the simple leading edge trigger. The efficiency

LED Supply Voltage	MWD-MWA trigger alg.			Leading-edge trigger alg.		
V	Valid trg	Total trg	Efficiency	Valid trg	Total trg	Efficiency
2.86	4	54'096	$7 \cdot 10^{-5}$	18	26'214	$7 \cdot 10^{-4}$

Table 7.3: Dark efficiency results

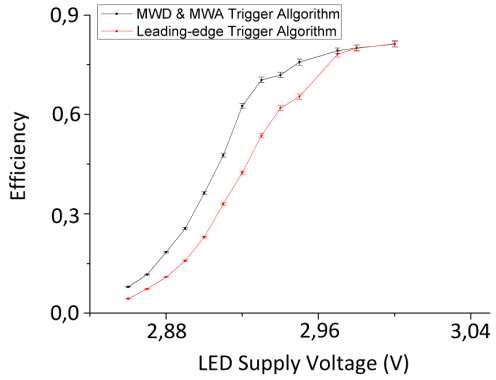

Figure 7.14: Efficiency scan for different LED supply voltages. The black line refers to the deconvolution based algorithm, while the red line refers to a leading-edge algorithm.

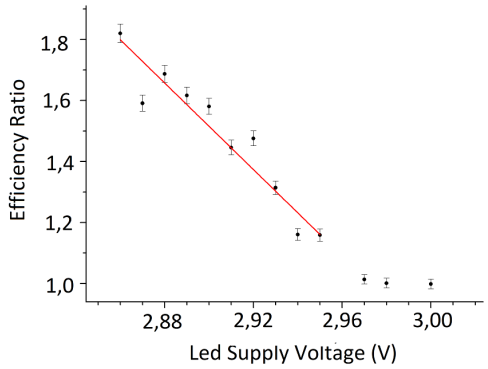

Figure 7.15: Effiency ratio scan for different LED supply voltages between the two algorithms under test.

comparison is more clear in Fig. 7.15, where the efficiency ratio is plotted. For sufficiently low LED supply voltages, the results manifest a linear relationship with a negative slope. To make sure that the *valid trigger requests* actually come from LED light, an acquisition on the lowest threshold level is run, keeping the LED off. The results are shown in Tab. 7.3, confirming that the systematic error caused by this sort of *dark efficiency* is compatible with the zero value.

The results of such test demonstrates an effective improvement in the discrimination capacity of low-amplitude signals, highlighting and efficiency improvement of a factor of two when compared to a simple leading edge trigger.

7.2 Spartan-6 RTL Design Overview

The smaller Xilinx Spartan-6 FPGA on-board plays an essential role in the overall GCU functionality and reliability. The main tasks of the Spartan-6, whose architecture is shown in Fig. 7.16, are:

- **I^{2}C IPBus slave**: The Spartan-6 is in charge of the MAC address assignment.

  The MAC address is stored in a small EEPROM memory, which can be written and read by an I^{2}C IPbus slave. The EEPROM is supposed to be written during the production phase of the board, but it's always possible to access it and change the address on-the-fly. A dedicated on-board bus

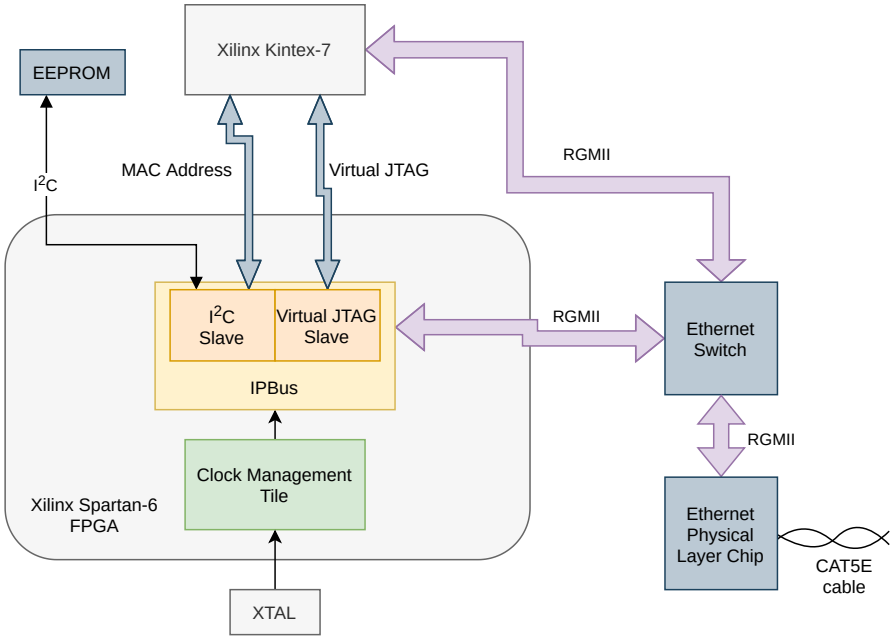

Figure 7.16: Overview of the Xilinx Spartan-6 firmware architecture.

transfers the MAC address information from the Spartan-6 to the Kintex-7 FPGA.

- **Xilinx Virtual Cable IPBus slave**: Xilinx Virtual Cable (XVC) [83] is a TCP/IP based protocol that embeds a JTAG scan protocol in a standard network transport layer.

  The XVC protocol is used by a TCP/IP client and server to transfer low level JTAG vectors from a high level application to a device. The client will connect to an XVC server application on the DAQ/Slow Control server using standard TCP/IP. Once connected, the XVC protocol defines a JTAG communication method with capabilities to perform complex functions like remote programming and debug of devices.

  As shown in Fig. 7.17, the XVC μHAL application connects via TCP/IP to the IPBus ControlHub in order to forward and receive the JTAG commands to the Spartan-6 FPGA through a dedicated virtual JTAG IPBus slave, which will then use a dedicated bus to exchange the commands to/from the Kintex-7.

The Spartan-6 firmware is the real *Golden Firmware* of the GCU, since the FPGA is configured at the production phase and will never be reconfigured again. Therefore, the configuration code has to be as small and simple as possible, to avoid any possible misbehavior during the experiment.

By employing this extra FPGA for support, trying different configurations for the main Kintex-7 is a safe procedure, as a recovery and reconfiguration of the main FPGA is always possible and granted by the XVC-IPBus system. The reconfiguration of the Kintex-7 is slow compared to the standard JTAG-Universal Serial Bus (USB) connection (5 minutes vs few seconds), but the configuration process is parallelized, leading to a potential capability of reprogramming all the 7'000 GCUs Kintex-7 of the

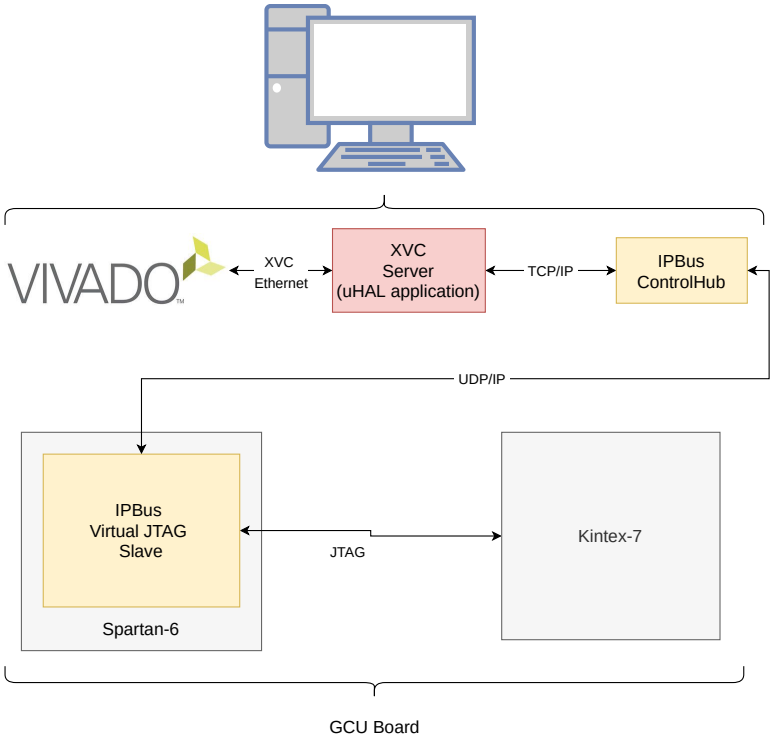

Figure 7.17: High level block diagram of the XVC topology.

JUNO detector in just a few minutes.

8

GCU Board Characterization

Upon arrival of the first GCU prototype board, which was coincidental to the start of my PhD program, a series of test have been performed in order to check its performances and functionalities.

When I joined the JUNO Padova electronics groups as a PhD candidate, my work mainly consisted in testing the board functionalities, as well as perform a reliability analysis in order to make sure the channel failure target of 0.5% over 6 year, as discussed in Sec. 6.1, is met. Most of the board characterizations required the development of a dedicated FPGA firmware. All the test and analysis I performed are detailed in the following sections.

8.1 Power Consumption

The main 36 V are provided by standard bench-top/rack mounted power supplies. This will be the same powering scheme employed on the JUNO detector, with the power supplies located on the surface and low impedance powering cables running inside the bellow together with the two communication link (synchronous and asynchronous/Ethernet link).

The power consumption of the board is a key parameter, as the GCU contained inside a water-tight metal box, will have no active cooling system, thus dissipating the heat by passive heat transfer to water; Maintaining a relatively low-temperature environment inside the box is essential to meet the reliability requirement of the board.

The power consumption is correlated to the logic designed within the FPGA, in particular by the percentage of resource utilization, the number and rate of I/O pins used, the clock frequency of

GCU Component	Power Consumption
DDR Memory	∼1 W
Single ADU	∼2.2 W
GCU board	∼20.9 W

Table 8.1: GCU power consumption measurements.

synchronous circuits and the toggle percentage of internal logic. To limit the power consumption, both the synchronous and asynchronous link do not use the dedicated high speed transceivers available in the FPGA.

Table 8.1 resumes the measured power consumption of the GCU's main components. The observed power consumption with the GCU's FPGAs configured with the latest firmware and all the components enabled (ADUs, DDR3 ...) is about 20 W. Measuring the power consumption is crucial, especially concerning the UWB design, in order to ensure that the board temperature plateaus at a value that meets the reliability requirements (see Sec. 8.3).

8.2 Thermal Analysis

The reliability requirements for the JUNO under-water electronics make the heat distribution of crucial importance. High temperatures can cause performance degradation and failures both on the PCB as well as at the die level.

Thermal imaging cameras are extremely helpful, performing live analysis of the thermal distribution creating an image using infrared radiation. Thermographic camera can be exploited during the prototype phase of development, to quickly find faulty spots on the board, such as issues in PCB manufacturing and assembly, short-circuits and other general hardware failures that typically manifest as high-temperature spots. Moreover, a thermal image can be used to identify the highest temperature points of the board, for a more precise estimation of the board's life time.

Thermographic images of the GCU can be seen in Fig. 8.1. In order to correctly measure the temperature through infrared thermography, all reflective surfaces, such as the FPGA, must be covered with black tape, since being inefficient emitters [84]. The effect of black tape application can be seen on Fig. 8.2.

Five temperature sensors are located on the GCU, whose temperature can be read out via slow-control (IPBus).

8.3 Board Reliability

A first estimate of the board reliability can come from the nominal Failure In Time (FIT) values of its components. The FIT rate of device is the number of failures expected in one billion (10^9) device-hours of operation (e.g., 1000 devices for one million hours, or one million devices for 1000 hours).

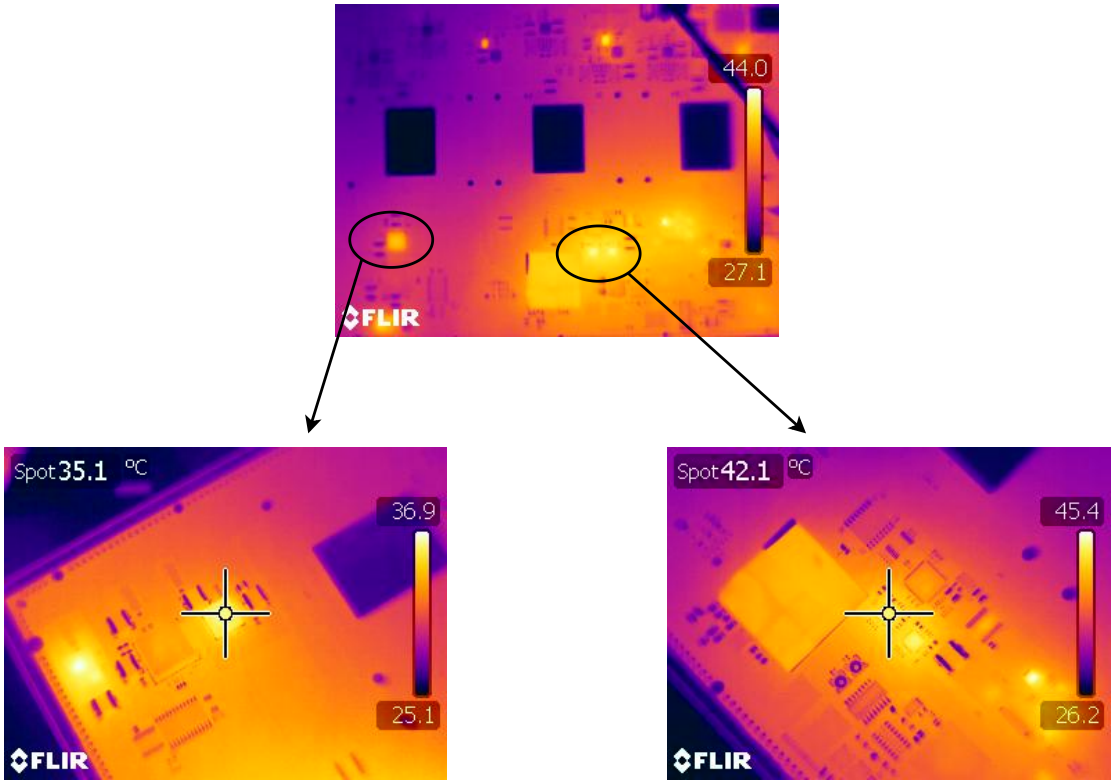

Figure 8.1: Thermal photos of the GCU with focus on the hottest spots.

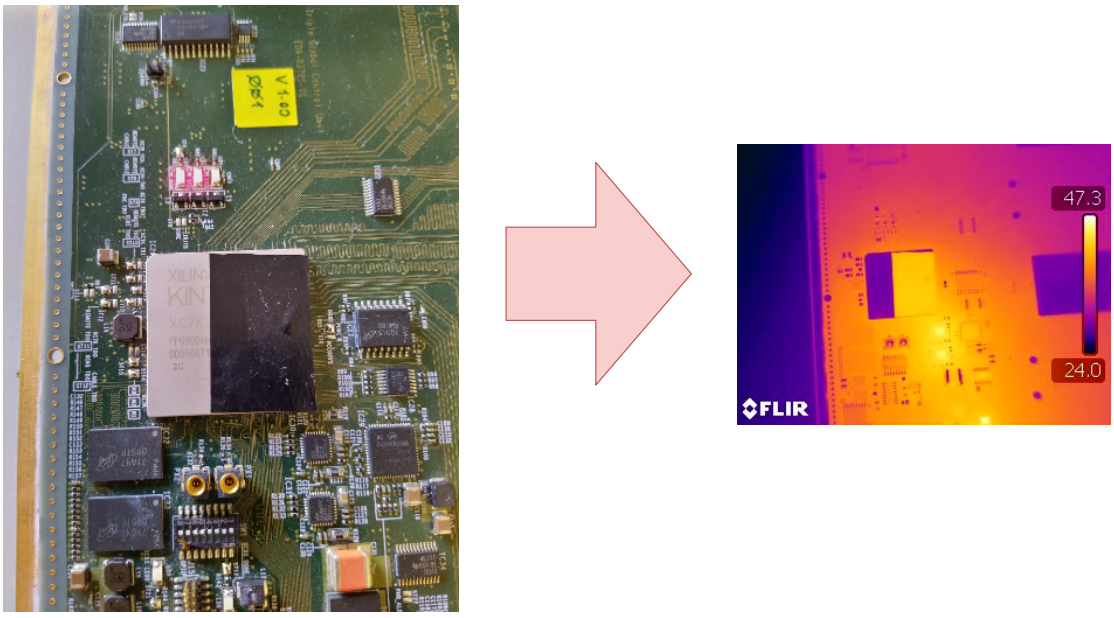

Figure 8.2: Effect of black tape application on reflective surfaces.

To compute the total FIT of the board, I have used an open-source C++ reliability calculation framework [85]. A set of classes have been developed in order to include every component in the FIT estimation. I have personally contributed to develop those dedicated to the passive components such as resistors and capacitors, in order to extrapolate their FIT values from [86], providing all the necessary information. As long as their current and power limits are not exceeded, their contribution is usually negligible, as most of the overall FIT value is normally decided by the IC chips on-board. The framework allows the user to include each IC with the correspondent FIT, which is usually given by the company or inferred from dedicated tests when the chips are custom. After having included all the board's components, the user needs to set an environment temperature, which can be tuned for each component, according to their own thermal resistance or experimental thermal measurement (using thermal imaging, for instance). The software automatically adjusts its lifetime, following the Arrhenius equation [87]:

$$\mathrm{AF} = \exp\left(\frac{E_a}{k_B} \cdot \left(\frac{1}{T_{\mathrm{prov}}} - \frac{1}{T_{\mathrm{op}}}\right)\right) \tag{8.1}$$

$$\mathrm{FIT}_{\mathrm{op}} = \mathrm{AF} \times \mathrm{FIT}_{\mathrm{prov}} \tag{8.2}$$

where:

- $\mathrm{FIT}_{\mathrm{prov}}$ is the provided FIT value, while $\mathrm{FIT}_{\mathrm{op}}$ is the FIT value at the operational temperature of the component.
- AF is the acceleration factor
- E_a is the activation energy of the component
- k_B is the Boltzmann constant
- T is the temperature. T_{fit} refers to the temperature of the provided $\mathrm{FIT}_{\mathrm{prov}}$, T_{op} refers to the operational temperature of the component.

Tab. 8.2 shows the computed FIT values for the underwater electronics. The temperature "T" is the environment temperature. Based on the thermal pictures shown in Sec. 8.2, the temperature of the hottest component have been raised accordingly. This was not possible to be done for the ADU and HVU, as only the overall reliability values at a certain temperature are provided from the Chinese colleagues that performed the tests.

The fail fraction is retrieved from the FIT value considering the following relation:

$$\mathrm{FF}_h = \mathrm{FIT}/10^9 \tag{8.3}$$

where FF_h is the fail fraction per hour. It is important to consider that a failure in the GCU comport the loss of three channels, while with a failure on the ADU or HVU only a single channel is lost. The total number of channel failures are computed considering a time of six years.

T [°C]	GCU FIT	ADU + HVU FIT	Channel failures due to GCU failures [%]	Channel failures due to ADU + HV failures [%]	Total channel failures [%]
25	10	23	0.16	0.12	0.28
30	15	36.6	0.24	0.19	0.43
35	23.5	55.8	0.37	0.29	0.66
40	35.3	85	0.56	0.45	1.01
45	52.4	127.8	0.82	0.67	1.49

Table 8.2: FIT values for the different FEE components and relative percentage of expected channel failures.

As mentioned in Sec. 6.1, the target for channel failures due to the electronics is less than 0.5%. Given that the water design temperature of JUNO is about 21°C, the UWB cooling should prevent the environment temperature inside the box to raise over 30°C to reach the target.

8.4 The Synchronous Link Characterization

The assessment of the synchronous link performance and transmission reliability is crucial for validation of the GCU board. I have performed two different tests to analyze different aspects of the transmission:

- PseudoRandom Binary Sequence (PRBS) Bit Error Rate (BER) test
- Eye diagram examination

8.4.1 PRBS BER Test

Sending a long sequence of bits through the system is needed to calculate the BER, which is equal to the number of incorrectly received bits divided by the total number of bits sent. The BER is estimated perfectly in the limiting case where the total number of sent bits tends to infinity; in reality, a statistical approach has to be used. This means that, instead of trying to estimate the BER of the transmission, we aim to reject with a pre-determined level of confidence the hypothesis that the BER is higher than a certain value.

By fixing the BER value at 10^{-12} (standard for data transmission over fiber optics and Ethernet channels) and the Confidence Level (CL) threshold at 95%, the number of bits required to be sent without any error is about $3 \cdot 10^{12}$ [88]. With a data rate of 250 Mbps, this equals to 200 minutes of error-free data transmission.

The test setup, shown in Fig. 8.3, is designed using a loop-back Cat-5E cable, where the same board generates a PRBS sequence, sends it to two twisted pairs and recover the same sequence through the two remaining twisted pairs in the cable that have been shorted on the other end. The total length of the cable is 50 meters, so that the overall trip length is 100 meters. To monitor the transmission, I have implemented in firmware a PRBS checker alongside an error counter. The monitoring of the

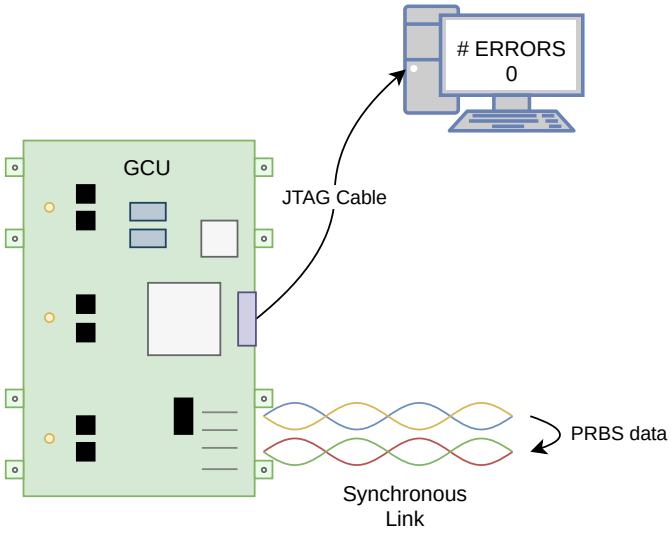

Figure 8.3: Test setup for the PRBS test of the synchronous link.

PRBS errors is performed through the customizable ILA IPC by Xilinx. Both the PRBS generator board and the CDR implementation board has been kept at constant temperature (ambient temperature) throughout the whole test.

The test ran for 200 minutes with zero errors counted, allowing to reject the possibility of a BER higher than 10^{-12} with a CL of 95%.

8.4.2 Eye Diagram Examination

To check the quality of transmission, an eye pattern figure has been recorded and displayed in Fig. 8.4. The data sent through the 100 m Cat-5E UTP cable is 125 Mbit/s, 1-to-2 BMC. The pattern is obtained by capturing the data stream after the cable equalizer chip. The driver-equalizer pair is needed to transmit and reconstruct the data stream over long cables, and therefore the vertical eye width presents minimal impact from the cable trip. The main issue that could potentially impact the data transmission quality is jitter, affecting the horizontal opening of the eye, reducing its width. In our case the overall eye width is about 7.8 ns with $\sim$ 74'000 recorded waveforms. This guarantees an optimal tolerance for correct data sampling. The eye jitter RMS is about 6.5 ps.

An eye patter has been retrieved at 250 Mbps as well, reported in Fig. 8.5, showing ideal conditions for correct data sampling. The recovered clock from the CDR is also recorded with its jitter histograms. As visible, the setup and hold times are met and the cycle-to-cycle jitter standard deviation is 3.4 ps RMS.

8.5 Ethernet Link Performances

To validate the asynchronous Ethernet link, two different tests have been performed:

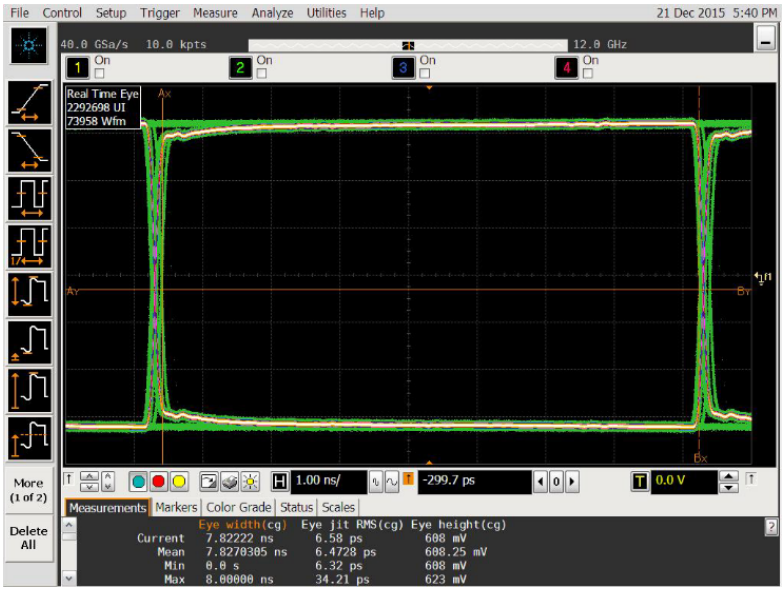

Figure 8.4: Measured eye diagram of the BMC data at 125 Mbps after 100 m of Cat-5E UTP cable.

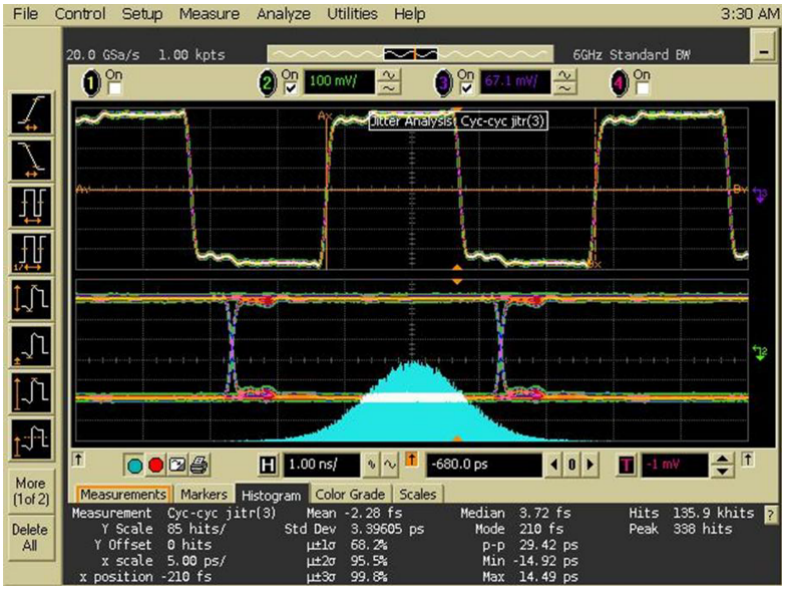

Figure 8.5: 250 MHz clock recovered on the GCU, CDR data output eye diagram and jitter measurements [62].

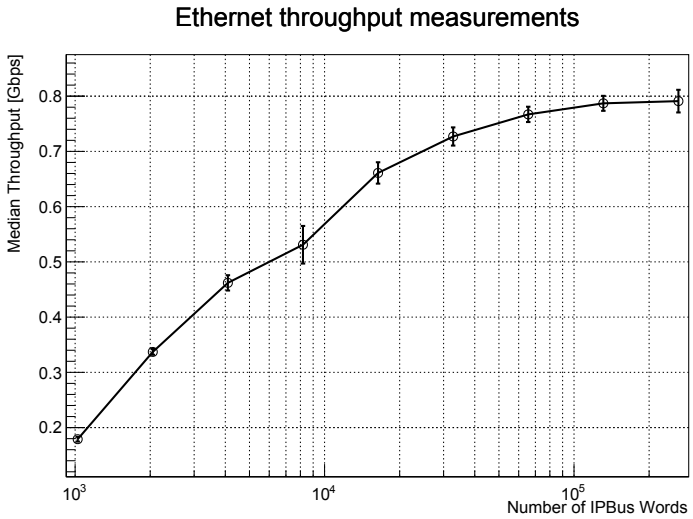

Figure 8.6: The measured median throughput as a function of depth, for one software client controlling one IPBus device, via the ControlHub.

- **IPBus throughput test**, where the total throughput of a single and multiple μHAL clients is measured.
- **Trigger rate test**, where three μHAL clients request waveform data from the three channels of a single GCU, using ControlHub.

Ideally, the trigger rate that a single GCU can sustain is easily retrieved by the following formula:

$$Trigger\ Rate = \frac{Total\ throughput\ [bit/s]}{Number\ of\ channels * Single\ data\ packet\ width\ [bit]} \tag{8.4}$$

but in a real-world scenario other factors may have an influence on the actual sustainable trigger rate; the ControlHub for example, might have difficulties to balance the load of the three channels μHAL clients, accessing the data from mostly one or two.

8.5.1 IPBus Throughput Test

The throughput test has been performed to confirm the expected performances shown in Sec. 6.2.4.1. The testing setup consists of a single GCU connected through a gigabit switch to a server, where μHAL clients access an IPBus slave register, via the ControlHub. The scripts, as well the firmware, that I developed for the test have been kept as minimal as possible, to avoid any bias in performances due to time-consuming tasks.

The first scenario is the *1-to-1 block transfers* where the server runs a single μHAL client which accesses a single IPBus slave register. The outcome of the test are shown in Fig. 8.6.

The results clearly show that the experimental measurements outperform the expected one, with the maximum throughput being about 800 Mbps versus the 500 Mbps reported by the IPBus official

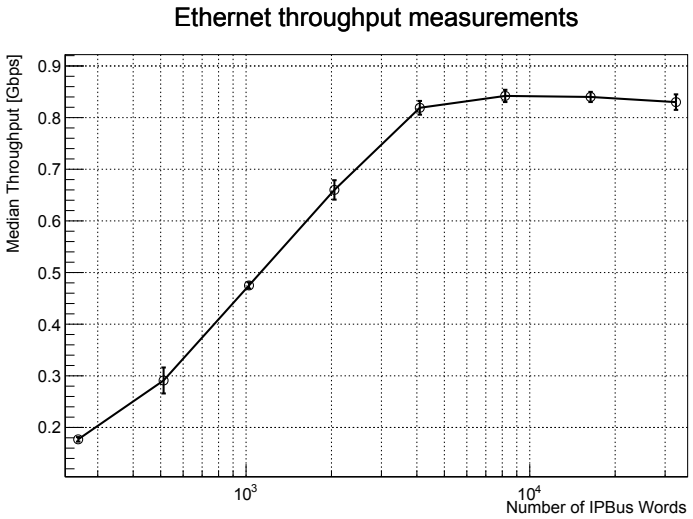

Figure 8.7: The measured total median throughput as a function of depth, for three software clients controlling one IPBus device, via the ControlHub.

documents. In both plots the curve reaches the plateau value at about 10^5 number of words, which equals to 400 kB Ethernet packets payload. Such difference is likely to be caused by the different version of IPBus suite used for the test, compared to the outdated one used in the IPBus documentation.

The second scenario is the *3-to-1 polling*, where three different μHAL clients runs on the same server accessing three different registers on the same device. This will emulate the operative data acquisition conditions for a single GCU, where the three clients poll data from the three PMTs data paths. To perform the test, three different instances of the same script used for the *1-to-1 block transfers* are launched. The results are shown in Fig 8.7

Comparing the results of the two different scenarios, we can observe how the 3-channels acquisition reaches the plateau value with smaller IPBus transactions, but the value itself does not differ much, going from about 0.8 Gbps for the single client configuration to about 0.85 Gbps for the multiple clients setup.

8.5.2 Trigger Rate Test

As stated above, the maximum trigger rate sustainable by the DAQ (i.e., without experiencing any data loss) is not directly linked with the throughput, as different factors may have an impact, such as the ControlHub "load-balancing" efficiency. The total throughput can anyway give an indication, fixing an upper limit on the maximum trigger rate, given by Eq. 8.4.

The setup for the trigger rate test, shown in Fig. 8.8, is simple: an external pulse generator module sends external trigger pulses at a user-controlled frequency, to the BEC system, through a SubMiniature version A (SMA) connection. The BEC/TTIM firmware treats the external trigger as a global trigger, timestamping the pulse, sending the time to the GCU via synchronous link. In the GCU's FPGA, the

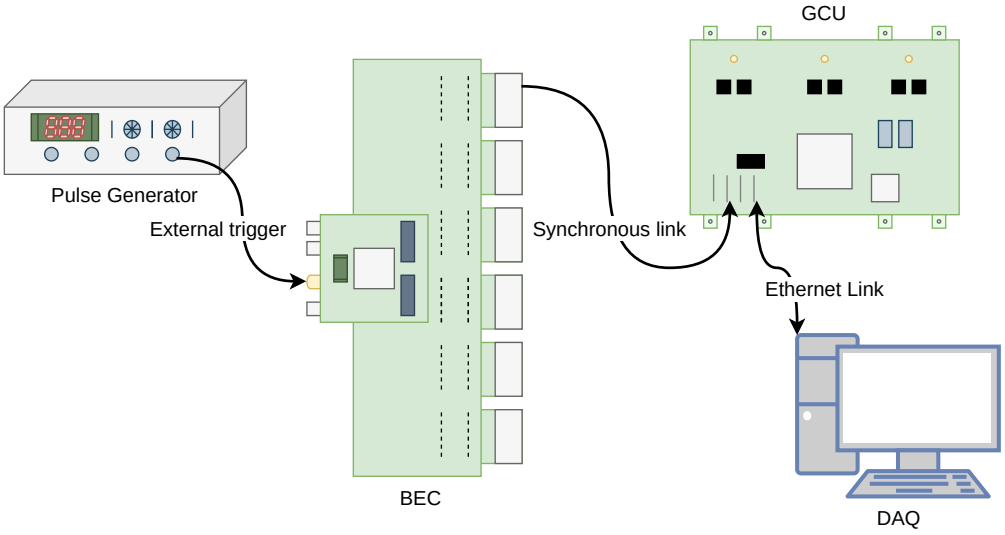

Figure 8.8: Setup for the trigger rate test.

correlated time window is extracted from the circular *L1-cache* of each channel and placed on FIFOs waiting for the DAQ request.

I, together wit the JUNO Padova electronics group, performed two different tests in order to validate the DAQ firmware/software architecture:

- A single channel acquisition
- A three channels/single GCU acquisition

For the **single channel acquisition** only one PMT channel data is requested by the DAQ, therefore falling into the *1-to-1 block transfers* scenario, where a single μHAL client perform a block read of a single register (the PMT waveform data).

The **three channels/single GCU acquisition** corresponds to the *3-to-1 polling* scenario, having three μHAL clients, one for each channel, block-reading a register in a single device.

The only parameters that have an influence on the maximum sustainable trigger rate are:

- the number of IPBus words read in a single block-read. As seen previously, this influences the total throughput.
- the trigger window width, which determines the number of bits that need to be transferred for a single event. Its influence is visible in Eq. 8.4.

Table 8.3 summarize the parameters chosen for the test.

The results of both tests are shown in Fig. 8.9. The efficiency value in the plot is defined as

$$Efficiency = \frac{\#\ of\ acquired\ events}{\#\ of\ external\ trigger\ sent} \tag{8.5}$$

Single Channel	
# of IPBus words	2048
Trigger window width	320 ns
Three Channels	
# of IPBus words (single client)	2048
Trigger window width	320 ns

Table 8.3: Acquisition parameters used during the trigger test.

Concerning the single channel acquisition, the efficiency starts to drop somewhere between 50 and 60 kHz. Considering that the single channel throughput is about 300 Mbps and that a single event consists of 5120 bit (320 ns * 16 bit), applying Eq. 8.4, the maximum achievable trigger rate is about 58 kHz. The consistency of the theoretical scenario with the measurements is given by the fact that, since only one single μHAL client is exchanging data with one device, no load needs to be balanced by the ControlHub and Central Processing Unit (CPU).

When running the three-channels acquisition, the total bandwidth is about 600 Mbps, which translates in ∼40 kHz applying Eq. 8.4. Fig. 8.9 shows that, at a rate of 40 kHz, the efficiency value already has started to drop, and even for lower event rates the efficiency is little below 1. This is probably due to the inefficiencies of the ControlHub/CPU to balance the different μHAL clients load, so that the total bandwidth is not equally spread between the three channels at any given time. However, this is not an issue for the DAQ, since the event rates foreseen in JUNO for which to use the default acquisition are small, residing in the *full-efficiency* zone.

When acquiring multiple channels, the efficiency value can be defined as

$$Efficiency(c) = \frac{\#\ of\ events\ acquired\ by\ at\ least\ \text{“}c\text{”}\ channels}{\#\ of\ external\ trigger\ sent} \tag{8.6}$$

To perform such analysis, a proper *event building* software must be designed, and for each event (timestamp), the number of channels that record this event has to be determined (the c parameter in Eq. 8.6). For a single GCU acquisition, each event can have a value of c up to 3, which means that the event is present in all the three channels data.

An efficiency plot based on Eq. 8.6 is shown in Fig. 8.10.

8.6 DDR3 Validation

The verification of the DDR3 memory chips is essential to ensure an error-free data transmission in writing and reading through the memory bus. In the firmware, The Xilinx 7 series FPGAs memory interface solutions core is exploited [89]. It is a combined pre-engineered controller and physical layer for interfacing 7 series FPGA user designs and Advanced eXtensible Interface 4 (AXI4) slave

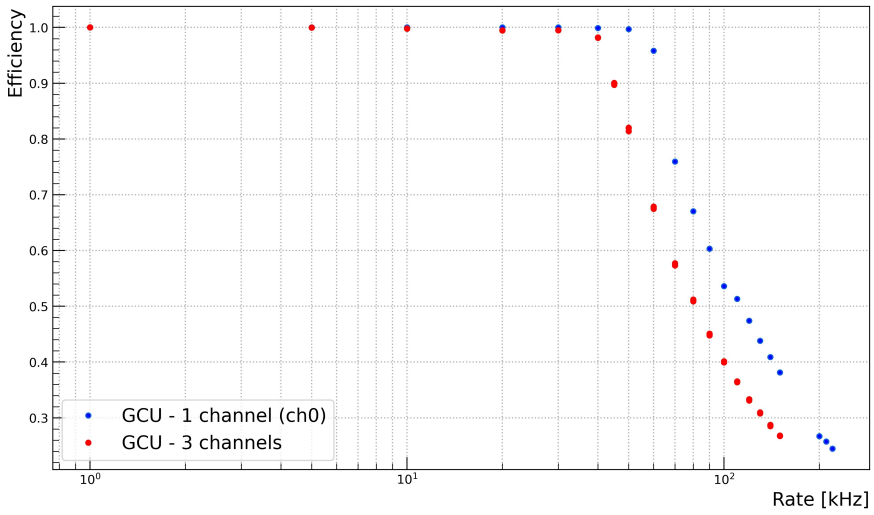

Figure 8.9: Trigger rate test results for both the single channel and three channels acquisitions.

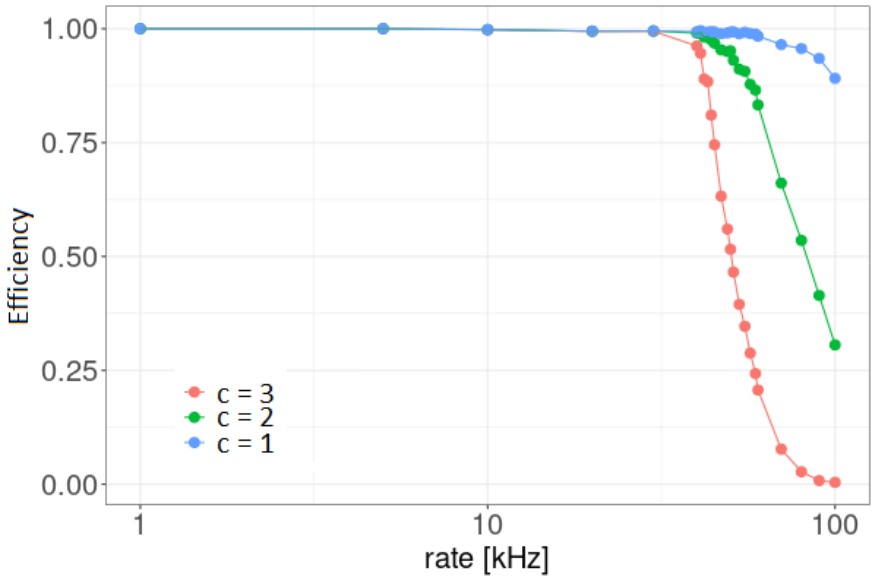

Figure 8.10: Efficiency plot based on Eq 8.6.

interfaces to DDR3 SDRAM device.

Besides the memory controller, the key component that makes up the design is the traffic generator which generates data patterns through RTL logic, looping through the address range.

When the memory has been initialized, the traffic generator begins stimulating the interface port to create traffic to and from the memory device. By default, the traffic generator sends pseudo-random commands to the port, meaning that the instruction sequence (R/W, R, W, etc.) and addresses are determined by PRBS generator logic in the traffic generator module, in order to model real-world traffic. The read data returning from the memory device is accessed by the traffic generator through the user interface read data port and compared against internally generated "expected" data. If an error is detected (i.e., a mismatch between the read data and the expected data), an error signal is asserted and the corresponding led on-board turns on.

After having implemented the DDR3 validation design in the GCU's Kintex-7 FPGA, I ran it for a few days with no errors being detected, surpassing by far the requirements to reject the possibility of a BER higher than 10^{-12} with a CL of 95%.

9

Upgrade to the GCU v2.0

Due to budget constraints, a new version of the GCU has been developed, with great effort of our Chinese colleagues from IHEP. The resulting board retains the same concept of the first version of the GCU described in this dissertation, but including a few modifications in order to make the new design more "cost-effective". Besides changes in the material for the PCB and for the passive components, other modifications described in the following sections have an impact on the board conceptual design and functionalities, and required effort in terms of firmware development in order to adjust the FPGA configuration for the upgrade. Personally, I have been in charge of adapting the synchronous link protocol, whose architecture changed completely. Nevertheless, after the new firmware was developed, the link was still affected by potential problems that could result in synchronization loss between the FEE and BEE. To avoid such issue, the functionalities of a CDR chip has been implemented in FPGA, which increases the link immunity to environmental noise. This core I have developed is openly available online [90], and it is easily portable to other, non-Xilinx, FPGA families.

The new board also includes the ADUs in the same PCB, as Fig. 9.1 shows. Heat sinks copper blocks are also used, which are foreseen to transfer the heat efficiently to the UWB enclosure.

9.1 The New Synchronous Link

A major difference in the new GCU version concerns the synchronous link. Both the link hardware and protocol is different, in order to make it more efficient and get rid of consequently unused components.

Concerning the protocol, no communication channels are TDM, instead they are broken up in order

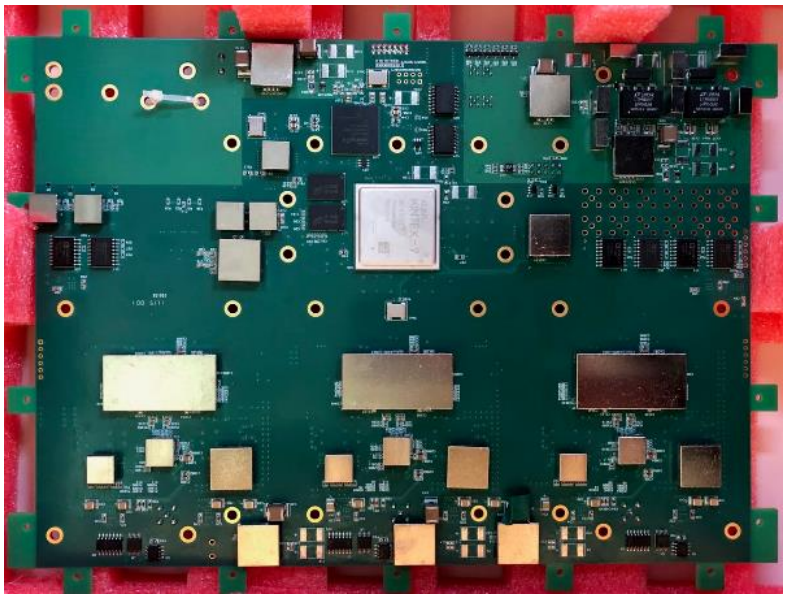

Figure 9.1: The upgraded version of the Global Control Unit. Heat sinks copper blocks are placed on the board hotspots.

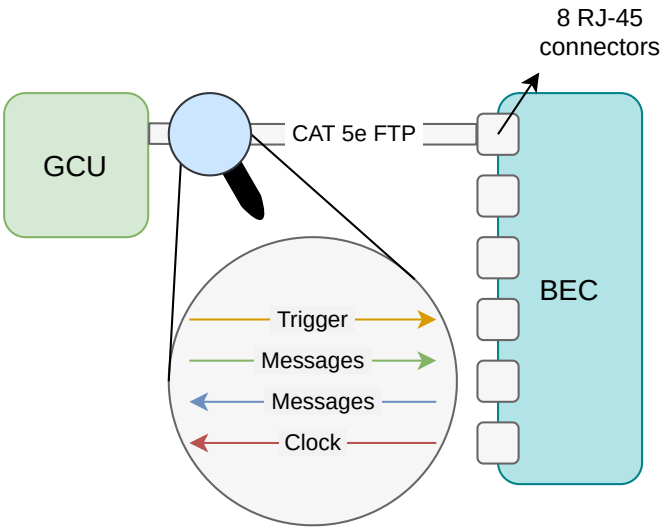

Figure 9.2: The new synchronous link cable pair structure.

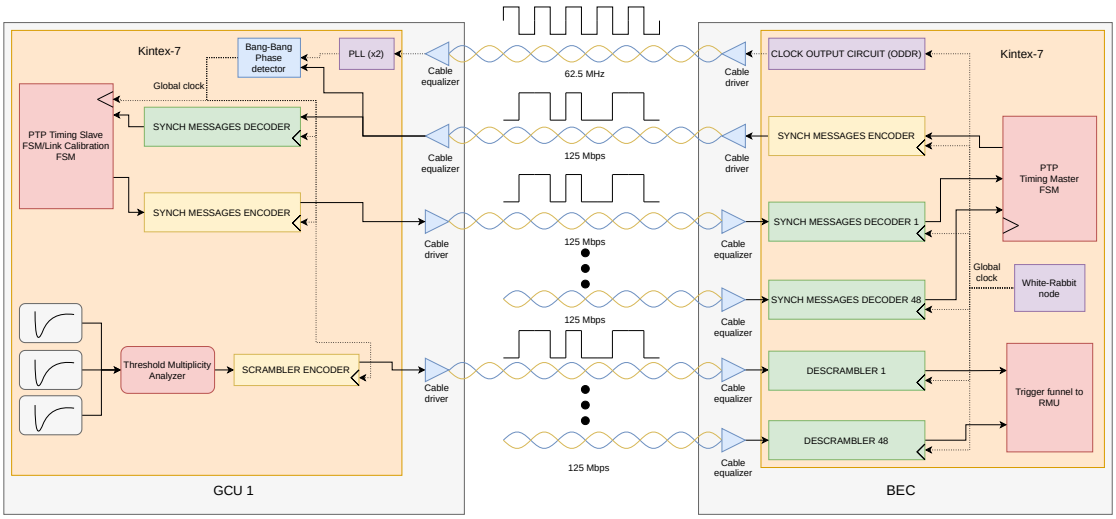

Figure 9.3: The new synchronous link digital design. Full lines represent data paths while dotted lines represent clock signals.

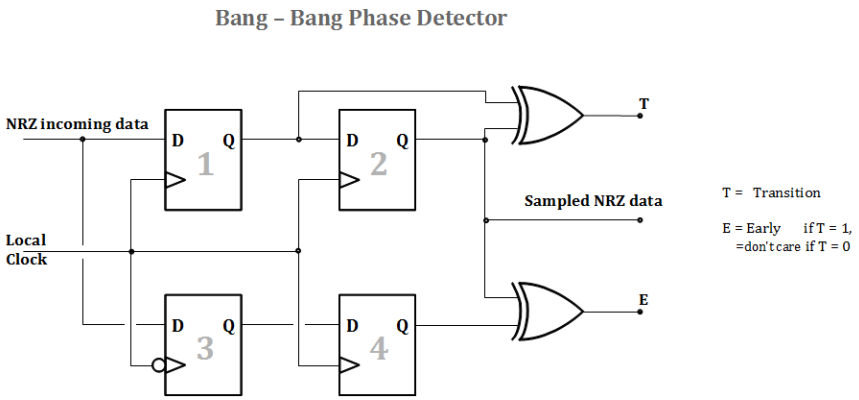

Figure 9.4: The Alexander type Bang-Bang (BB) phase detector [91].

to exploit all the four twisted pairs of a Cat-5E cable. Furthermore, the clock is no more embedded in the data and is now sent explicitly through a single pair. As shown in Fig. 9.2, the different pairs transport

- 125 Mbps, GCU to BEC trigger requests.
- 125 Mbps, Bidirectional synchronous messages (broadcast and individually-addressed).
- 62.5 MHz Digital clock (BEC to GCU).

This reorganization of the protocol allows to drop the CDR chip from the design, as the clock signals enters the FPGA directly going through two FPGA's PLLs, one used in a jitter cleaner configuration [92], and the second used to retrieve all the necessary clock frequencies. A schematic of the implementation is shown in Fig. 9.3.

The cable equalizer chip is still used to recover the data over the long Cat-5E cable. As this chip requires a minimal data rate (long constant values on the link will result in loss of data locking), all the link channels requires some kind of encoding to make sure a minimal switching activity is present. The physical layer of the synchronous messages remains unchanged, as the channel is still BMC.

The same BMC encoding was not possible to employ for the trigger link: a requirement from the collaboration is that the trigger link should not just provide the logical "OR" of the three PMTs trigger every 16 ns, but the multiplicity instead, therefore requiring two bits and the full 125 Mbps throughput (which would be split in half from the 1b/2b BMC). To avoid wasting bandwidth, a scrambler encoder/decoder scheme has been implemented, so that the PRBS-like encryption put in place guarantees the minimal switching activity.

Due to the absence of the CDR, the clock recovered on the GCU and the master clock from the BEE have different clock domains, featuring the same frequency but random phase relationship; sampling the incoming messages may lead to setup and hold time violations [78], introducing errors in the communication. On the GCU side, this potential issue is controlled by employing an Alenxander type BB phase detector [91] (Fig. 9.4), that allows to control the data-clock phase exploiting the phase-shift capability of the FPGA clock management tiles. On the BEC side, the same calibration procedure detailed in Sec. 7.1.4.3 is used for both the trigger and the synchronous message line. Errors on the message pairs are retrieved thanks to the Hamming code error detection capability, while for the trigger link which does not foreseen any error detection/correction encoding, the error count is retrieved by sending PRBS data during the calibration phase and use a PRBS-checker on the backend (receiver) side. As the line rate is half compared to the old link, the calibration procedure only spans one full period, but it is still enough to calibrate the link and avoid metastability issues. The calibration eye is shown in Fig. 9.5. Moreover, with the new data rate the performances of the IEEE 1588-2008 PTP protocol degrades, and the synchronization window between the FEE and BEE goes from ± 4 ns to ± 8 ns, although still fulfilling the requirements.

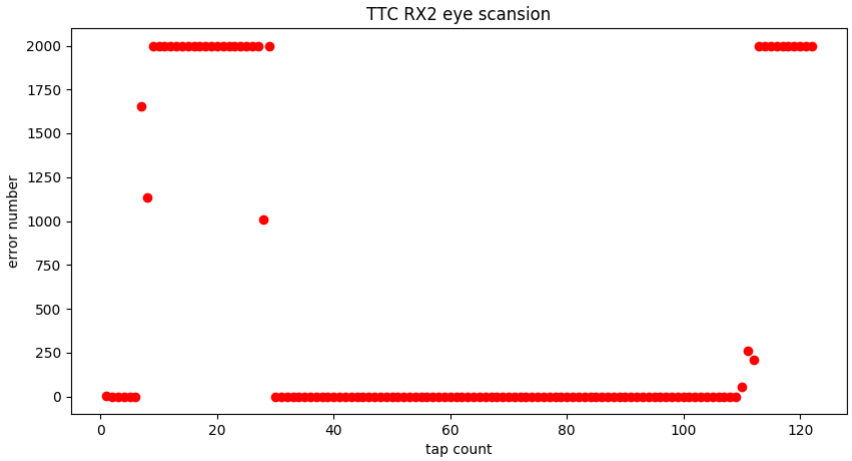

Figure 9.5: Bathtub plot of the LVDS serial data stream capturing of the new synchronous link.

9.2 The New Asynchronous Data Readout and Slow Control Link

In the GCU v.2 the architecture of the Ethernet link has been changed. On the first prototype, the external link was connected to an on-board Ethernet switch IC, which would allow both the Xilinx Kintex-7 and Spartan-6 to connect to the network. An Ethernet hub has been now included in the Xilinx Spartan-6 configuration, which is now capable of routing the Ethernet traffic of both the Xilinx Kintex-7 and itself, without any drop in performances. The only firmware modifications needed for the new design concern the Xilinx Spartan-6 FPGA, where the RGMII hub had to be added. The new firmware architecture for the small FPGA is shown in Fig. 9.6.

9.3 The UnderWater Box

The UWB has been developed in IHEP, and it is essential to provide the frontend electronics with a water-tight environment as well as a mechanical anchor to the detector truss. Fig. 9.7 and 9.8 show an open and closed UWB respectively.

The box structure come from a single metal sheet, 6 mm thick, that is later bent and argon-arc-welded. Once the electronics, including the GCU v.2 and the HVU together with their splitter board, is placed inside the box and the Cat-5E links + power cables are soldered, the top cover plane is laser welded to the box. Some measurements of the box are shown in Fig. 9.9

Several tests have been performed by the Chinese colleagues to ensure that the UWB would meet all the requirements in order to be employed in JUNO. Some of these tests are:

- Mechanical **stress** and **deformation** of the box under a loading pressure of 0.5 MPa (equivalent to $\sim$ 50 meters of water).

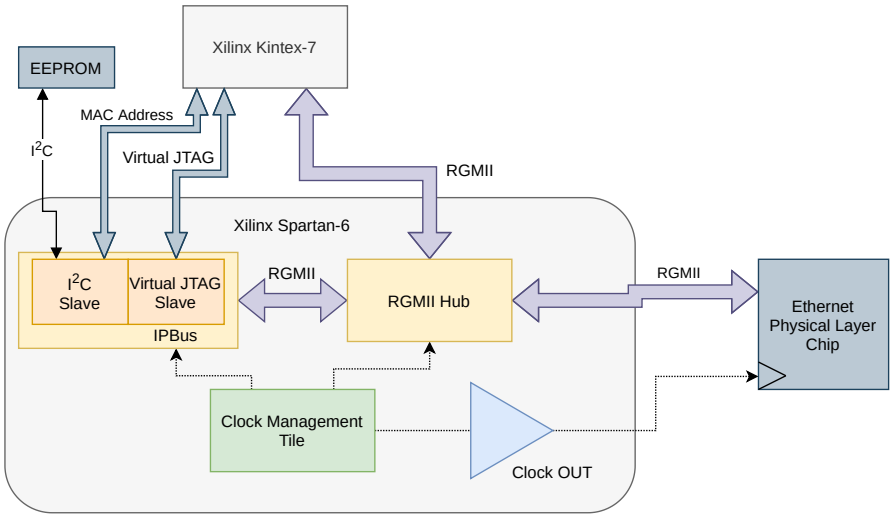

Figure 9.6: Overview of the Xilinx Spartan-6 firmware architecture, including the RGMII hub for Ethernet connection.

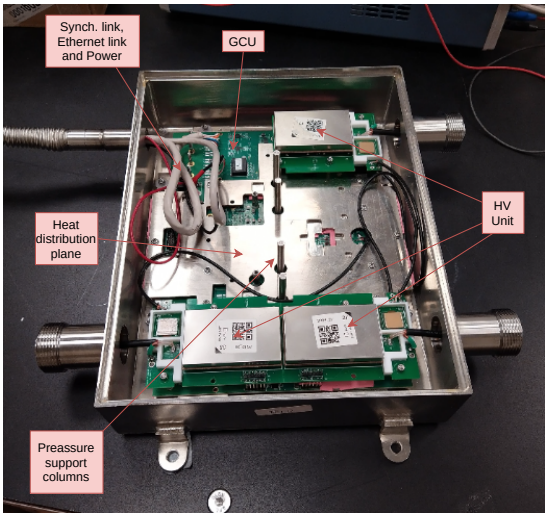

Figure 9.7: An open UWB and its internal components.

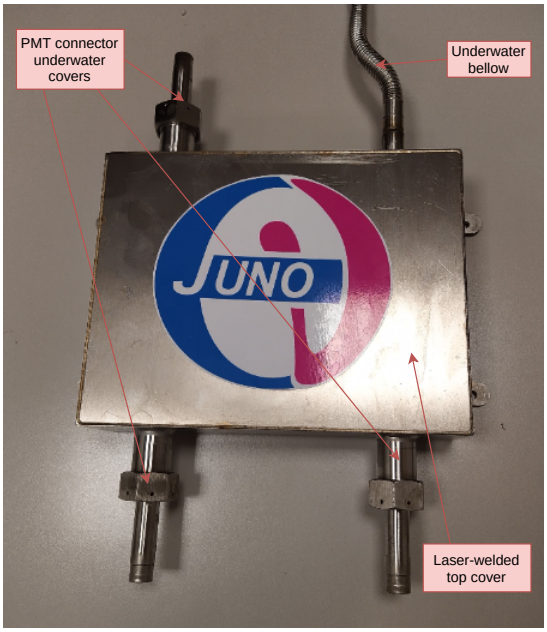

Figure 9.8: A laser-welded sealed UWB.

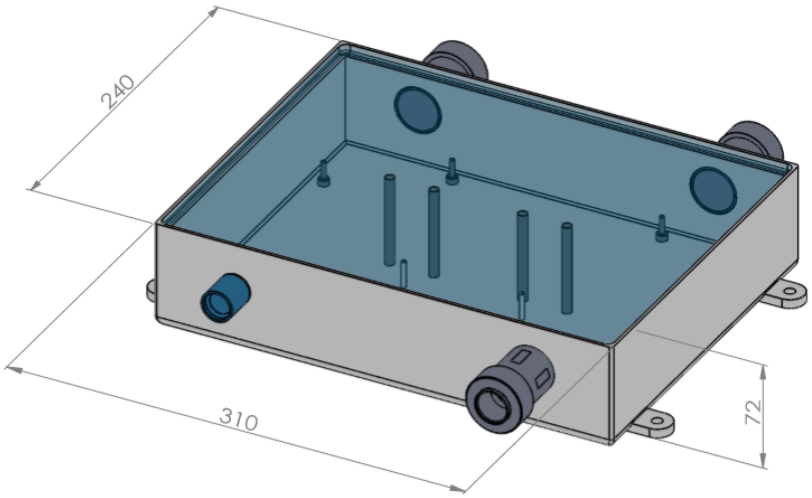

Figure 9.9: Mechanical drawings of the UWB.

- **Water leaking** test, exposing the box to 1 MPa of water pressure for about a week.
- **Helium leaking** test, using a leakage detector with the help of a vacuum pump.
- **Background** and possible additional **electronics noise** test.
- **Humidity** test, sealing an hygrometer into the box, placed in a water tank under a pressure of 0.5 MPa for 40 days.
- **Laser welding** temperature monitoring for possible damage to the electronics.

All of the test results fall inside the requirements for JUNO.

9.3.1 UWB Deep-Water Test

Subsequent to the reception of the first UWB prototypes, tests have been performed in Padova to ensure no damage has been occurred due to the China-Italy trip. A verification of the electronics has been performed hooking up the UWB to a JUNO PMT, powered by the GCU-attached HVU.

A more in-depth electronics and mechanical verification has been performed thanks to a collaboration with the *Y-40, The deep joy* pool in Montegrotto Terme [93], the deepest thermal water pool in the world, with its 42.15 meters in depth. The structure of the pool can be seen in Fig. 9.10 while a photo of the 40 meters hole can be seen in Fig. 9.11.

Since the UWB actually came with the top cover unsealed, the first operation has been the sealing of the box through laser welding. This has been performed by the mechanical workshop at the University of Padova. Prior to bury the box 40 meters deep, a small bucket has been filled with water in order to check for any major leak in the box and bellow. No leak has been registered.

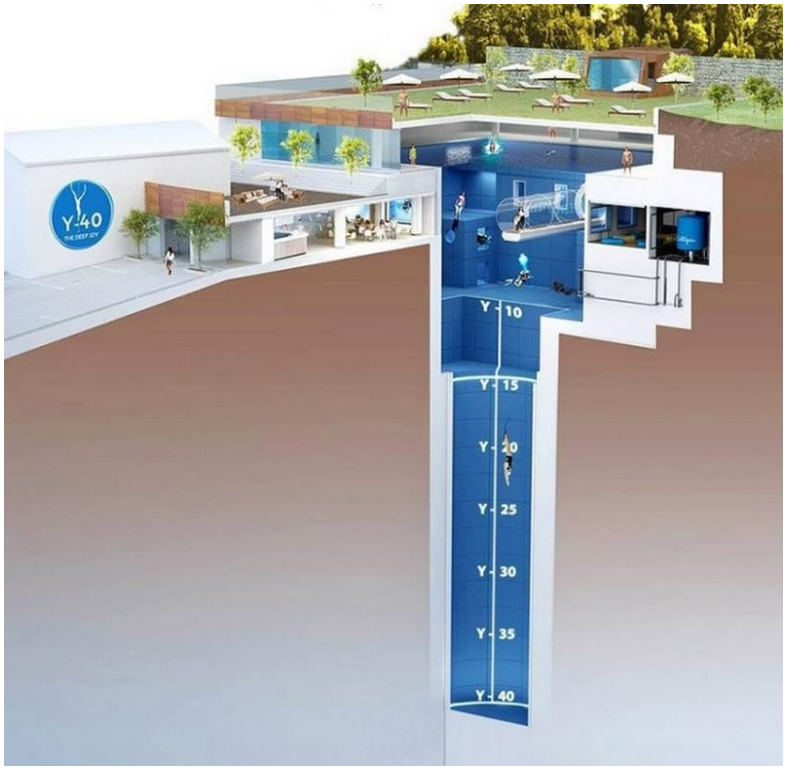

Figure 9.10: Y-40, The deep joy.

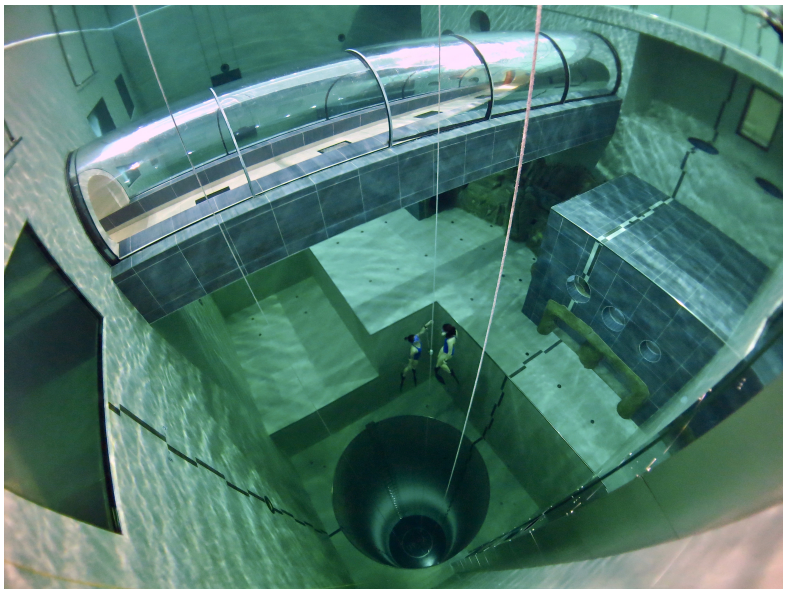

Figure 9.11: The 40 meters hole at *Y-40*.

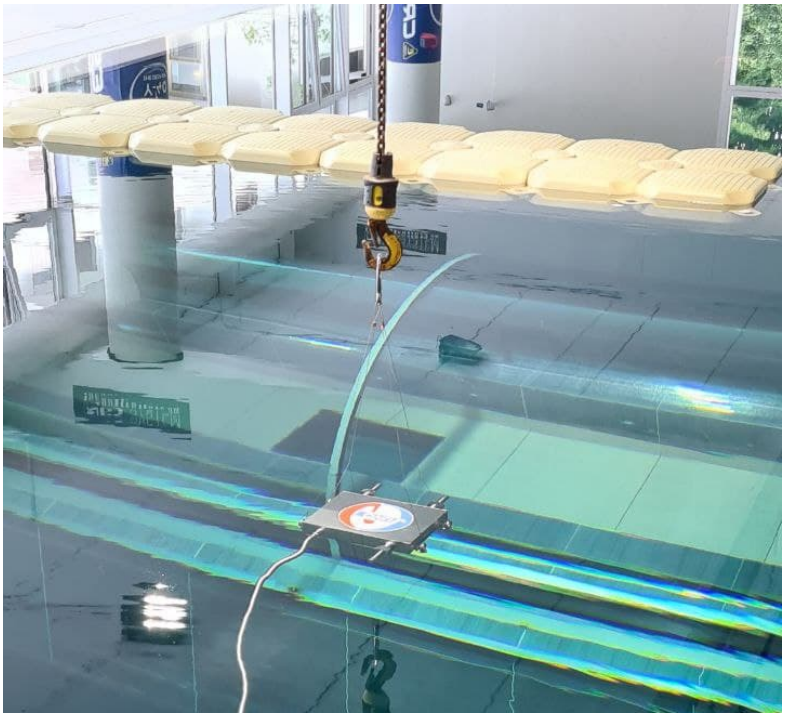

Figure 9.12: The lifting tackle used to lower the UWB.

To place the UWB at the bottom of the pool a lifting tackle has been used, visible in Fig. 9.12. Particular attention had to be paid in lowering the bellow, since it presents some stiffness making it hard to manage. To ease the unwinding operation, an uncoil system has been used. A photo of the system is shown in Fig. 9.13.

The box stayed lowered at the bottom of the pool for about 30 hours. During this time, the FPGA and HV units temperature was monitored, as well as the baseline average value and standard deviation. Since no BEC was used, a modified GCU-standalone version of the firmware has been developed, where there is no need of the synchronous link. The board has been set in self-trigger mode, where calibration pulses, a feature foreseen in the ADU, were triggered remotely via IPBus.

While underwater, the baseline value as well as its standard deviation has been monitored. Fig. 9.14 and 9.15 report the results for one of the three channels.

Moreover, the FPGA temperature has been recorded (firmware/software to read the DC/DC temperature sensors had not been developed yet). The results are shown in Fig. 9.16 and indicates a stable FPGA temperature of about 56°C with a water temperature of about 33°C. That equals to a difference in temperature of about 23°C. Since the water temperature in JUNO is foreseen to be about 21°C, the FPGA temperature should be below 45°C, which falls within the requirements in order to achieve the necessary reliability (see Sec. 8.3), considering that the FPGA die temperature is more than 15°C higher compared to the overall temperature of the board. A baseline - temperature value relationship is evident from the resulting plots: as the temperature increases the baseline

Figure 9.13: UWB with its bellow cable twisted in the uncoiling system.

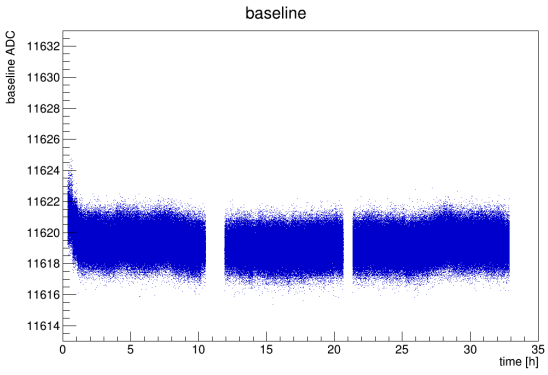

Figure 9.14: Trend of the channel 0 baseline value over the underwater time. The curve is interrupted twice due to stops in data taking.

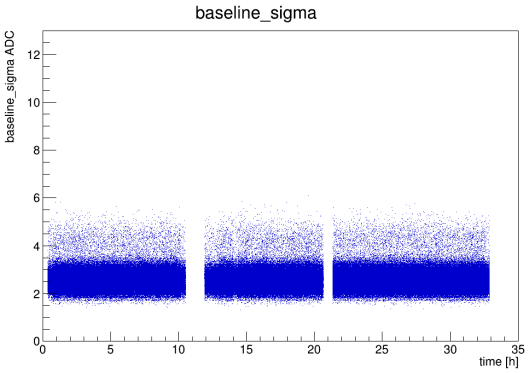

Figure 9.15: Trend of the channel 0 baseline standard deviation value over the underwater time. The curve is interrupted twice due to stops in data taking.

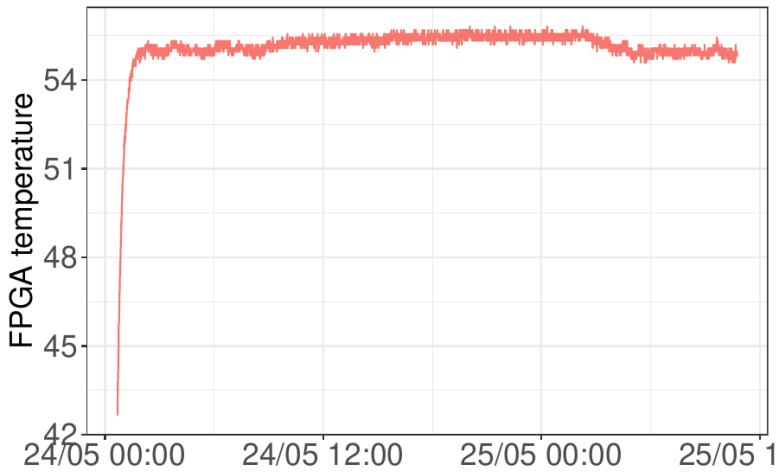

Figure 9.16: Trend of the GCU's FPGA temperature.

value decreases. No need of measurements were needed to further analyze this relationship, since water temperature in JUNO is kept at a constant temperature and therefore no changes in the GCU's temperature are to be expected once it stabilizes, which takes about one hour. The baseline standard deviation value did not show any relationship with the temperature, and remained stable during the entire test.

10

FPGA Implementation of a CDR

The immunity of the link to ElectroMagnetic Interference (EMI) is a key aspect of the synchronous link, particularly concerning the clock forwarding operation. With the JUNO laboratory still being under construction, the level of EMI is still unknown; for example, possible noise and interference can be caused by the complex calibration systems that are currently being developed [59]. If the FEE PLLs that recover the clock from the BEE are affected by this environmental noise, they may experience loss of lock, breaking the timing synchronization of the experiment. If that happens, the start-up calibration procedure has to be restarted.

To avoid any loss of clock issue, I have developed an FPGA implementation of a CDR, allowing the clock to be recovered directly from the 125 Mbps Manchester encoded stream, freeing up a twisted pair previously dedicated to the clock transmission for extra feature and improving the link immunity to EMI. The openly-available design [90] is introduced in the next sections, but the full published paper can be found at [94].

10.1 CDR Digital Design Overview

Usually, a CDR architecture is similar to the PLL model (fig. 10.1), where the phase of a reference signal is compared to the phase of an adjustable feedback signal, generally provided by a controlled oscillator, like a Voltage-Controlled Oscillator (VCO). The output of the Phase Detector (PD) is filtered and used to drive the VCO frequency. When the phase comparison is in steady state, e.g. the phase and frequency of the reference signal is equal to the phase and frequency of the feedback signal, we

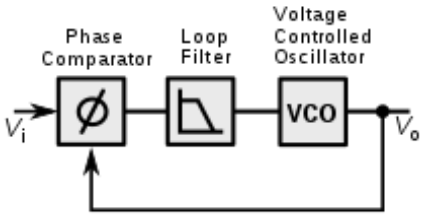

Figure 10.1: The standard PLL architecture.

say that the PLL is locked. In the case of a CDR, the steady state is reached when the VCO clock frequency matches the reference signal's data rate.

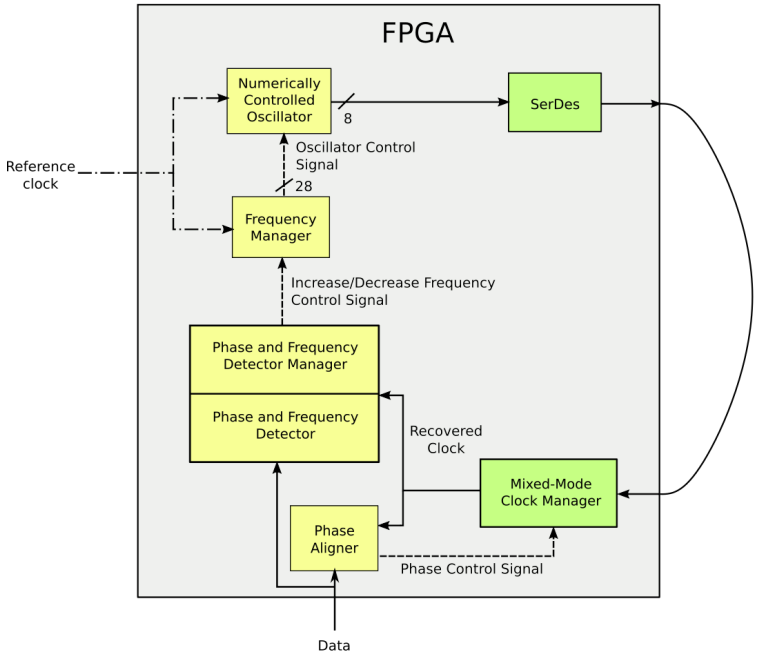

Figure 10.2: Block diagram for the proposed CDR design. Yellow blocks represents custom VHDL modules, green blocks are used to represent FPGA proprietary tiles. Dashed lines are used for control signals.

An overview of the proposed CDR architecture is given in fig. 10.2. The design is implemented in a Xilinx KC705 evaluation board [95] featuring a Xilinx Kintex-7 FPGA. The design mimics the PLL architecture, consisting of a Numerically Controlled Oscillator (NCO) which is used to create a frequency controlled clock, a Phase and Frequency Detector (PFD) monitoring the NCO's clock frequency to match it with the data rate, and a Phase Aligner (PA) that, together with the Xilinx 7 Series MMCME2_ADV tile [92], dynamically adjusts residual clock drifting and have a deterministic phase relationship with the incoming data stream.

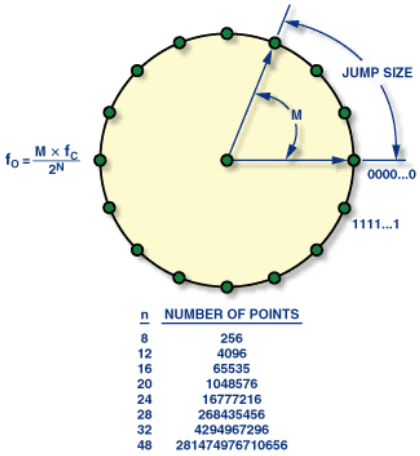

Figure 10.3: The phase-wheel.

Given the expected recovered clock frequency of 125 MHz, the design uses the HR general purpose I/O pin of the FPGA rather than dedicated transceivers, resulting in a reduced power consumption and a more straightforward design. Moreover, the core is not tied to any particular FPGA family, as the VHDL code is generic and no proprietary Xilinx IPCs are used. Nevertheless, particular attention should be paid for the porting of I/O logic resources (SerDes) and clock management tiles, which must be features supported by the FPGA foreseen to employ this solution.

10.2 CDR Modules

The **NCO** [96] design consists of two parts:

- A Phase ACCumulator (PACC), which is basically a counter driven by a reference clock incremented by a user-defined value related to the nominal data stream rate.
- A phase-to-amplitude converter, which uses the PACC output as an index to a LUT

The counter can be visualized as the phase-wheel shown in Fig. 10.3: a circle equally divided in a certain number of sections, bounded by phase-points (the PACC output) and for each phase-point we associate the corresponding sine value (this association process is done by the LUT). As a vector rotates around the wheel, by taking these correlated sine values a digital sine waveform is generated. A complete revolution around the phase-circle corresponds to a complete period of the sine wave. Imagining now that the vector skips a few (fixed) points each jump, the revolution is completed in a much shorter time. As a result, the frequency of the output waveform has increased. The correlation between the jump size, the reference clock and the output waveform frequency is

$$f_{OUT} = \frac{M \times f_C}{2^N} \tag{10.1}$$

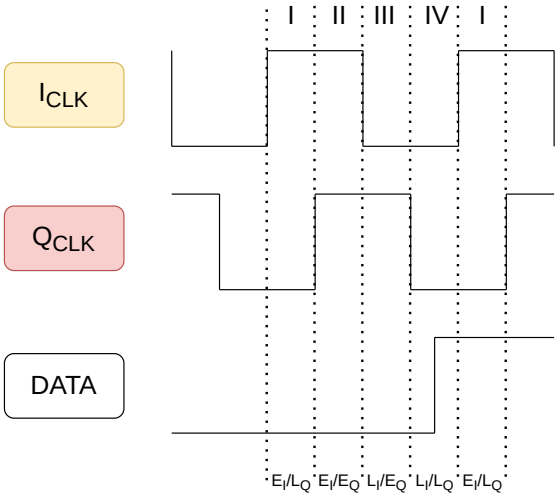

Figure 10.4: Two synchronous clocks with 50% duty cycle, I_{CLK} (In-phase Clock) and Q_{CLK} (Quadrature Clock), divide the period T in four quadrants identified by their positive and negative transitions. Q_{CLK} leads I_{CLK} by 90 degrees. Thanks to the Early/Late (E/L) identification by the Phase Detector Unit, it is possible to identify where the *DATA* transitions reside, the fourth quadrant in the example.

where:

- M is the jump size
- f_{OUT} is the NCO output waveform frequency
- f_C is the reference clock frequency, generated by a local oscillator on board
- N is the number of bits dedicated to the PACC counter

To retrieve a digital clock signal, the LUT design is simple: half of the circle is associated to the digital value 0, while the other half to the digital value 1. To overcome the maximum frequency limitation (which would be half of the reference clock frequency, corresponding to the Nyquist frequency), several phase-wheels are implemented in parallel with their outputs serialized using a SerDes tile in the FPGA. By implementing 8 phase-wheels, the maximum theoretical frequency that can be obtained is $4 \cdot f_C$. Of course, the clock frequency must be sustainable by the FPGA technology. Since the SerDes output can only be connected to IOB, a loop-back in and out of the FPGA is a precondition to be foreseen when designing the PCB.

The **frequency detection** capability relies on the use of two clock signals, with 50% duty cycle and orthogonal with each other ($\pi/2$ of phase difference). This allows the division of the entire 360 degrees clock period into four quadrants, as shown in fig. 10.4. A *frequency detector* module is used in order to estimate whether the data edges are shifting up (data period > clock period) or down (data period < clock period) in the clock quadrants. This information is used to adjust the clock frequency to match the data rate.

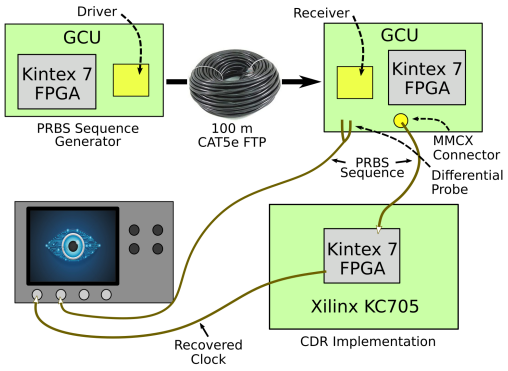

Figure 10.5: Block diagram for the CDR testing setup.

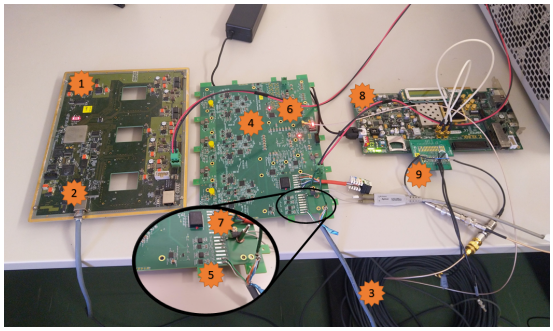

Figure 10.6: Picture of the CDR testing setup. · 1: GCU version 1.0 · 2: RJ45 connector · 3: 100m Cat-5E FTP cable · 4: GCU version 2.2 · 5: RJ45 soldering pads · 6: MMCX connector · 7: Differential probe · 8: Xilinx KC705 evaluation board · 9: FMC interconnection board..

Lastly, the **PA module** has the task of providing a deterministic phase relationship between the data and the clock edges, to ensure the optimal sampling conditions. To achieve this, a BB PD dynamically operates directly on the PLL, to generate an extra clock signal phase aligned with the data rate.

10.3 Transmission Testing

To evaluate the design, the proposed CDR has to recover the clock and the data from a 125 Mbps PRBS generated from a different board. To better emulate the JUNO conditions, the physical medium which transmits the sequence is a 100 meters long Cat-5E FTP cable.

The block design for the setup is illustrated in fig. 10.5 and 10.6. A first GCU board generates the PRBS sequence and exploits the on-board differential cable buffers to forward it to the cable where, reaching the end, a second GCU recovers the signal through the cable equalizer chip and redirects it to a MMCX connector and to a differential GPIO pin pair. No logic operations are performed inside this second FPGA. From the GCU's MMCX connector and through an FMC interconnection board, the PRBS sequence arrives at the Xilinx KC705's FPGA, where the actual CDR operation takes place. After the clock is recovered, this is used to sample the incoming data and, thanks to a PRBS checker module [97], monitor any error in the reconstructed sequence.

The recovered clock from the CDR is also used to trigger an oscilloscope, where the second GCU's differential pair signal is monitored thanks to a differential probe. By setting an infinite persistence in the oscilloscope's display, the eye pattern of the PRBS sequence is visible, and it is shown in Fig. 10.7. The eye width is about 6.4 ns (500.000 recorded eyes) while the eye jitter is about 217 ps RMS. These measurements guarantee the correct data sampling.

A BER test has also been performed. Following the considerations made in Sec. 8.4.1, with 400 minutes of error free 125 Mbps data transmission, the possibility of a BER higher than 10^{-12} is rejected with a CL of 95%.

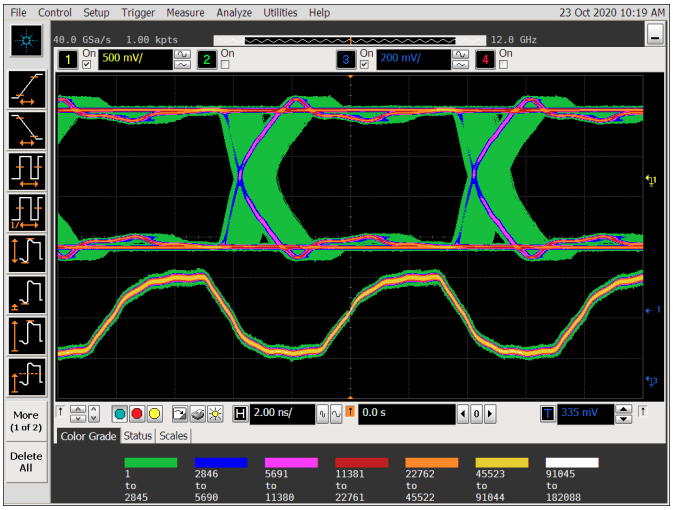

Figure 10.7: Measured eye diagram of the PRBS data at 125 Mbps after 100 m of Cat-5E cable (top) together with the CDR recovered clock (bottom).

10.4 CDR Clock Immunity to EMI

To test the improvement of the recovered clock stability to sudden EMI (and environmental noise in general), a qualitative test has been set up using a neon tube lamp placed underneath the Cat-5E coil, exploiting its “property” to emit EMI when turned on.

The first test has been performed with a JUNO-like architecture, where the first GCU board generates a 62.5 MHz clock, sending it through the Cat-5E cable to the second GCU board, where it is recovered by the FPGA’s PLL. The *locked* flag of the PLL is continuously monitored though the Xilinx ILA IPC [98]. In this condition, when the neon tubes are turned on, the PLL loses the locking state for several clock cycles. In an actual JUNO-experiment scenario, this would cause the board to lose the timing synchronization with the BEC, therefore losing data from three PMTs until a new synchronization procedure would run.

The same setup has been used to test the stability of the CDR recovered clock, sending PRBS-7 data though the cable and connecting the Xilinx KC705 board to the second JUNO board. The Xilinx ILA IPC has been used to check both the CDR locking condition as well as the PRBS error counter. The test shows that, even though the neon tubes induce errors on the recovered PRBS data stream, the CDR does not lose the lock and the recovered clock remains stable.

The proposed CDR is also insensitive to transition-free data pattern, not losing the lock condition keeping the recovered clock at a stable frequency.

Part III

The 48 PMTs Test Facility

11

The 48 PMTs Detector

A crucial part of the development of the Front-End electronics for a huge experiment such as JUNO is the ability of testing a smaller scale detector, in order to characterize the full electronics chain in a controlled environment, without having the complications of dealing with thousand of channels placed in an inaccessible location.

The 48 PMTs detector, shown in Fig. 11.1, is a standalone 17 liters LS detector located at the INFN - Laboratori Nazionali di Legnaro *(Legnaro National Laboratories)* (LNL) in Italy, which provides the possibility of testing a 48 PMT slice of the JUNO detector. This allows the inspecting of up to 16 GCUs as well as the JUNO dry readout electronics, making it an extremely helpful debugging test platform for new firmware developments.

Such a system would allow to “stress-test” the electronics for a long period of time, potentially leading to show criticalities in both firmware and hardware, before the production stage, where about six thousand boards will be manufactured and mounted. This is a critical step in ensuring that the reliability target for the JUNO electronics (0.5% of defective channels over 6 years) is met.

I have been personally involved in setting up the apparatus, integrating the FEE and BEE. As the dry electronics readout components were not fully developed at the time of this work, I have developed a test firmware for the BEC/TTIM system which accommodates all the required functionalities needed for the foreseen tests, such as timing synchronization and trigger management. The data readout and its analysis has been performed in collaboration with the JUNO Padova group.

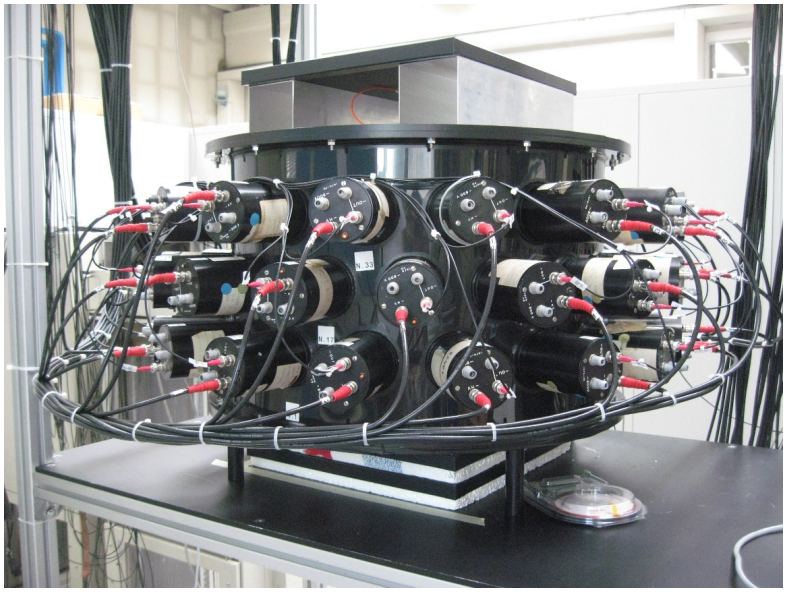

Figure 11.1: The 48 PMTs test system.

11.1 Mechanical design and Geometry

The mini-JUNO detector consists of a two-layer cylinder structure, where the inner cylinder is a transparent 25 cm diameter acrylic vessel, holding the 17 liters of LS. The external layer holds the PMTs in place providing a lightproof cover. The black plastic external cylinder has a diameter of about 75 cm with 48 holes organized in 3 rings with 16 holes each.

The PMTs installed are the 2 inches in diameter Philips XP2020. The HV is provided to the related proprietary commercial bases through commercial CAEN modules. The JUNO HVU have not been used since the detector's PMTs need positive voltage, unlike the JUNO's large PMTs. The choice of the PMT has been driven by the necessity to keep a compact size for the detector maintaining a good linearity, low background noise and good time characteristic.

The QE value of a PMT is expressed as

$$QE(\lambda) = \frac{N_{e^-}}{N_{ph,\lambda}} \tag{11.1}$$

where

- N_{e^-} is the number of emitted photolectrons
- $N_{ph,\lambda}$ the number of incident photons at a specific wavelength
- λ the wavelength

This ratio is not equal to one, since the *photoelectric effect*, responsible to convert the photons that reach the photocatode into photo-electrons, is a stochastic process.

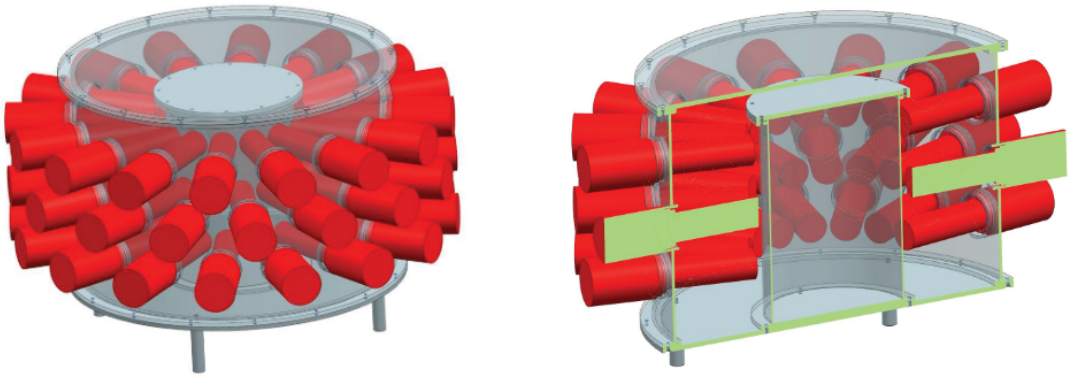

Figure 11.2: Mechanical design of the 48 PMTs system structure. The two-layers cylindrical structure is colored in grey while the PMTs with their respective bases are shown in red.

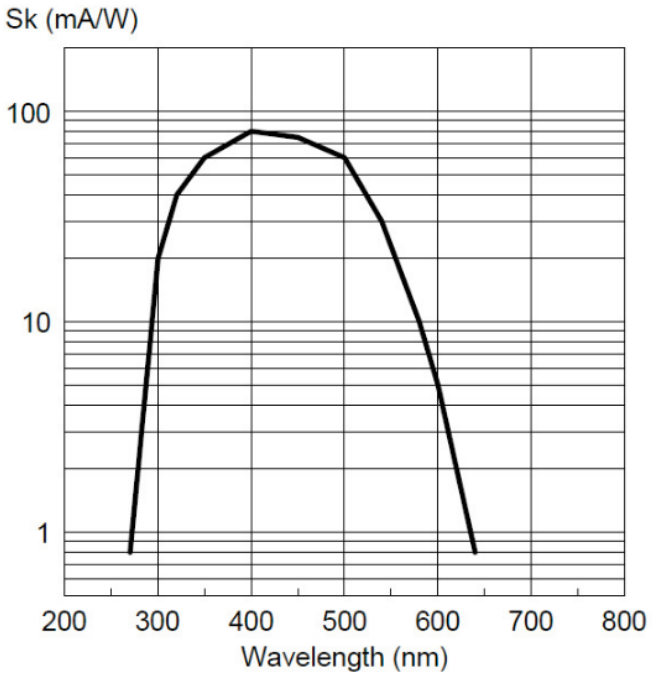

Figure 11.3: Typical spectral characteristics of the Philips XP2020, taken from the datasheet.

Philips XP2020	
Useful diameter of photocathode	44 mm
QE at 400 nm	25 %
Anode pulse rise time	1.5 ns
Signal transit distribution	0.25 ns

Table 11.1: Philips XP2020 reference data.

Fig. 11.3 reports the *radiant sensitivity (S_K)* of the Philips XP2020. S_K is defined as the photoelectric current generated by the photocathode over the incident radiant flux at a given wavelength. The following simple relationship between S_K and QE holds [99]:

$$QE(\lambda) = \frac{S_K}{\lambda} \cdot \frac{hc}{e} \simeq \frac{S_K}{\lambda} \cdot 1240 \frac{W \cdot nm}{A} \tag{11.2}$$

where:

- λ is the wavelength of the incident light
- h is the Planck constant
- c is the speed of light in vacuum
- e is the elementary charge

By fixing the wavelength $\lambda = 420nm$, this leads to a QE $\simeq 0.24$.

Some other reference data for the Philips XP2020 are provided in Table 11.1. The photocathode coverage is about 50%. Mechanical designs of the detector are shown in Fig. 11.2.

The LS contained inside the internal vessel is composed by a LAB solvent doped with PPO and bisMSB, used as a wavelength shifter to match the PMT response; the same formula has been used by the Daya Bay neutrino experiment, with concentrations of 3 g/l of PPO and 15 mg/l of bisMSB [100]. The typical light output is $\sim 10^4 photons/MeV$, with wavelength that mainly ranges from 400 up to 440 nm; the red line shown in Fig. 11.4, at 420 nm, represents the maximum sensitivity of the PMTs in the setup.

11.2 Signal Sources

Several sources can be exploited to induce signal pulses on the PMT. Each source has different features, therefore serving different purposes, guaranteeing a real “in-depth” study on the system and on the electronics.

Some of the sources consist of:

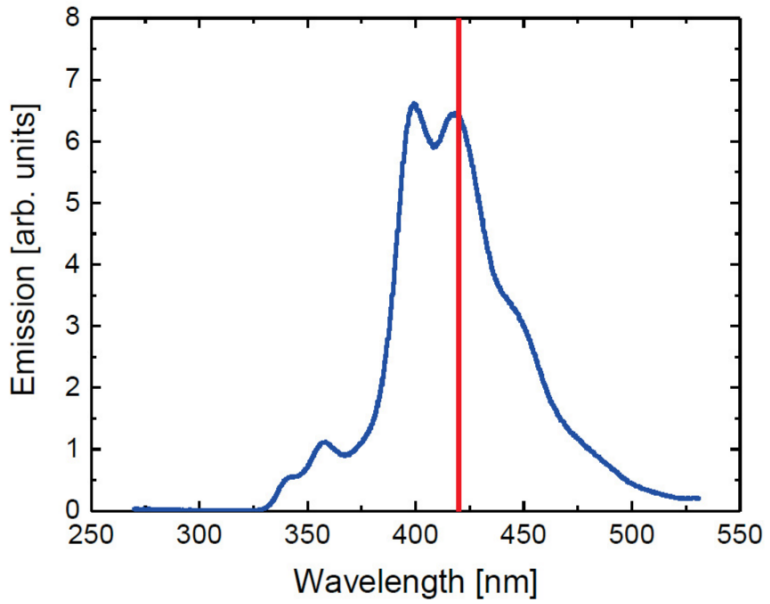

Figure 11.4: Emission spectrum of the LAB scintillator. The maximum sensitivity of the PMTs employed in the LNL detector is represented by the red line at 420 nm. Courtesy of F. Ortica.

- Cosmic muons passing through the inner vessel generate light as they release energy to the LS. To trigger on muons, three plastic scintillators are installed, one on top of the detector and two on the bottom, whose coincidence generates a trigger signal that can be used to trigger the acquisition from the system. The distance between the top scintillator and the one placed below is 52 cm, while the distance between the bottom ones is 3 cm.

- A LED light providing light at 405 nm is used. The LED is kept outside of the system, making its way to the center of the detector inner vessel, traveling inside an optical fiber going through a hole at the center of the top black plastic cover. At the end of the fiber, a light diffuser guarantees the spreading of the photons to avoid “dark zones” inside the vessel. As power supply, a pulse generator is used, giving the possibility to generate pulses with such an amplitude and width that single PE signals are generated by the PMTs.

- A Light Amplification by Stimulated Emission of Radiation (LASER) device has also been installed. Its light can be used in place of the LED, entering the same optical fiber. The power pulses supplied to the LASER device are provided by the commercial LASER pulse generator. Since at minimum power the amount of photons detected by the PMTs is still big, far away from the single PE conditions, a series of interchangeable optical filters are installed as well. Moreover, to precisely monitor the optical power emitted by the laser at different wavelength, a power meter device is used.

For a secure installation, as well as for safety reasons, a “light-box” has been developed, that contains all the LED and LASER equipment. A picture of it together with a schematic overview are

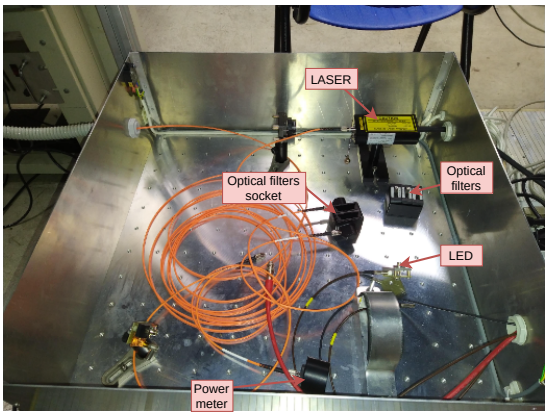

Figure 11.5: Inside of the “light-box”.

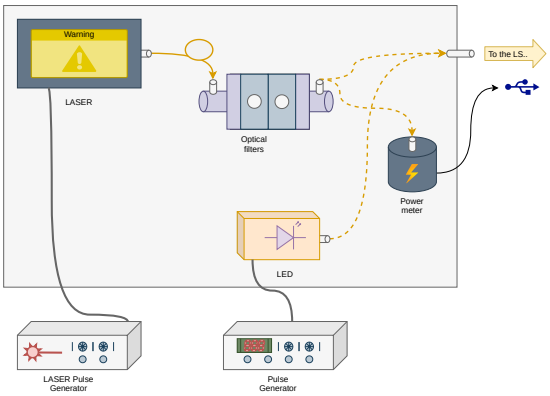

Figure 11.6: Schematics of the “light-box”. Only one of the dashed line are allowed at any time.

visible on Fig. 11.5 and 11.6 respectively.

11.3 Readout Electronics

Fig. 11.7 shows the connections of the 48 PMTs detector with the readout electronics. Being the system main goal to test the JUNO electronics, the readout scheme is similar to the final JUNO detector scheme.

11.3.1 Front-End

An shown in Fig 11.8, GCUs v.2 are mounted inside custom boxes, that allow them to be placed on racks (Fig. 11.9) as well as to stay ventilated. The boxes exposes on the front and back panel all the useful connection to the DAQ and backend electronics (Ethernet and synchronous link, PMTs analogue signal, etc.).

A single rack, consisting of a maximum of eight GCUs, is powered by its own power supply unit, a Keysight N5767A [101], that is LAN connected through the detector Ethernet switch for remote control.

Even though the Xilinx Spartan-6 FPGA on-board grants the possibility to re-program the setup through the network (see Sec. 7.2), an additional JTAG-USB connection from each box with the DAQ server has been foreseen, for a faster FPGA configuration. This is particularly useful when testing new firmware developments, where multiple firmware updates are necessary.

11.3.2 Back-End

The BEE presents some differences with respect to the final JUNO back-end chain. Since the detector has been set up during the electronics development phase, different components were not available or

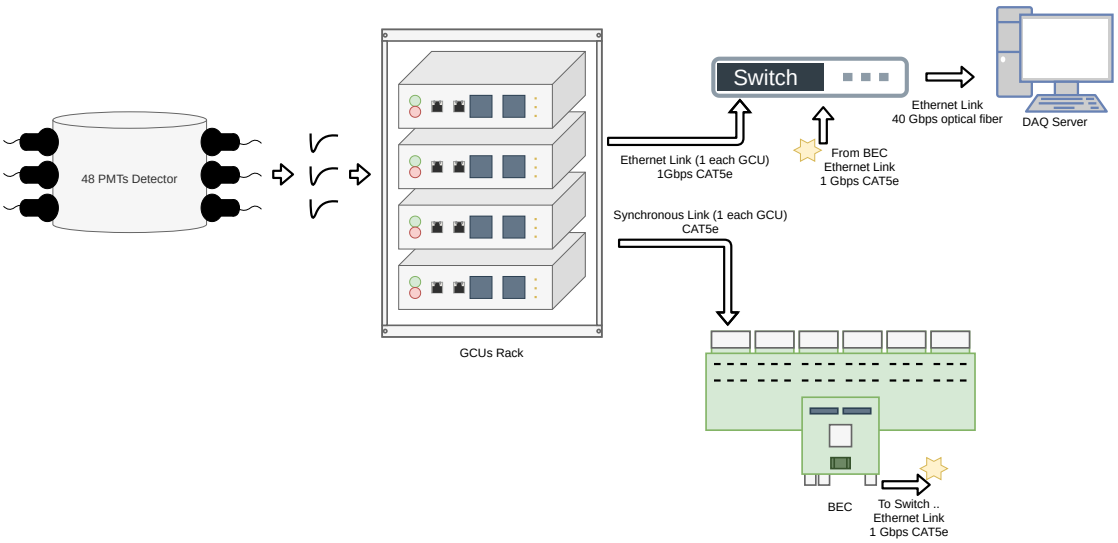

Figure 11.7: The 48 PMTs system and connections.

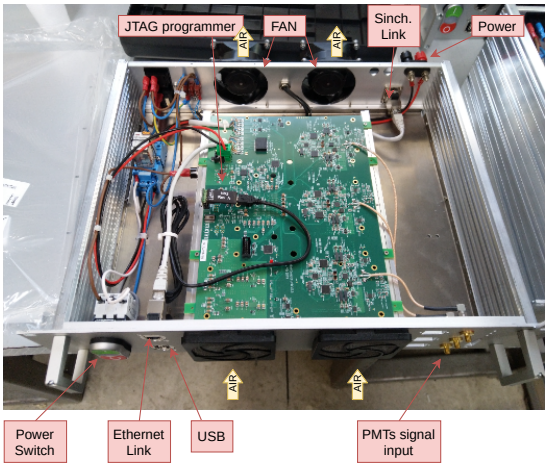

Figure 11.8: Insides of a “48 PMTs system” front-end box.

Figure 11.9: 13 GCUs equipped on two racks at the INFN-LNL.

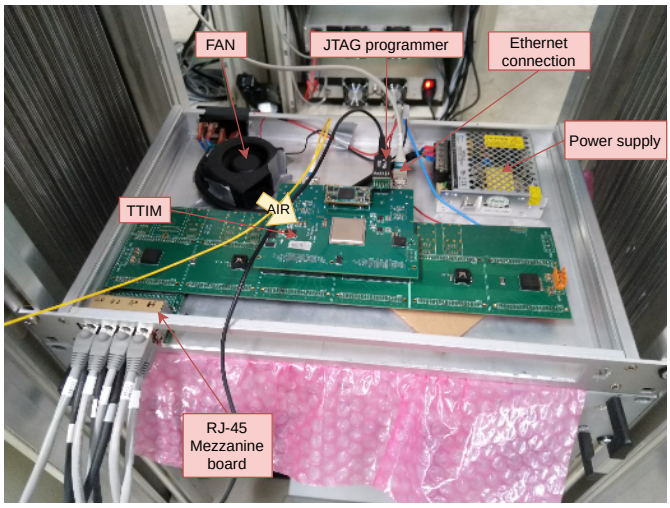

Figure 11.10: A BEC system mounted inside a preliminary box.

not fully functional; therefore the BEE initially included only the BEC and TTIM.

The JUNO electronics group from the *Université Libre de Bruxelles* designed a preliminary box to facilitate the installation of the BEC system into the INFN-LNL rack. As shown in Fig. 11.10, the box allows an easier connection of the RJ45 synchronous link cables.

To make up for the absence of the rest of the chain, a special TTIM FPGA configuration has been developed, which includes all the basic trigger decision functionalities and IPBus connectivity. Fig. 11.11 shows the building blocks concerning the trigger decisioning process on the LNL-detector version of the BEC/TTIM firmware:

1. Trigger requests are received on the back-end. The synchronous link connectivity is used to retrieve triggers from the GCUs while a general purpose SMA connector is dedicated for the receiving of external triggers generated by a pulse generator.

2. In case the trigger comes from the FEE and not from the external trigger, a *trigger multiplicity check* module counts the number of coincidental GCU triggers, comparing them with the *IPBus trigger multiplicity* register value, assigned by the user. If the value is equal or greater, a global trigger validation is issued. An *IPBus trigger mask* register is used to ignore un-connected or faulty GCUs.

3. Through the *IPBus external trigger* register, the user has the ability to switch from external to GCU's related triggers.

4. The *timestamping* module timestamps a trigger, forwarding the information to all the GCUs connected via synchronous link.

Additionally, this temporary backend firmware includes the backend module for the IEEE 1588 synchronization protocol (Sec. 4.3.1), that works in conjunction with the synchronization modules of the frontend boards.

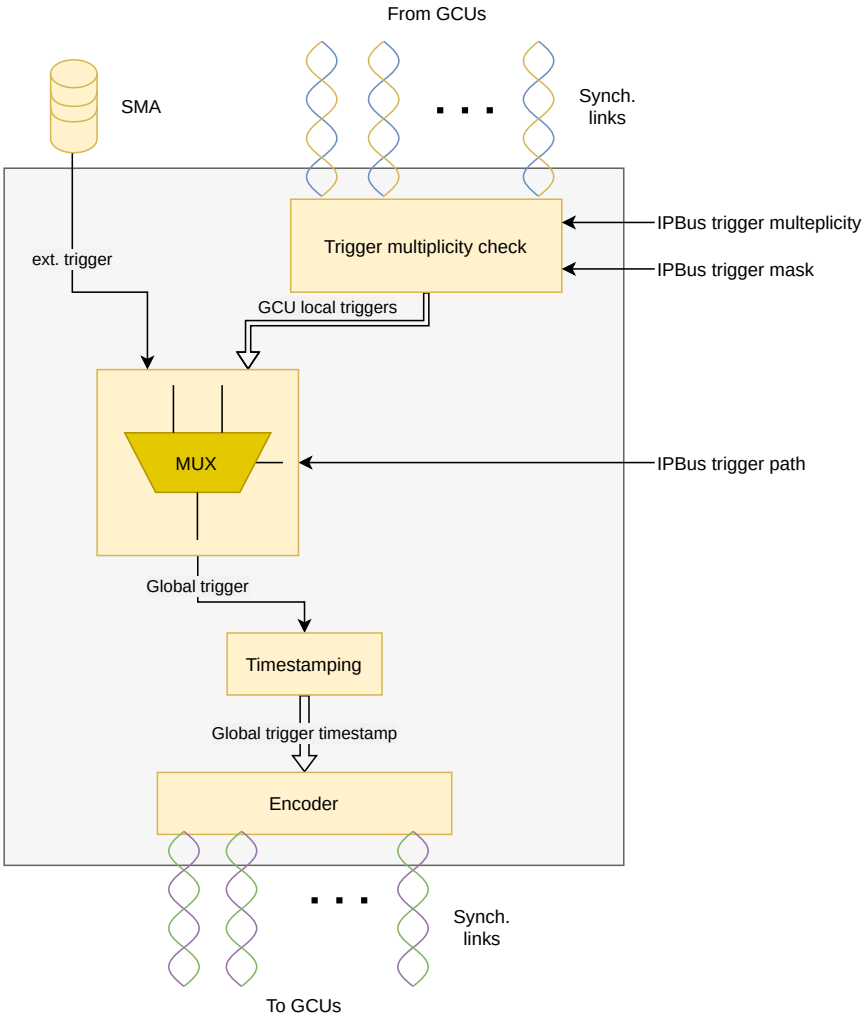

Figure 11.11: Block diagram of the LNL-detector BEC trigger path.

11.4 PMTs High Voltage Calibration

The HV calibration is a needed operation to make sure that gain of the PMTs is fixed. The gain value of a PMT can be extracted from its characteristic peak-to-valley plot by the formula:

$$G(\mu_n, \mu_{pe1}) = \frac{\mu_{pe1} - \mu_n}{e} \tag{11.3}$$

where:

- μ_{pe1} is the mean value of the single photoelectron peak
- μ_n is the mean value of the noise peak (~ 0)
- e is the electron charge

11.4.1 Charge Reconstruction

The energy released in the LS should be proportional to the total PMTs output charge; A single PMT charge should be equal to the following formula:

$$Q_{PMT} = \sum_{i=1}^{N_B} \frac{\Delta t_S \cdot |N_i - B| \cdot 75\mu V}{R} \tag{11.4}$$

where

- Δt_s is the time interval of a single bin, which in our case is equal to *1 ns*.
- N_B is the bin-width of the integrating window.
- N_i is the content in ADC counts of the i-th bin.
- B is the baseline mean value calculated on that single event.
- $75\mu V$ is the voltage corresponding to 1 ADC count.
- R is the termination resistor, which is equal to 50 Ω.

For a simplified analysis, Eq. 11.4 can be written as:

$$Q_{PMT} \propto k \cdot \sum_{i=1}^{N_B} |N_i - B| \tag{11.5}$$

where k is a constant expressed in *Coulomb (C)*. Basically, by using Eq. 11.5, a bin-to-bin sum over the integration window defined by N_B is sufficient to estimate the total PMT's anode output charge. To reconstruct the total charge of a LS event related to the timestamp t, the following Eq. 11.6, should be used, which sums all the single PMTs output charge with this same timestamp in one single value.

$$Q_{TOT,t} = \sum_{i=1}^{N_{PMT}} Q_{PMT_i,t} \tag{11.6}$$

where

- N_{PMT} is the number of active PMTs in the detector.
- $Q_{PMT_i,t}$ is the single PMT's output charge of the i-th PMT in the detector, related to the timestamp t.

To recover the baseline mean value for each waveform, the mean value of the first N_{pre} bins is calculated, where N_{pre} is the number of bins that corresponds to the pre-trigger region, i.e. the time interval that precedes the PMT pulse. The N_{pre} value should be chosen with a certain margin, so that the skew/jitter of the PMT pulse position never affects the baseline computation.

Fig. 11.12 shows how the N_{pre} and N_B values are chosen for the charge reconstruction analysis.

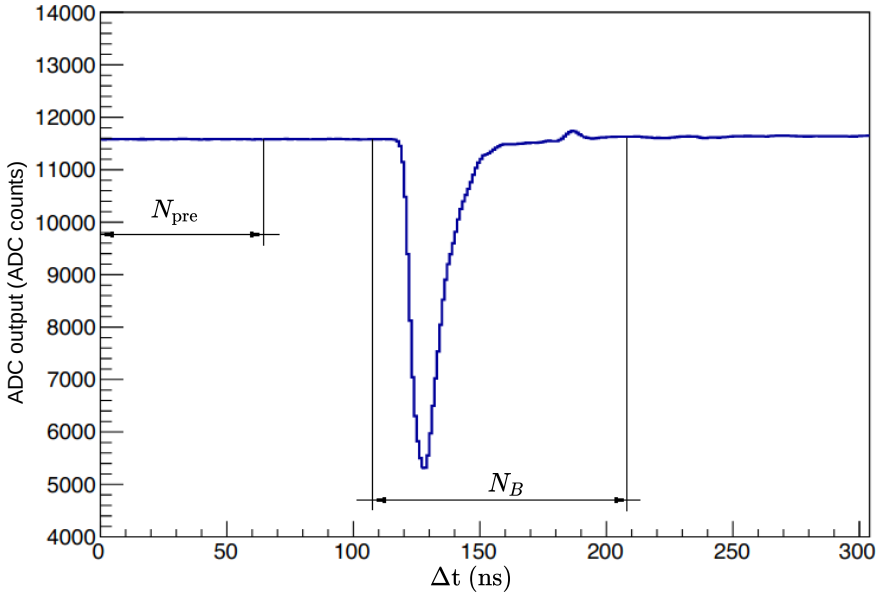

Figure 11.12: Visualization of the N_{pre} and N_B values.

11.4.2 Procedure and Results

On the LNL setup, the capability to observe single PE signals is granted by the LED, which is powered up by an external pulse generator module, as shown in Fig. 11.5 and 11.6.

A typical LED single PE spectrum, with the parameters used in Eq. 11.3 shown, is reported in Fig. 11.13. The parameters μ_{pe1} and μ_n are extracted through a triple Gaussian function fit; two peaks (noise and single PE) are evident, while a third (two PE events) is hinted. The explicit function used is:

$$F(x) = C_n \cdot e^{-\frac{(x-\mu_n)^2}{2\sigma_n^2}} + C_{pe1} \cdot e^{-\frac{(x-\mu_{pe1})^2}{2\sigma_{pe1}^2}} + C_{pe2} \cdot e^{-\frac{(x-\mu_{pe2})^2}{2\sigma_{pe2}^2}} \tag{11.7}$$

For each PMT, single PE plots have been acquired with the HV ranging from 1900 V to 2200 V. Fig. 11.14 shows a typical trend in the single PE distribution varying the HV value. As the HV increase, it is evident that the PMT gain increases as well, as the distance between the noise and single PE peaks increases. The reported charge on the plot has been calculated using Eq. 11.4 and 11.6.

For each PMT of the system, the gain value (Eq. 11.3) for every HV value has been registered. The points have been fitted with both an exponential function. The fit is reported in Fig. 11.15.

After retrieving the needed parameters, a fixed gain value of $2 \cdot 10^8$ has been set on all the PMTs of the system.

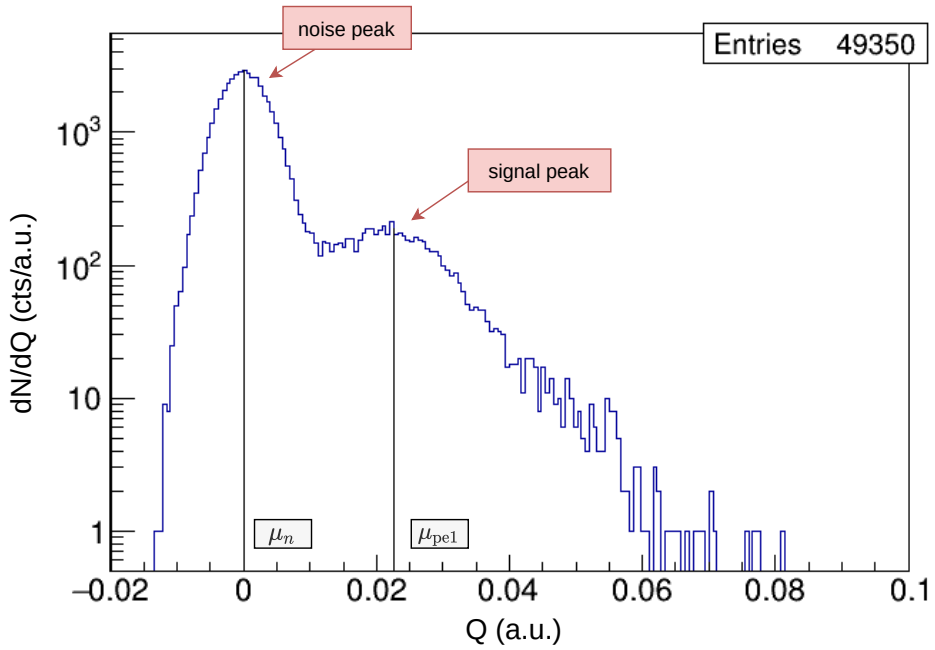

Figure 11.13: LED charge distribution.

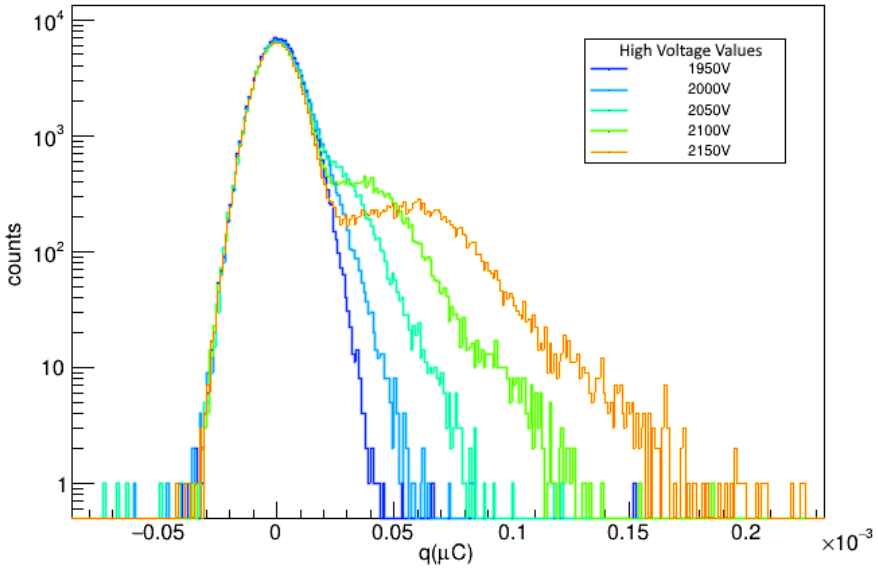

Figure 11.14: Trending of the peak-to-valley plot for different HV values.

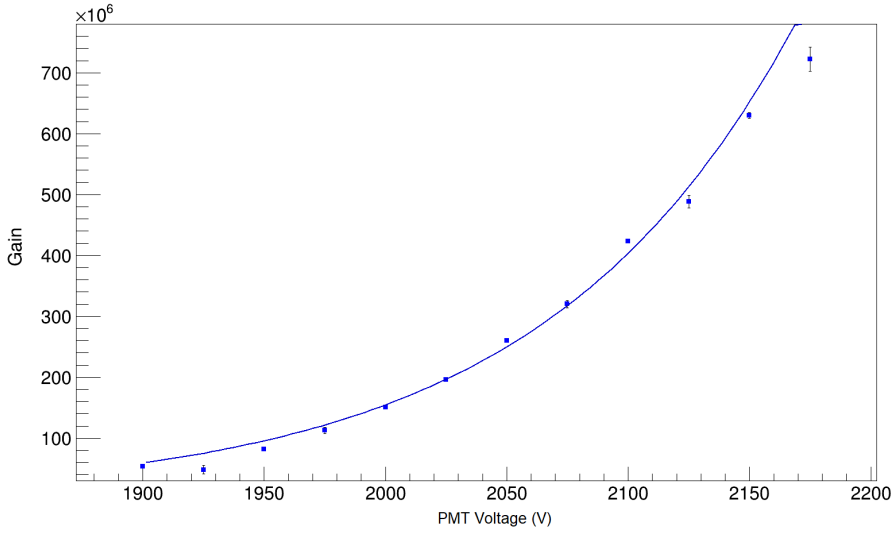

Figure 11.15: PMT gain value versus the PMT HV value.

12

Front-End Characterization

The main objective of the LNL 48 PMTs detector is to test the FEE/FPGA configuration in order to validate its design for the final production and be ready for the commissioning phase of JUNO. As a matter of fact, having a "mini-JUNO" experiment (or, in other words, a *slice* of the entire detector) allows to perform tests that otherwise would not be possible. In particular, the following features have been analyzed:

- The timing synchronization
- The detector readout performances

12.1 Timing Synchronization

The *timing synchronization* test aims to evaluate the frontend-backend synchronization performances, to ensure that the requirements are met.

As explained in Sec. 4.3.1, the IEEE 1588 PTP protocol in ideal conditions guarantees a timing synchronization between global (backend) end local (frontend) clocks inside a ± one clock cycle window. Since the synchronous link protocol rate is 125 Mbps, the synchronization window is ± 8 ns.

A second contribution to a possible timing mismatch between two simultaneous PMT pulses detected on two different channels comes from the usage of the SerDes tile to interface with the ADCs, as explained in Sec. 6.2.2. Since the initialization time of the SerDes is asynchronous, there is no

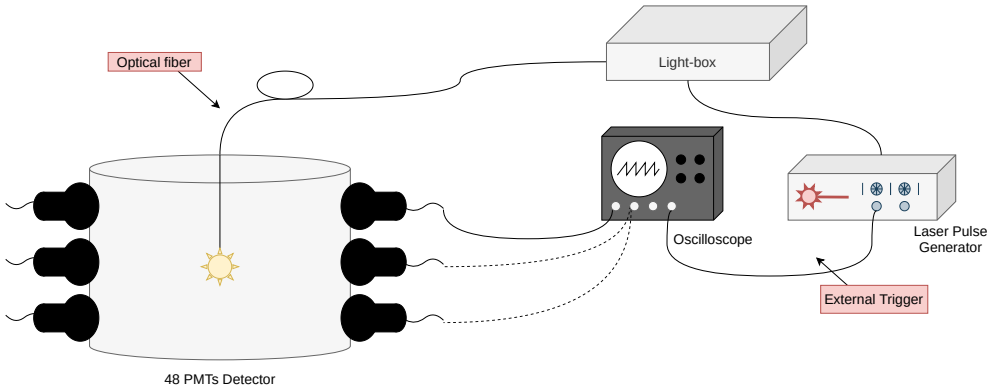

Figure 12.1: Time difference measurements using the LASER. The fixed line is used for the reference PMT, while the dashed line is connected to one different PMT for every measurement.

guarantee that ADC words on the same spot in the "8 words output vector" of the SerDes, corresponds to ADC words received at the same time.

Both of these factors introduce a synchronization uncertainty of 16 ns. While the latter is always present, the first one only affects channels on different GCUs. Therefore the timing mismatch should be:

- Up to 16 ns for same GCU channels.
- Up to 32 ns for channels residing on different GCUs.

To evaluate the timing synchronization and mismatch between GCU channels, the 48 PMTs setup at LNL has been used. The signal source employed for the test is the laser light; a choice mainly driven by its timing performances.

The light diffuser placed at the center of the detector vessel should guarantee that all the PMTs in the system are hit by photons at the same time, a necessary requirement to run the test. To ensure this, the time difference between LASER PMT pulses on different channels has been measured using an oscilloscope, keeping one channel fixed for reference. To avoid dark-noise related pulses, an external trigger provided by the LASER pulse generator is used; the setup is illustrated in Fig. 12.1. Fig. 12.2 shows the oscilloscope screen of a typical time difference measurement. The time-offsets with the reference PMT range from -1 ns to about +2 ns, which can be considered negligible for the sake of the test.

The test setup for the GCU acquisition has been shown in Fig. 11.7, with the BEC set in external trigger mode, connected to the external trigger output of the LASER pulse generation. The acquisition is therefore triggered only when the LASER is emitting light, ignoring dark-noise pulses. By setting the GCUs in *global trigger mode*, each time the laser emits light, the correlated timestamp is received from the BEC via synchronous link as a global trigger validation, defining the start of the event. If the GCUs were perfectly synchronized to the nanoseconds, the pulses on acquisition windows of different channels would overlap; in reality, an offset is present, due to the aforementioned motivations. Fig. 12.3 shows a typical histogram of these time offsets between two channels.

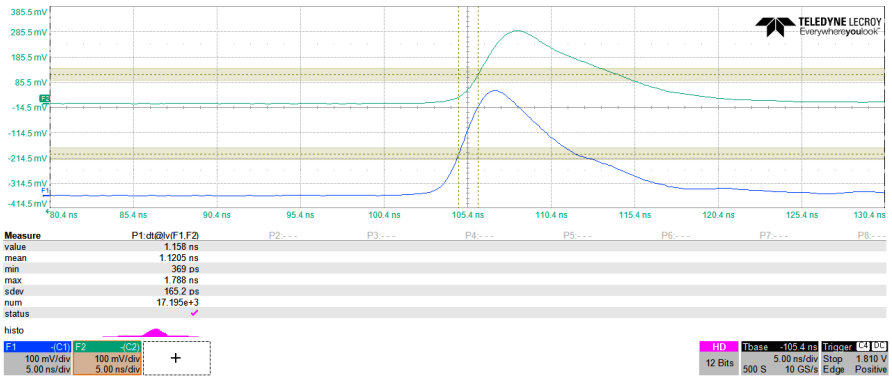

Figure 12.2: Oscilloscope screen of a typical time difference measurement using the LASER.

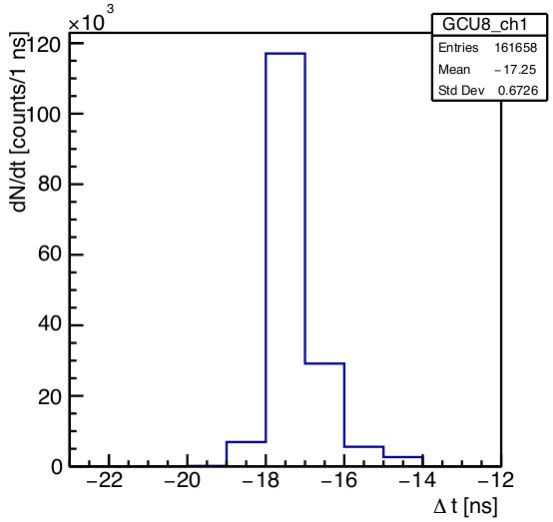

Figure 12.3: Typical histogram of time differences between different channels acquired from different GCUs using the LASER source.

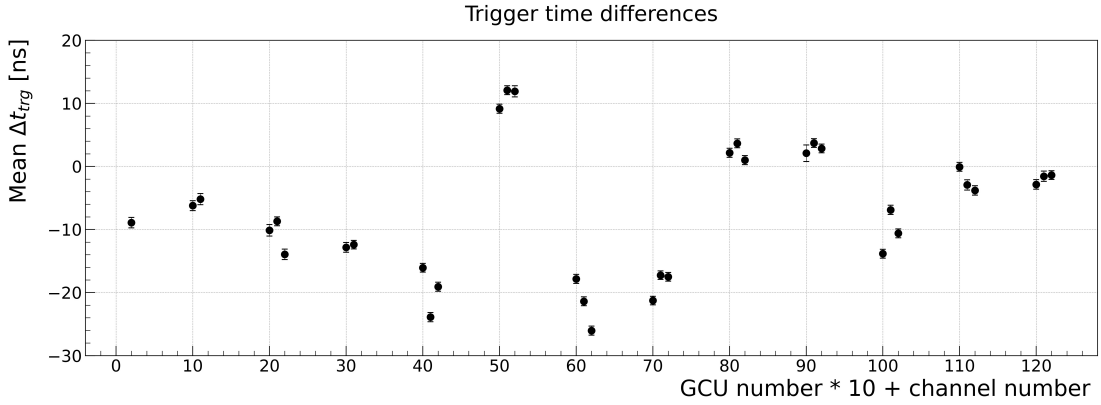

Figure 12.4: Average time differences using the LASER source for the different channels available.

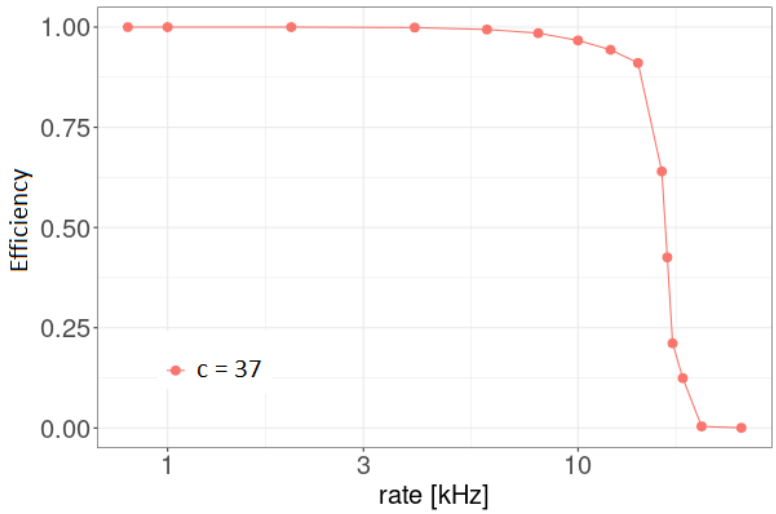

Figure 12.5: Efficiency of the 37-channel readout. The efficiency value refers to Eq. 8.6, with $c = 37$.

Ideally, the average time difference between channels must not exceed 32 ns. All the average time differences for the different channels are shown in Fig. 12.4. The values range from +12 ns to -26 ns, which sum up to 38 ns. The maximum value of 32 ns is exceeded by about 6 ns, and this is likely to be due to the asymmetry of the Cat-5E twisted pairs, which worsen the time synchronization performances of the IEEE 1588-2008 PTP protocol, as explained in Sec. 4.3.1.

12.2 Detector Readout Performances

Testing the readout performances of the whole LNL detector is needed to better understand the ControlHub and μHAL library efficiency on the acquisition server side.

The test falls into the *n-to-1 polling* scenario described in Sec. 6.2.4.1, with $n = 37$ in this case (13 GCUs $\times$ 3 Channels $-$ 2 broken ADUs). The same acquisition parameters of the "single GCU trigger rate test" (Tab. 8.3) has been set, in order to have a direct comparison.

The test setup is described in Sec. 11.3. The BEE has been set to *external trigger mode*, connecting a pulse generator output to the SMA input of the TTIM card (see Fig. 11.11). Using an external pulse generator the event rate can be set very easily, with frequencies up to several MHz.

Concerning the acquisition server, a preliminary version of the JUNO DAQ software has been used, being developed by IHEP colleagues. To avoid efficiency loss due to external factors, the acquired data is stored on a RAM disk rather than the hard drive.

The results shown in Fig. 12.5 are expressed in terms of Eq. 8.6, with the parameter $c = 37$. As shown, the efficiency starts to drop at $\sim$10 kHz acquiring data windows of 384 ns, which equals to about 50 Mbps per channel (150 Mbps per GCU, 1.8 Gbps total). The total throughput is about half of the single GCU throughput reported in Sec. 8.5.2.

Most likely, the bottleneck comes from the CPU load as it closely reach the 100% busy time. More

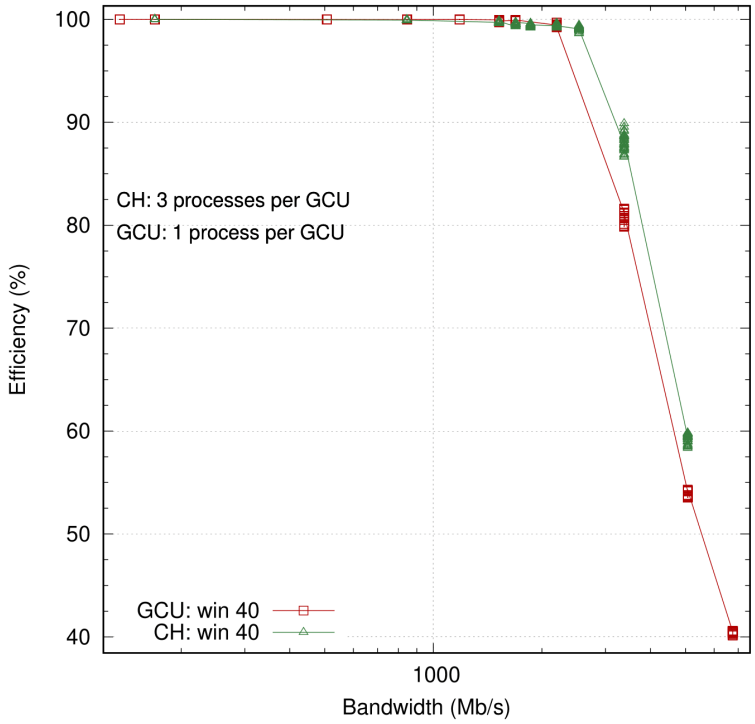

Figure 12.6: Efficiency of the 37-channel readout computed for each single channel independently. The green triangles refers to the "single channel per DAQ script" architecture, while the green squares corresponds to a "single GCU (three channels) per DAQ script" readout.

than half of the CPU time occupation is caused by the ControlHub, whose load strongly depends on the number of μHAL clients it needs to manage.

Although being the most flexible solution, the test results show that the "one μHAL client per channel" configuration is not CPU efficient and it is maybe not feasible when 20'000 channels are readout. Therefore a trade-off between flexibility/performance and CPU load efficiency will have to be considered. The most straightforward modification to the acquisition script that would reduce the number of μHAL clients maintaining its flexibility is using a single script to read the three channels of a GCU. In this case the DAQ would perform three block transfers, one for each channel, and concatenate them in a single IPBus transaction (see Sec. 6.2.4.1). This approach has been tried on the LNL setup, and the results are visible on Fig. 12.6. In this case no event building has been used, and the efficiency of every single channel has been retrieved using Eq. 8.5, converting the event rate to bandwidth thanks to Eq. 8.4 .

While the new DAQ concept did not outperform the old, the CPU load was significantly reduced. The slight efficiency drop is likely to be caused by the serialization of the three channels readout, instead of parallelizing the task to different cores.

Since the final JUNO event rate is estimated to be in the order of hundreds of Hz, the performance of a single GCU readout is not to be worried about, and the above-mentioned trade-off could be

focused on the CPU load efficiency, reading several GCUs in a single script, therefore reducing the ControlHub burden and accommodate the readout in a reasonable amount of DAQ servers. In addition, different architectures could be tested, for example dedicate a number of server only to accommodate the ControlHub software, and use the rest for the acquisition script; such "role division" is possible with IPBus, as explained in Sec. 6.2.4.

12.3 DDR3 Trigger Rate Test

Being the reason of employing the DDR3 memory to be able to sustain higher trigger rates, a trigger rate test is mandatory in order to assess the limits of what a GCU, and JUNO itself, can observe. The interface for the DDR chip has been implemented in FPGA with a frequency of operation of 400 MHz, which equals to a data rate of 800 MT/s. Being the transfer unit 16 bit, the bandwidth is capped at 12.8 Gbps, but this value must be multiplied by the DDR bandwidth efficiency in order to retrieve the real value.

The bandwidth efficiency of a DDR SDRAM memory chip is conditioned by several factors, both from its application (a drop in bandwidth efficiency occurs when the DDR controller repeatedly switches between reads and writes operations) and from the memory itself (DDR memory refresh). The bandwidth efficiency value can span from about 10% to about 90% [102].

The setup used to test the GCU's DDR3 SDRAM memory bandwidth efficiency as well as validate and test the performances of the *complementary DDR readout* data path described in Sec. 7.1.2, is shown in Fig. 12.7. The LASER light source is employed to trigger the transfer of data windows to the DDR memory chip. The LASER pulse generator is used to control the frequency of the light pulses while a specific threshold is set on the firmware in order to avoid dark noise.

Similarly to the trigger rate test of Sec. 8.5.2, the DDR readout path efficiency is computed by the following equation:

$$Efficiency = \frac{\#\ of\ acquired\ events}{\#\ of\ trigger\ sent} \tag{12.1}$$

The results are reported in Fig. 12.8. The efficiency starts dropping at a rate of 1.5 MHz, which translates to a 9.6 Gbps throughput considering a data window of 400 ns is set for the DDR acquisition. This equals to a DDR bandwidth efficiency of 75%.

Such results validate the *complementary DDR readout* path and grant the GCU with the ability to acquire SN events efficiently, allowing JUNO to extend its physics program including SN studies.

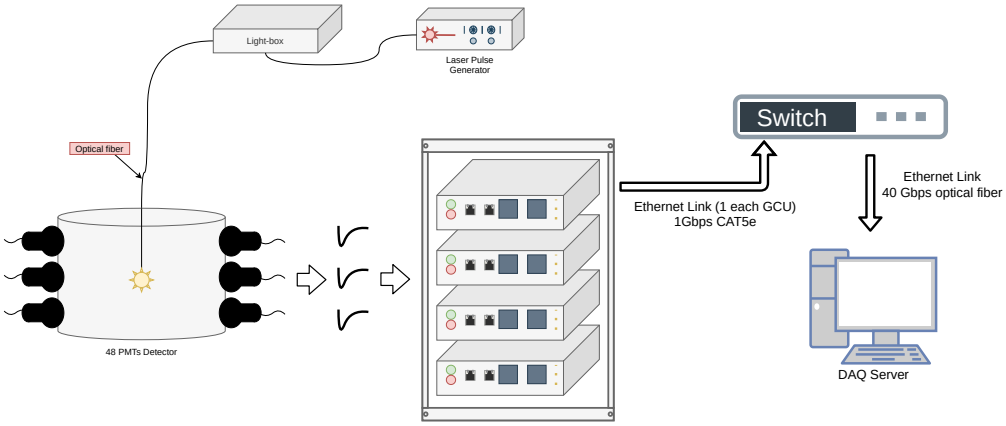

Figure 12.7: LNL detector setup for DDR3 trigger rate test. The BEC is not shown as it is only used for clock distribution and not trigger.

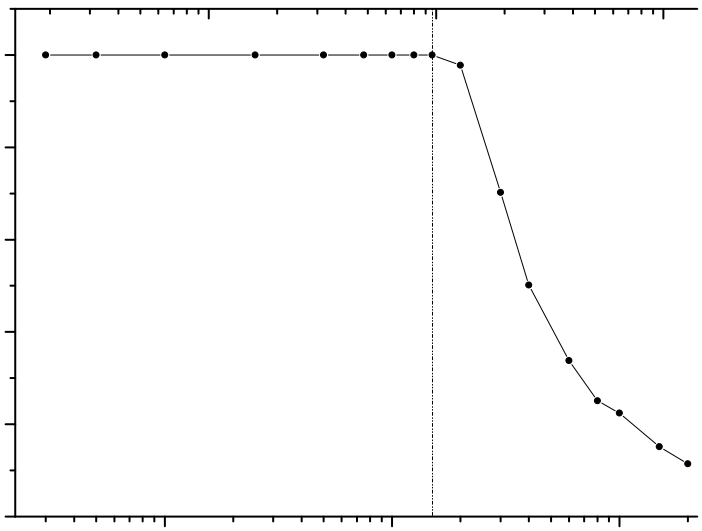

Figure 12.8: *Complementary DDR readout* path efficiency.

13

Detector Energy Calibration

For an overall testing of the JUNO front-end readout electronics, an energy calibration of the setup has been foreseen. The simplest way to calibrate in energy the response of the experimental setup is through the usage of radioactive sources with a simple and well-known decay scheme.

The radioactive sources employed for the energy calibration of the detector and their respective, most intensive, gamma energies are reported in Tab 13.1. The sources have been placed on top of the detector, using a lead collimator, as shown in Fig 13.1.

13.1 Preliminary Simulations

In order to set the ideal trigger conditions, Monte-Carlo simulations have been performed for the setup response to the radioactive-sources.

A first simulation has been performed to compute the optimal trigger multiplicity value to set on

Caesium-137	661.7 keV
Sodium-22	1.274 keV
Cobalt-60	1.1732 MeV/1.3325 MeV

Table 13.1: Radioactive sources used for energy calibration of the LNL setup and their respective principal gamma energies.

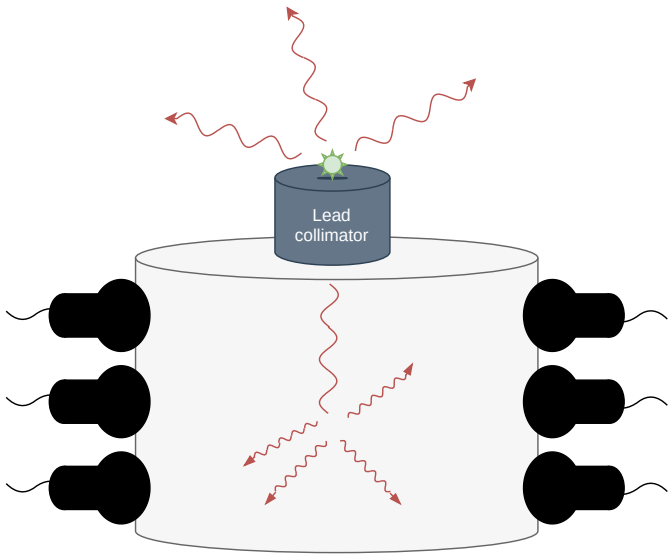

Figure 13.1: The LNL detector setup using radioactive sources.

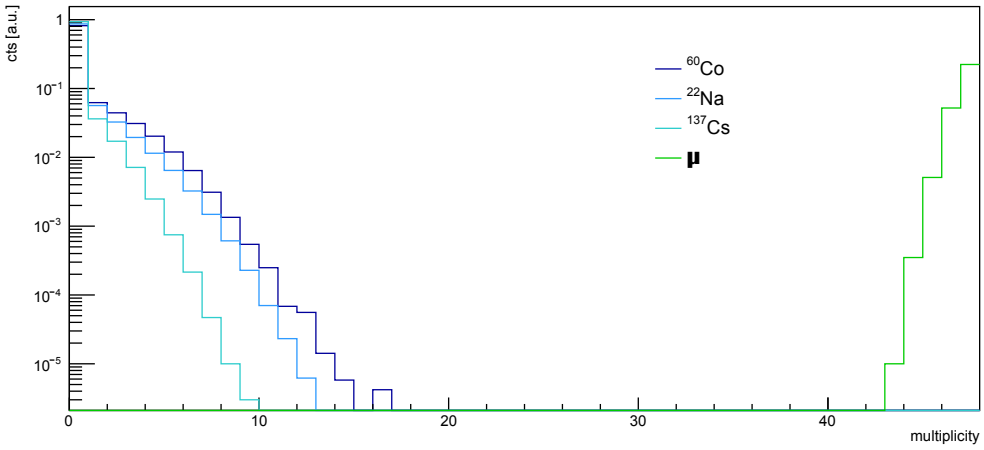

Figure 13.2: Multiplicity simulation for radioactive sources collimated events as well as cosmic muons.

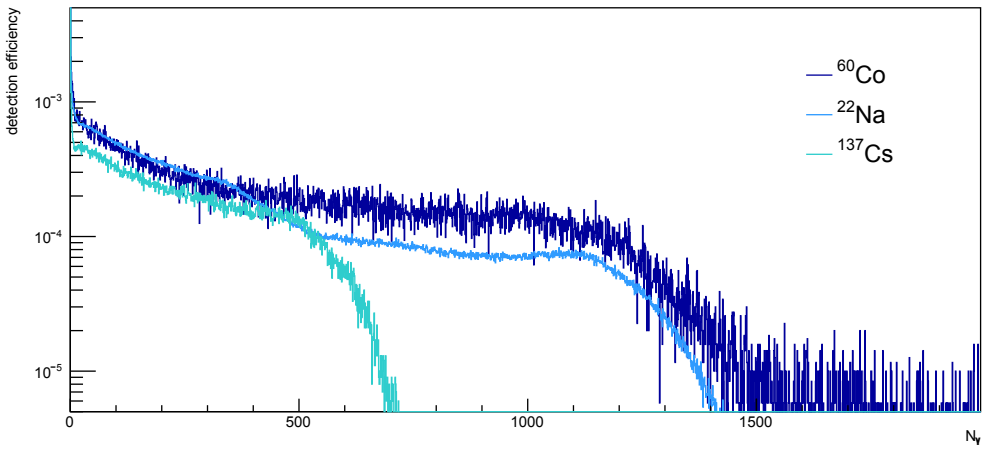

Figure 13.3: Simulated distributions of the number of photons absorbed by the PMT photocathodes with collimated sources.

Run time	15 minutes
PMT multiplicity trigger:	3
GCU local threshold	6 baseline standard deviations from the baseline value.

Table 13.2: DAQ parameters for energy calibration acquisitions.

the BEC level in order to avoid most of the uncorrelated signals, such as PMT dark noise induced events. The results of such simulation are shown in Fig. 13.2.

Fig. 13.3 is a Monte-Carlo simulations concerning the number of photons N_γ impacting on the PMT photocathodes, with collimated sources. By assuming a fixed, single waveform of the photons, N_γ is proportional to the energy released in the LS and, consequently to the total PMTs output charge (Eq. 11.6).

The two simulations illustrate a peculiarity of the detector: due to the small amount of active mass of LS for the LNL-detector in combination with its characteristic density, the gamma rays are not able to release their full energy, escaping early from the detector. Therefore the setup energy calibration is based on the Compton continuum only, due to the absence of the full-energy peaks. The relationship between the gamma energy E_γ and the correlated Compton edge value $E_{e,\max}$ is the following:

$$E_{e,\max} = \frac{2E_\gamma^2}{2E_\gamma + m_e} \tag{13.1}$$

13.2 Acquisition Results

The acquisitions parameters are summarized in Tab. 13.2.

A first acquisition has been performed without the presence of any radioactive sources, in order to

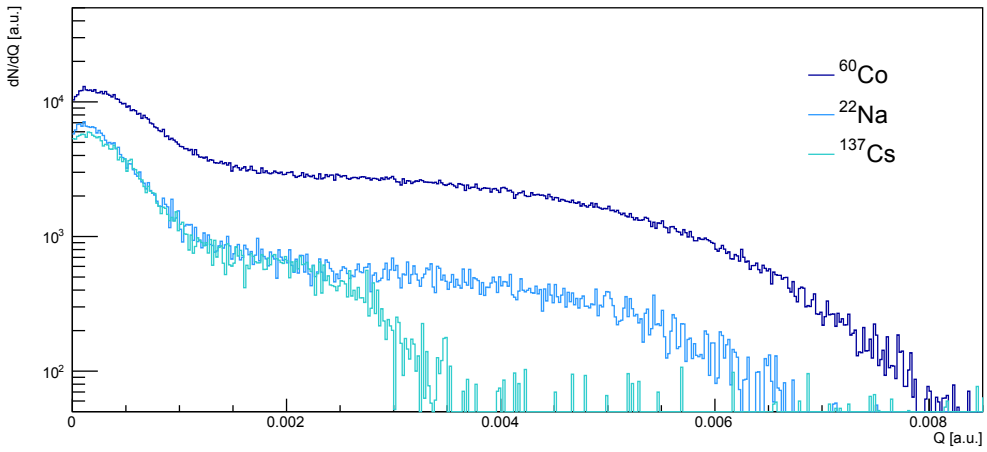

Figure 13.4: Experimental radioactive sources spectrum subtracted of the background.

determine the background contribution to the data. Contribution to the background may arise from residual light penetrating into the detector and environmental radioactivity.

Subtracting the background spectrum from the radioactive sources spectra, the plot in Fig. 13.4 is produced. Since the actual value for the PMTs output charge has no need for the energy calibration procedure, Eq. 11.5 and 11.6 are used for simplicity, ending up with a value proportional to the real charge value expressed in *Coulomb*. Good agreement is noticeable between the experimental measurements and the simulation plot in Fig 13.3.

Emerging from the comparison, the distribution curves on the Monte-Carlo plot in Fig. 13.3 present sharper edges. The reason is likely to lie in the finite energy resolution of the experimental setup, that is not taken into account for the simulations. A comparison between different energy resolution simulated spectra for the collimated ^{22}Na source has been produced and shown in Fig 13.5. The plot indicates that, by using the *smearing* procedure and therefore emulating the finite resolution of the system, the simulated plots resemble the experimental ones.

13.3 Energy Calibration Procedure and Results

To perform the energy calibration fit, the positions of the Compton edges has been extracted using the complementary error function (Erfc) [103].

The energy calibration linear fit between the experimental Compton edges values and the theoretical values is plotted and reported in Fig. 13.6.

13.4 Energy Calibration on Cosmic Muons Spectrum

Charge reconstruction on cosmic muons data has been performed, in order to compare and have a better interpretation of the calibration data.

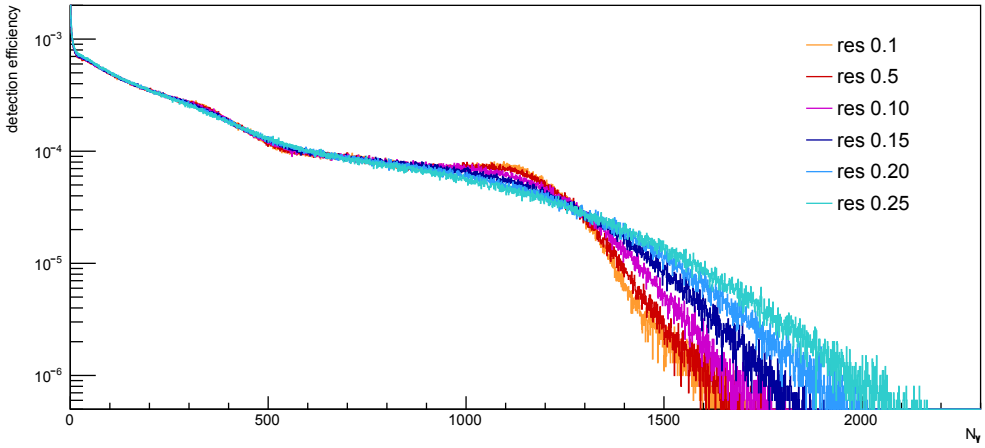

Figure 13.5: Smearing procedure applied to the original simulation of the collimated ^{22}Na energy distribution. R defines the standard deviation of a Gaussian distribution for which each *un-smeared* bin has been substituted with. The relationship is $\sigma = x_i \cdot R$ where x_i correspond to the bin central value.

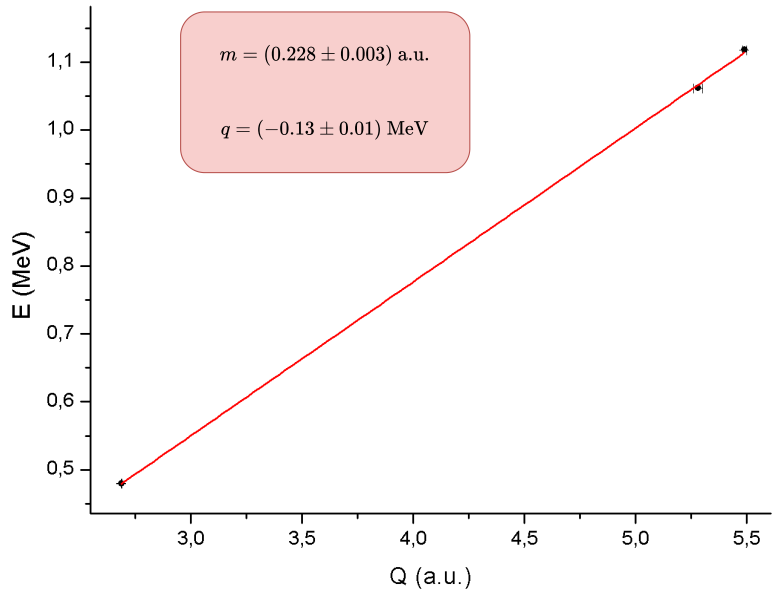

Figure 13.6: Energy calibration fit.

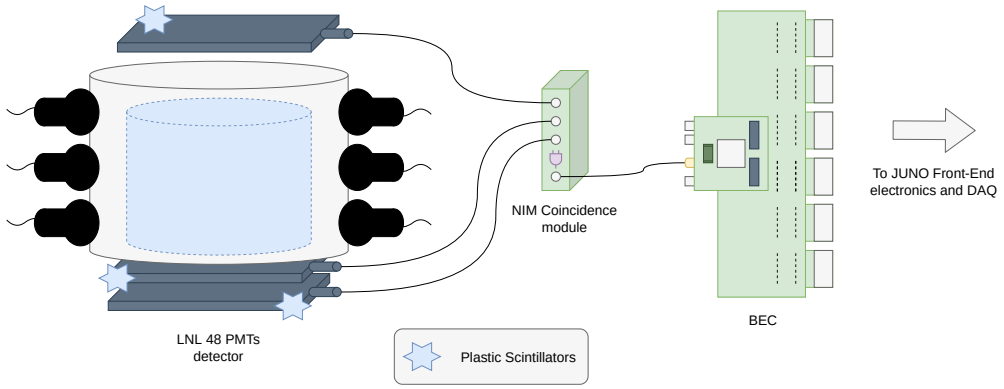

Figure 13.7: Experimental setup for cosmic muons acquisition.

13.4.1 Experimental Setup

Fig. 13.7 illustrates the experimental setup to perform a cosmic muons acquisition run. The three plastic scintillators placed on the top and on the bottom of the LS detector are connected to a Nuclear Instrumentation Module (NIM) module that returns the logic AND of the three signals. This coincidence signal is connected to the SMA connector of the BEC and used to externally trigger the acquisition of the system.

This architecture guarantees that the acquired signal are generated from cosmic muons, avoiding the acquisition of PMT pulses generated by external light or environmental noise.

13.4.2 Simulation and Results

A Monte-Carlo simulation for cosmic muons vertically entering the LNL-detector has been performed. The expected energy distribution profile that should be returned from the detector is shown in Fig. 13.8. The extraction of the curve's parameters, such as its centroid value, a fit with the *Landau* function is performed. Both the simulation and the acquisition take into account muons with a vertical direction (for the experimental setup, this is guaranteed by the placement of the plastic scintillators), therefore the two distribution should be in good agreement.

The experimental energy distribution acquired with cosmic muons is shown in Fig. 13.9. The curve is fitted using the *Crystal Ball* function [104, 105]. The energy values on the x-axis are retrieved using the energy calibration provided by the radioactive sources. It is noticeable how the Most Probable Value (MPV) for the simulation (59 ± 3) is perfectly compatible with the centroid value of the experimental distribution (59.57 ± 0.02).

Including the cosmic muon measurement in the plot of Fig. 13.6, Fig. 13.10 is returned, showing perfect agreement.

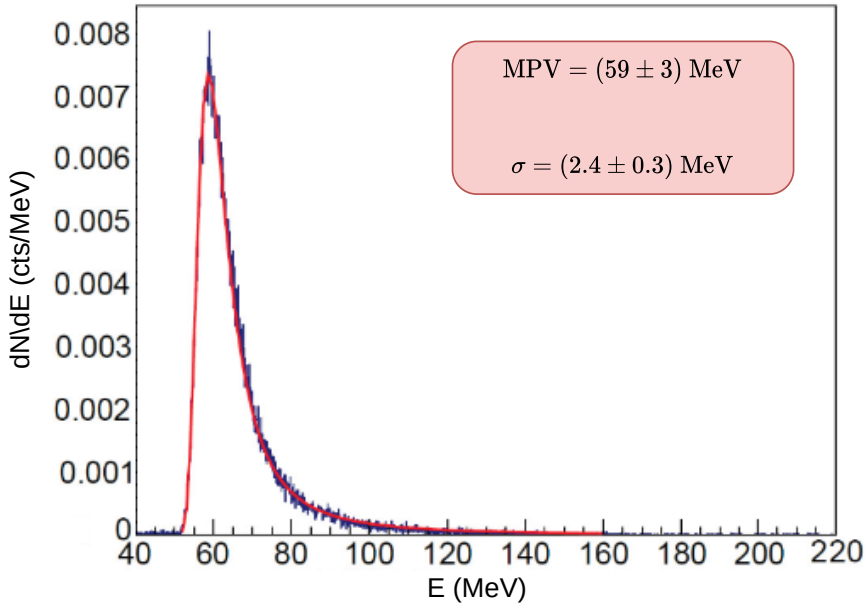

Figure 13.8: Simulated energy spectrum for cosmic muons on the sea level, with vertical direction. The red line is the *Landau* function fitting.

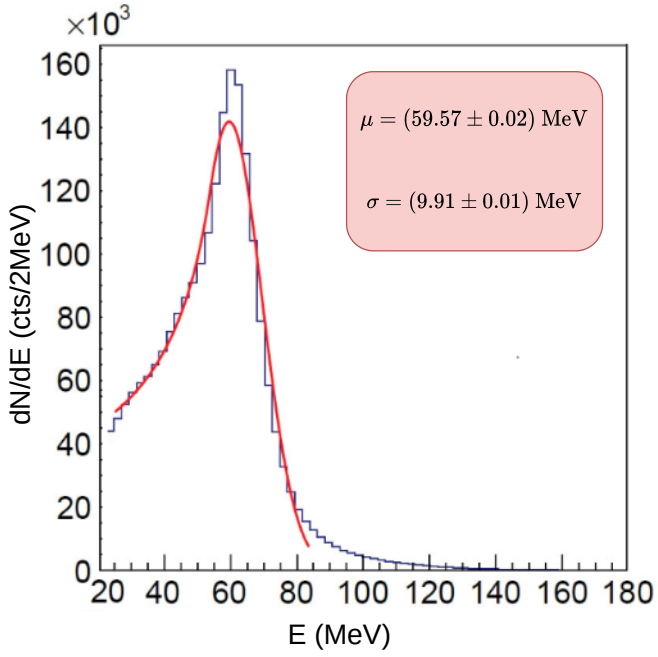

Figure 13.9: Experimental energy spectrum for cosmic muons. The red line is the *Crystal Ball* function fitting.

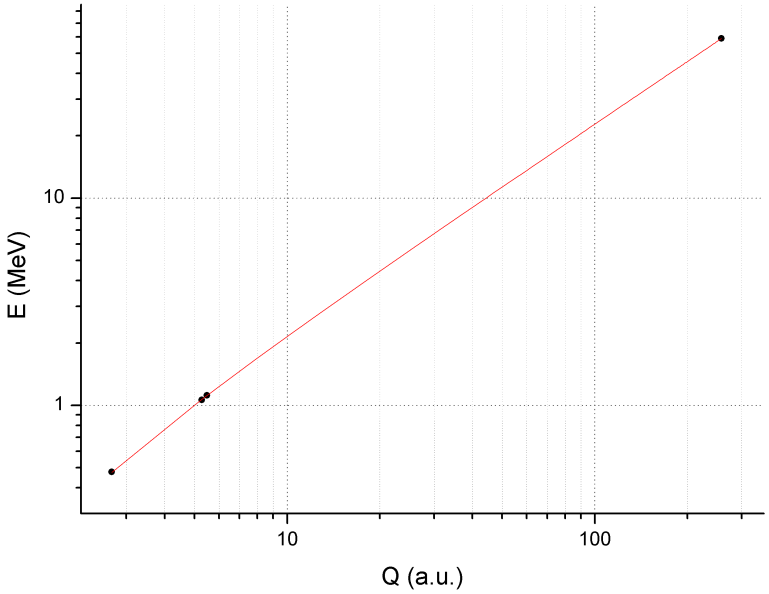

Figure 13.10: Energy calibration points including radioactive sources and cosmic muon measurements. The red line represents the linear fit using only radioactive sources.

Part IV

Conclusions

14

PhD Results and Conclusions

14.1 GCU Characterization and Firmware Development

My work on the GCU's characterization provided measurements and analysis in order to ensure that the board's reliability and performances fall within the experiment's requirements. In particular, the analysis I performed on the overall GCU FIT value ensured that the target of less than 0.5% of channel failures due to electronics failures is met, provided that the operating environment temperature of the UWB plateaus below a certain value. I have also validated the communication links of the board, performing the signal integrity analysis on the custom synchronous link as well as assessing the throughput performances of the Ethernet link employing IPBus as the transport protocol. These series of test were of crucial importance as the board was heading to the final production stage.

Most of my PhD work has been dedicated on the FPGA firmware development, implementing the features foreseen for the JUNO FEE. I have been responsible for:

- **Pulse-shape processing for trigger requests**

  The technique implemented in FPGA, is a pulse-shape processing trigger primitives generation algorithm, aiming for an improvement in the detection of small amplitude PMT pulses [80]. Based on the results reported in Sec. 7.1.5.4, the core has been successfully developed and implemented in FPGA. Furthermore, tests were performed employing a JUNO large PMT, where a simple leading edge trigger, implemented in parallel, has been outperformed in trigger efficiency. The proposed algorithm is to be implemented in the JUNO GCU's final FPGA firmware and will be crucial for reaching the target energy resolution.

- **The synchronous link protocol**

  The synchronous link is custom, deterministic, low-latency bidirectional communication link between the FEE and BEE, responsible for the timing and trigger system. Running on a Cat-5E cable, employing a cable driver and receiver for link equalization and a CDR for clock recovery purposes, the protocol is based on the CERN's TTC project. During my work, I have ported and adjusted the link protocol firmware from a prototype version developed for a former JUNO FEE architecture, to the present GCU board. The link has been characterized (Sec. 8.4) with a BER test and an eye diagram analysis, and the results are a strong indication for the link reliability, featuring a wide open eye and excluding a BER higher than 10^{-12} (standard for data transmission over fiber optics and Ethernet channels) with a CL of 95%.

  During the course of my PhD, the GCU did undergo a major upgrade (Sec. 9), forcing the necessity of a complete synchronous link re-design, mainly driven by the absence of the CDR chip. I have successfully adjusted the synchronous link protocol to the new architecture, as well as developed a new link calibration procedure.

- **FPGA implementation of a CDR**

  As explained in Sec. 10, the synchronous link architecture after the GCU upgrade is potentially affected by EMI, resulting in loss of timing synchronization between the FEE and BEE. To avoid such issue, I have developed an FPGA implementation of a CDR [90, 94], allowing the link architecture to resemble the pre-upgrade scheme. Taking into account the reported results, consisting in an improved EMI immunity improvement, wide-open eye diagram and a BER higher than 10^{-12} rejected with CL of 95%, the usage of the new CDR scheme by JUNO in the GCU's FPGA would bring the following advantages to the synchronous link communication:

  – Robustness, in terms of avoiding loss of clock locking in the presence of short EMI.

  – Features, by freeing a twisted pair in the cable, previously dedicated to clock forwarding.

  However, the main limitation of this project is the mandatory loop-back for the NCO's output clock, due to the usage of the SerDes tile, which can only connect to an IOB. As mentioned above, a small modification on the PCB would therefore be required. Nevertheless, if such core would be necessary to be employed after production, further development can be put in place to avoid the use of a SerDes, exploiting a delay-line to generate a clock signal directly within the FPGA [106] instead of the present architecture, for instance.

- **The complementary DDR readout**

  An additional data path alongside the online *default readout*, the *DDR readout* path is essential to provide JUNO with the ability to perform SN research studies. In case of a SN burst, the event rate inside the CD undergo a sudden, vast increase. By storing this huge amount of data in an external DDR3 chip on-board instead of the internal FPGA memory, the GCU is able to cope with a significantly higher event rate. Before the development of the *DDR readout* path, I have successfully validated the hardware PCB design, in order to guarantee an error-free data

transmission in writing and reading from the memory bus (Sec. 8.6). Subsequently, I have tested the performances of the DDR readout path (Sec. 12.3), assessing a maximal bandwidth of 92.6 Gbps, corresponding to a DDR memory bandwidth efficiency of 75%. It is still unclear what the minimal requirements for the DDR acquisition are for JUNO, but nevertheless the test validates the firmware development for the *complementary DDR readout* data path described in Sec. 7.1.2. If the performances are not sufficient, a change in the DDR operating frequency is possible, doubling it from 400 MHz to 800 MHz. Moreover, optimization on the data path is also achievable.

As previously mentioned, the inclusion of the external DDR3 memory to the JUNO FEE allows the extension of the JUNO physics program to SN studies. Without the development of the *complementary DDR readout*, most of the SN events would be lost, together with the potential information that those events carry along.

Upon arrival of the first UWB, I have been involved with a deep-water test, to ensure no damage has occurred during transportation and perform several measurements, particularly focusing on the temperature. The box has been placed about 40 m underwater for about 30 hours. During this time, the FPGA temperature has been recorded, showing a die-water temperature difference of about 23 °C. These measurements are crucial in order to precisely compute the boards expected life time, matching the GCU FIT value to the final operating temperature in JUNO.

The successful firmware developments described in this work together with their correlated tests and results, ensures the suitability of the GCU board as the main component of the JUNO FEE readout system, satisfying the necessary requirements in terms of FIT value, data readout performance, ability to cope with SN bursts events and provide a stable timing and trigger system.

14.2 The JUNO Readout Electronics Integration Test

The 48 PMTs test system at INFN-LNL is and has been a central part for the validation of the JUNO readout electronics. Before the start of the FEE mass-production phase, the system has been used as a long-time test for the electronics, allowing for hardware weak points and firmware flaws to be detected and corrected. After a brief description of the apparatus in Sec. 11, the dissertation reports the tests and analysis performed. Using the final JUNO electronics, I, together with the collaboration of colleagues from the JUNO Padova group, have successfully calibrated the detector's energy response exploiting both radioactive sources and cosmic rays. The results are in perfect agreement, exposing an extremely good electronics energy linearity.

The detector has also been used for the characterization of the timing synchronization and readout performances, where having a multi-PMT/multi-GCU setup is essential. The results from the timing synchronization shows a timing offset between different GCUs spanning over a range of 38 ns, slightly diverging from the ideal conditions timing window which should be limited to 32 ns. This is likely to be caused by the asymmetry of the Cat-5E twisted pairs, which degrades the performances of the IEEE 1588-2008 PTP protocol. This unavoidable divergence, although it can not be considered negligible

per se, does not represent an issue for JUNO, as an accurate calibration procedure is foreseen, concisely described in Sec. 3.2.4, which will take into account the time differences from the different channels providing a nanosecond online timing accuracy.

The readout performances reported in Sec. 12.2 are useful to determine the ControlHub and μHAL library efficiency and whether the use of the IPBus protocol is suitable for the readout of the whole JUNO detector. The results show that the readout efficiency starts to drop below 1 at $\sim$ 10 kHz, reading out data windows of 384 ns. The total throughput per channel is about half of the single GCU throughput. A crucial point concerning an IPBus-based data readout system is the CPU load and occupation. This is maximized when a single μHAL client readouts a single channel, which is the most flexible architecture. What the results using the 48 PMTs setup has shown, is that some trade-off is necessary between flexibility and CPU occupation. In fact, reducing the number of μHAL clients by having them serialize the data readout from different channels, allows for a significantly lower CPU load. More tests need to be performed, on a higher number of channels, in order to fine-tune the trade-off, but the outcome of the readout test on the LNL detector highlights the feasibility of a IPBus-based readout system.

Aside from the FEE characterization and hardware/firmware validation, an additional implicit benefit of the setup has been the gain of familiarity with the JUNO electronics. With the commissioning phase of JUNO being close, an hardware testing facility based in Kunshan, China, is currently under construction, with the objective being to test every GCU board after production. The Kunshan site will have the ability to test up to 200 boards (inside their own UWB) concurrently. Without a small-scale test, such as the LNL detector, the challenges to set up such a huge testing site would have been much amplified. Moreover, the experience that me and my colleagues from the JUNO Padova group have acquired, allowed us to develop a test protocol, that will be used in Kunshan to determine whether a board is suitable to be used in JUNO, or is in need of some hardware fix.

14.3 PhD Conclusions

The research activities concerning the development of readout electronics are essential for the successfulness of physics experiments, where technical innovations are vital in order to push the boundaries for new physics discoveries. The GCU board of the JUNO experiment is an innovative technical solution in order to process the PMT information online, providing real-time processing capabilities avoiding any signal degradation due to long cabling.

Thanks to this PhD opportunity I was able to be part of the JUNO collaboration, being included and influencing the JUNO FEE developments. My PhD work ensured the delivery of a fully functional front-end readout solution, giving an extensive and meaningful contribution to the characterization of the GCU board, the development of its FPGA firmware and the accomplishment of a first integration test employing a 48 PMTs LS detector, whose results highlight the validity and suitability of the GCU concept and JUNO FEE to be used in the final installment on the JUNO CD. Moreover, the reported results were pivotal in order to proceed with the production stage of the GCU boards.

The work and activities carried out during my PhD, offered me the opportunity to gain experience

and advanced skills in several aspects of digital design, FPGA programming, HDL simulation, power and signal integrity analysis as well as electronics prototyping and testing, timing and trigger systems for large detector systems and data analysis techniques on PMT data from LS detectors. All these competencies are and will be fundamental in the design and preparation of new and innovative physics experiments.

Acronyms

μTCA Micro TCA. 52

ACU Automatic Calibration Unit. 26, 27

ADC Analog to Digital Converter. 49–51, 56, 59, 61, 63, 120, 125, 126

ADU Analog to Digital Unit. 35, 49–51, 54, 56, 57, 59, 61, 63, 69, 78, 80, 81, 91, 99

API Application Programming Interface. 53

ARP Address Resolution Protocol. 60, 154

ASIC Application-Specific IC. 48

AXI4 Advanced eXtensible Interface 4. 87

BB Bang-Bang. 93, 94, 107

BEC Back-End Card. 35, 36, 39–41, 51, 56, 65, 67, 85, 94, 99, 108, 111, 118, 119, 126, 131, 135, 138

BEE Back-End Electronics. 33–36, 51, 52, 63, 65–67, 91, 94, 103, 111, 116, 118, 128, 144

BER Bit Error Rate. 81, 82, 89, 107, 144

bisMSB p-bis-(o-MethylStyryl)-Benzene. 24, 114

BMC Biphase Mark Coded. 65, 66, 82, 83, 94

BRAM Block RAM. 48, 49

Cat-5E Category 5 Enhanced. 34–36, 38, 40, 51, 52, 57, 66, 81–83, 94, 95, 107, 108, 128, 144, 145

CC Charged Current. 3, 10, 11

CD Central Detector. 14, 22, 26, 27, 31, 33, 34, 144, 146

CDC Clock-Domain Crossing. 62

CDR Clock and Data Recovery. 52, 66, 67, 82, 83, 91, 94, 103, 104, 107, 108, 144

CERN Conseil Européen pour la Recherche Nucléaire *(European Organization for Nuclear Research)*. 35, 36, 52, 144

CL Confidence Level. 81, 82, 89, 107, 144

CLB Configurable Logic Blocks. 48, 49

CLS Cable Loop System. 26, 27

CMS Compact Muon Solenoid. 52

CMT Clock Management Tile. 49

CNO Carbon-Nitrogen-Oxygen. 11

CPU Central Processing Unit. 87, 128–130, 146

CTU Central Trigger Unit. 34–36, 39–42, 62

DAQ Data Acquisition system. 31–35, 42, 45, 46, 54, 56, 61–63, 65, 74, 85–87, 116, 128–130, 135

DDR Double Data Rate. 33, 34, 50, 56, 59–63, 69, 78, 87, 89, 130, 131, 144, 145

DSP Digital Signal Processing. 48, 49

DUNE Deep Underground Neutrino Experiment. 7

EEPROM Electrically Erasable PROM. 56, 73

EMI ElectroMagnetic Interference. 103, 108, 144

Erfc complementary error function. 136

FEC Front-End Chip. 49, 50

FEE Front-End Electronics. 31–36, 48, 51, 52, 66, 67, 81, 91, 94, 103, 111, 118, 125, 143–146

FF Flip-Flop. 48

FIFO First In, First Out. 62, 63, 86

FIT Failure In Time. 78, 80, 81, 143, 145

FMC FPGA Mezzanine Card. 39, 40, 107

FPGA Field Programmable Gate Array. 33, 35, 41, 45–52, 54, 56, 57, 59–61, 63, 66, 68, 69, 72–74, 77, 78, 85, 87, 89, 91, 94, 95, 99, 101, 103–108, 116, 118, 125, 130, 143–147, 150

FSM Finite State Machine. 67

FTP Foiled Twisted Pairs. 51, 66, 107

GCU Global Control Unit. 32, 35, 36, 38, 40, 42, 45–52, 54, 56, 57, 59, 63, 65, 66, 69, 72–74, 77–81, 83–87, 89, 91, 94, 95, 97, 99, 101, 107, 108, 111, 116–118, 126–130, 135, 143–146

GPIO General Purpose I/O. 48, 107

GSI Gesellschaft für Schwerionenforschung *(Centre for Heavy Ion Research)*. 36

GTCS Guide Tube Control System. 26, 27

HAL Hardware Access Library. 53

HDL Hardware Description Language. 60, 147, 155

HK Hyper-Kamiokande. 7, 12

HP High Performance. 49

HR High Range. 49, 66, 105

HV High Voltage. 24, 38, 49, 54, 56, 81, 112, 119, 121–123, 151

HVU HV Unit. 54, 61, 80, 81, 95, 97, 112

I^2C Inter-Integrated Circuit. 61, 73

I/O Input/Output. 47–49, 66, 77, 105, 151

IBD Inverse Beta Decay. 3, 9, 13–16, 18, 32, 35, 42

IC Integrated Circuit. 48, 66, 67, 80, 95, 149

ICMP Internet Control Message Protocol. 60

IH Inverted Hierarchy. 7, 8, 15–17

IHEP Institute of High Energy Physics. 32, 49, 91, 95, 128

ILA Integrated Logic Analyzer. 46, 82, 108

INFN Istituto Nazionale di Fisica Nucleare *(National Institute for Nuclear Physics)*. 32, 45, 111, 117, 118, 145

IOB I/O Block. 48, 61, 68, 106, 144

IP Internet Protocol. 52, 60, 74

IPC Intellectual Property Core. 46, 60, 82, 105, 108

JINR Joint Institute for Nuclear Research. 32, 54

JUNO Jiangmen Underground Neutrino Observatory. 7, 9–18, 21–24, 26, 27, 31, 33–36, 38, 45–47, 51, 53, 65, 66, 68, 71, 76–78, 81, 86, 87, 95, 97, 99, 101, 103, 107, 108, 111, 112, 116, 118, 125, 128–130, 133, 143–146

K2K KEK to Kamioka. 7

KamLAND Kamioka Liquid scintillator AntiNeutrino Detector. 6, 10

LAB Linear AlkylBenzene. 24, 114

LAN Local Area Network. 38, 116

LASER Light Amplification by Stimulated Emission of Radiation. 115, 126, 127, 130

LED Light Emitting Diode. 72, 73, 115, 121, 122

LNL Laboratori Nazionali di Legnaro *(Legnaro National Laboratories)*. 111, 115, 117–119, 121, 125, 126, 128, 129, 131, 133–135, 138, 145, 146

LS Liquid Scintillator. 9, 10, 14, 19, 22, 24, 32, 34, 111, 112, 114, 115, 120, 135, 138, 146, 147

LUT Look-Up Table. 48, 105, 106

LVDS Low-Voltage Differential Signaling. 40, 51, 68, 95

MAC Media Access Control. 56, 60, 63, 73, 74

MACRO Monopole, Astrophysics and Cosmic Ray Observatory. 7

MaPMT Multianode PMT. 26

MCP Micro-Channel Plate. 24–26

MH Mass Hierarchy. 7, 15–18, 21, 22

MIG Memory Interface Generator. 60

MINOS Main Injector Neutrino Oscillation Search. 7

MMCM Mixed Mode Clock Manager. 60

MMCX Micro-Minimature CoaXial. 107

MPV Most Probable Value. 138

MWA Moving Window Average. 71, 73

MWD Moving Window Deconvolution. 69–71, 73

mwe meter water equivalent. 9, 14, 22

NC Neutral Current. 3, 10, 11

NCO Numerically Controlled Oscillator. 104–106, 144

NH Normal Hierarchy. 7, 8, 15–17

NIC Network Interface Cards. 46

NIM Nuclear Instrumentation Module. 138

NNVT North Night Vision Technologies. 24, 25

NOνA NuMI Off-axis ν_e Appearance. 7

NPP Nuclear Power Plants. 21

NuMI Neutrinos at the Main Injector. 7, 153

OPERA Oscillation Project with Emulsion-tRacking Apparatus. 26

ORCA Oscillation Research with Cosmics in the Abyss. 7, 12

PA Phase Aligner. 104, 107

PACC Phase ACCumulator. 105, 106

PCB Printed Circuit Board. 46, 78, 91, 106, 144

PD Phase Detector. 103, 107

PE PhotoElectron. 18, 22, 24, 31–33, 47, 50, 63, 68, 115, 121

PFD Phase and Frequency Detector. 104

PINGU Precision Icecube Next Generation Upgrade. 7, 12

PLD Programmable Logic Device. 48

PLL Phase-Locked Loop. 50, 56, 60, 94, 103, 104, 107, 108

PMT PhotoMultiplier Tube. 9, 15, 18, 19, 22, 24–26, 31, 33–35, 42, 45, 46, 48, 49, 54, 59, 61, 63, 68–72, 85, 86, 94, 97, 108, 111–117, 119–121, 123, 125, 126, 135, 136, 138, 143, 145–147, 152

pp proton-proton. 11

PPO Poly-Phenylene Oxide. 24, 114

PRBS PseudoRandom Binary Sequence. 81, 82, 89, 94, 107, 108

PROM Programmable Read-Only Memory. 48, 56, 150

PTP Precision Time Protocol. 35, 36, 38, 67, 125, 128, 145

QE Quantum Efficiency. 24, 112, 114

RAM Random-Access Memory. 33, 48, 49, 56, 128, 149, 154

RARP Reverse ARP. 60

RENO Reactor Experiment for Neutrino Oscillation. 7

RGMII Reduced Gigabit Media-Independent Interface. 63, 95

RMS Root Mean Square. 50, 56, 82

RMU Reorganize and Multiplex Unit. 40–42

ROV Remotely Operated under-liquid-scintillator Vehicle. 27

RTL Register-Transfer Level. 59, 60, 89

SDRAM Synchronous Dynamic RAM. 56, 89, 130

SerDes Serializer/Deserializer. 50, 51, 61, 105, 106, 125, 126, 144

SFP Small Form-factor Pluggable. 41

SK Super-Kamiokande. 6, 7

SM Standard Model. 4

SMA SubMiniature version A. 85, 128, 138

SN SuperNova. 10, 11, 32–34, 47, 62, 130, 144, 145

SNO Sudbury Neutrino Observatory. 4, 6

SNR Signal to Noise Ratio. 63

SPI Serial Peripheral Interface. 48, 60

SRAM Static RAM. 48

STP Shielded Twisted Pairs. 35

SyncE Synchronous Ethernet. 36

T2K Tokai to Kamioka. 7

TAO Taishan Antineutrino Observatory. 12

TCA Telecommunications Computing Architecture. 52, 149

TCP Transmission Control Protocol. 53, 74

TDM Time Division Multiplexed. 65, 91

TTC Timing, Trigger and Control. 35, 52, 65, 66, 144

TTIM Trigger and TIMing. 40, 41, 65, 85, 111, 118, 128

UART Universal Asynchronous Receiver-Transmitter. 61

UDP User Datagram Protocol. 35, 52, 53, 60, 63

USA United States of America. 7

USB Universal Serial Bus. 74, 116

UTP Unshielded Twisted Pairs. 35, 52, 82, 83

UWB Under-Water Box. 34, 35, 38, 39, 45, 49, 54, 78, 81, 91, 95–97, 99, 100, 143, 145, 146

VCO Voltage-Controlled Oscillator. 103, 104

VFL Vertex Fitting Logic. 42

VHDL VHSIC HDL. 60, 104, 105

VHSIC Very High Speed Integrated Circuit Program. 60, 155

WLS Wave-Length Shifting. 26

WP Water Pool. 22, 26, 31, 34

WR White Rabbit. 36, 40–43, 67

XML Extensible Markup Language. 60

XVC Xilinx Virtual Cable. 74, 75

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