EPICS IOC BASED ON COMPUTER-ON-MODULE FOR THE LNL LABORATORY

J. Vásquez, D. Pedretti, R. Ponchia, INFN/LNL, Legnaro, Italy
M. Bellato, R. Isocrate, INFN, Padova, Italy
M. Bertocco, UNIPD, Padova, Italy

Abstract

At LNL it is being carried out an upgrade campaign of the control systems of the accelerator complex. The two main goals are standardization of hardware and software and system interoperability. EPICS has been chosen as the standard framework for developing new control systems; this will address software standardization and system interoperability. In order to achieve hardware standardization, a new EPICS IOC is under development, which will become a basic construction block for all future control systems. The COM (Computer-on-Modules) from factor has been chosen as the hardware platform for the IOC, along with the peripheral devices needed for developing all the foreseen control system at LNL. Prototypes of this IOC has been developed using ADLINK's Type 6 COM Express modules on generic carrier boards with DIO, ADC and DAC expansion boards. These prototypes have been tested under typical applications at LNL in order to validate the hardware platform choice. Experimental results show that the performance of the IOC in terms of effective resolution (ENOB and bias error), sample rates and CPU usage is suitable for satisfying the requirements of the control systems.

IOC DESCRIPTION

The IOC is intended as a standard system with the necessary interfaces in order to be able to control the instrumentation present on all the foreseen system at LNL. EPICS tools will be used for software development in a standard way. For each application, a custom-made control algorithm will be developed under the framework.

COM form factor has been chosen as the hardware platform for the IOC. In particular, the type 6 COM Express standard was selected [1].

The COM will be installed on a custom carrier board, designed at LNL. This carrier board will contain peripheral devices such as digital IO, ADCs, DACs, stepper motor controllers, and communication interfaces, among others, connected to the COM. Its design is under carefully considerations in order to cover all the common needs for the current and the foreseen future control systems at LNL.

Some interfaces are already available directly from the COM. Others will be controlled using USB ports. Many others will be controlled by a FPGA that will communicate with the COM through a PIC Express lane. Figure 1 shows a simplify block diagram of the IOC.

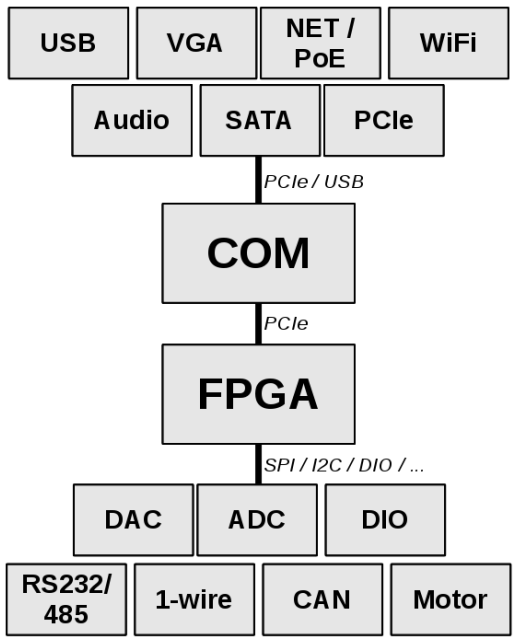

Figure 1: IOC simplify block.

IOC PROTOTYPES IMPLEMENTATION AT LNL

In order to test the validity of the COM as hardware platform for IOC developments, prototypes were developed using commercial devices. These prototypes, at the same time, allowed developing the software part of control systems.

The developed software is mostly independent from the hardware implementation, due the fact that the selected COM uses Intel CPUs allowing the use of a standard Linux environment for the implementation. In this way, once the custom IOC will be ready, the software would be easy transport to the new hardware platform.

On the other hand, prototypes were used to develop and implement diverse control systems at LNL. This allowed testing them under real operative conditions, as well as to develop critical control system without waiting for the final custom IOC to be available.

Hardware Architecture

The prototypes have been developed using Adlink [2] Type 6 COM Express module on a generic carrier board. Commercial Digital IO, ADCs and DACs PCIe boards were installed on the carrier board in order to provide IO capabilities to the IOC.

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Adlink's DAQe-2214 boards were used as ADC inputs. Each board uses one x1 PCIe interface and provides 16 16-bits, 250 KSample/s, +/-10 V channels. It also provides 24 digital IO channels.

In the same way, Adlink's PCIe-6216 boards were used as DAC outputs. Each board provides 16 16-bits, +/-10 V channels, using a 1x PCIe line.

On Figure 2 it is shown a picture of a prototype with the COM on a generic carrier board with a DAQe-2214 and a PICe-6216 boars.

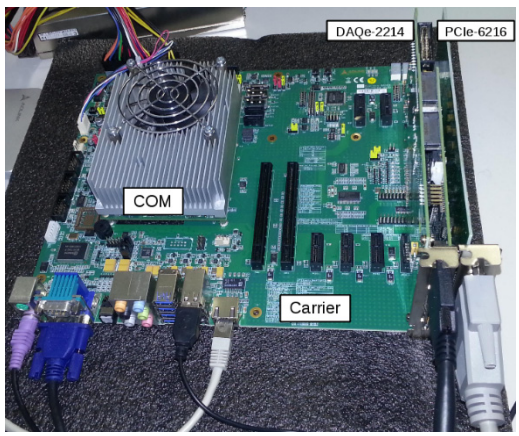

Figure 2: IOC prototype.

Software Architecture

Adlink provides linux drivers for the expansion boards used on the prototypes. The drivers provide common APIs. In order to interface the EPICS IOC device supports to Adlink drivers, asynDriver [3] was used.

The analog input acquisition is performed using a periodic scanning function on the asynDriver software. This function reads the ADC inputs and do callbacks updating the recently read values into the parameter library. In this way, the EPICS record attached to an analog input receives an interruption request each time a new value is available. Inside the scanning function loop, an adjustable delay was introduced in order to allow changing the sample rate of the inputs. The same procedure is done for digital inputs acquisition.

On the other hand, for the analog outputs, a function that writes the DAC channels was implemented on the asynDriver software. This function is called each time a new value is written to an EPICS record attached to an analog output, passing it the written value. The same procedure applies for digital outputs.

EXPERIMENTAL TEST AND RESULTS

A soft IOC was deployed on a prototype IOC in order to test its performance. The COM used on the prototype was the model “Express-IB-i3-3120ME” which has an Intel Core i3-3120ME CPU at 2.4GHz and 4Gb of RAM. The COM was installed on a generic carrier board model “Express-BASE6” with a DAQ-2214 and a PCIe-6216 boards. A picture of this prototype is shown on Figure 2.

Fedora Core 17 with kernel versions 3.3.4-5.fc17.x86_64 was installed on the IOC with the board drivers installed on the system. EPICS R3.14.12 and asynDriver R4-23 were also compiled and installed. On this system, an EPICS IOC application consisting only on analog inputs and analog outputs records linked to the physical ADCs and DACs using the driver written with asynDriver.

This IOC application was used to compute the CPU usage by the application and the resolution of the ADC channels.

Acquisition Rate and CPU Usage Performance

This test was performed in order to estimate the maximum sample rate that be achieved with this IOC, as well as the correlation between the sample rate and CPU usage by the application. The test consisted on measure the CPU usage by the EPICS application (which include the driver interface) for different samples periods.

The sample period was changed using the delay inserted on the scanning function on the asynDriver described earlier. Four different scanning rate where targeted. The first one correspond to the faster scanning rate achievable, setting the delay to zero. The latest one was set to around 10 Samples/s, which it is a usual value used as sample frequency on several applications at LNL. Finally, other two rates were selected in between these values, i.e. 200 Samples/s and 1000 Samples/s. The test was perfomed both, only acquiring a single analog input channel, and acquiring all 16 analog input channels. The results are presented on Figure 3.

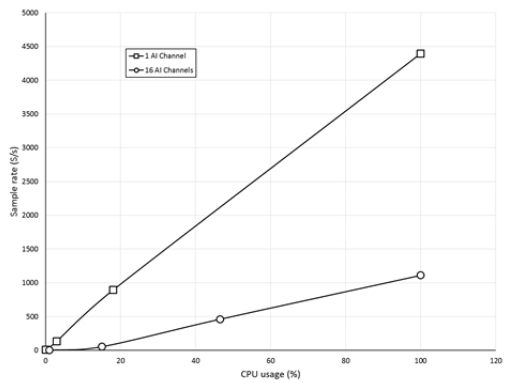

Figure 3: CPU usage versus sample frequency results.

The results show that the highest sample rate that can be reached scanning only one channel is almost 4.4 KSample/s, while when scanning all 16 channel it is around 1.1 KSample/s. However, for reaching these rates, the application uses all the available CPU, due to the fact that the acquisition loop continuously read the input channels, without any delay.

The CPU usage decreases drastically when a delay is set, lowering also of course the acquisition rates. Furthermore, it is evident that more CPU is needed for achieving higher rates on all channel respect to the case with only one channel, as it is expected.

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Particularly, for application when only one channel is needed, the second obtained value is a good compromise, achieving a sample rate of almost 900 Sample/s using only 18% of CPU. For application when all channels are needed, the third case is a good choice, using only 15% of CPU reaching rates of almost 55 Samples/s. Finally, low acquisition rates of some units of Sample/s, typically used on the LNL applications, the CPU usage is negligible.

Analog-to-Digital Performance

In order to determinate the performance of the ADC inputs, tests were performed for estimating its effective number of bits (ENOB) of resolution, following the method using frequency domain described on [4].

The ADC input range was set to +/-10 V, with a 90% full-scale input sine wave signal. For each test, more than 205888 samples were taken, at a rate of 890 Sample/s. The frequency of the input signal was 400 Hz, chosen in order to be lower that the Nyquist frequency. The calculations were performed for other six lower frequencies: 200 Hz, 100 Hz, 50 Hz, 10 Hz, 5 Hz and 1 Hz.

A plot of the obtained ENOB for the different input signal frequencies is presented on Figure 4.

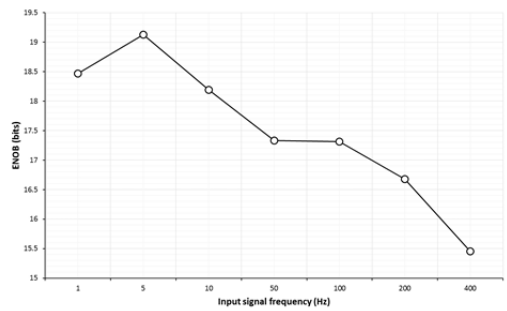

Figure 4: ENOB obtained for the analog inputs.

It can be see that for low frequency signals (lower than 150 Hz approximately) the obtained ENOB is higher than 17 bits, reaching even 19 bits. For a signal of 400 Hz, the ENOB is around 15.5 bits. The reason for accomplishing resolution greater the 16 bits (the ADC resolution) for the lower frequency signals is the effect of oversampling the input signal.

CONTROL SYSTEM IMPLEMENTATION AT LNL

Four different system were selected for the prototype implementation. The control system for these four systems contains most of elements that will be necessary on all the future implementations. Therefore, testing the prototype on all of them will demonstrate that the IOC could be implemented on any other system at LNL.

The Beam Diagnostic Data Acquisition

Beam diagnostic units are one of the most important and widely use elements on any accelerator facility. At LNL, a standard beam diagnostic unit is formed by a Faraday Cup for measuring the beam current, and a Beam Profiler for measuring the spatial distribution particles of the beam.

An IOC prototype was designed for acquiring the data from this beam diagnostic unit. On the IOC an analog input channel is used to read the output of the pre-amplifier of the Faraday Cup, while two digital outputs are used to set its gain. On the EPICS database, the read signal is converted back to the corresponding beam current.

The pre-amplifier of the beam profiler is formed by forty transconductance amplifiers with variable gain, similar to the one use on the Faraday Cup pre-amplifier. The 40 signals are multiplexed to a single analog output. On the IOC, an analog input channel is used to read the output of the pre-amplifier, while one digital output is used to generate a clock signal to control the analog multiplexer and two digital outputs are used to set the gain. In this case, a scanning function was implemented on the asynDriver driver that generates the clock and synchronously reads the analog input. At the end of a scanning sequence, the data are placed on a 40-value vector, which is passed to an EPICS waveform record.

The Electrostatic Beam Focalization and Beam Extraction

Beam focalization devices are of paramount importance on an accelerator facility, used even more extensively that the beam diagnostics. A large number of electrostatic beam focalization units are installed along the low energy beam line. These devices are driven by a series of high voltage power supplies.

On the other hand, the beam extraction system, even though it has a completely different function, its control system implementation is very similar to the beam focalization system. It consists on a single high voltage power supply that set an electric potential between the ion source and the extraction electrode.

An IOC prototype was designed for controlling the beam extraction system and an electrostatic beam focalization unit. The focalization unit comprises a steerer and a quadrupole triplet groups.

For each power supply, both the output voltage and current can be set using four analog signals. On the IOC, two ADC channels, two DAC channels and a digital output are used to control each one of the power supplies. Inside the EPICS databases, Proportional-Integral-Derivative (PID) algorithms were implemented in order to automatically control both the current and voltage, according to the set points imposed by the operator.

The Magnetic Beam Steerers

Magnetic steerers are part of the beam transport elements. They are widely used at LNL for the transport of high energy beams. A magnetic steerer unit is form by four coils, two vertical and two horizontals, installed on the beam line. They are connected on series of two, and piloted using two high current power supplies.

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The IOC configuration is exactly the same respect to the electrostatic beam focalization described on the previous section.

The ECR (Electron Cyclotron Resonance) Negative Beam Source

At LNL, one of the stable ion source present is an Electron Cyclotron Resonance (ECR) source [5] [6]. The ECR ion source in controlled by a large number of instruments: nine power supplies with analog control, five power supplies and measure instrument with serial communication port (RS232), one faraday cup for beam diagnostic, and one PLC.

The IOC developed is equipped with 16 DAC channels, 32 ADC channels, 96 digital IO and 8 serial ports, in order to be able to control all the instrumentation on the system. Most of the software components were taken from the previously described prototypes, as for example, PIDs algorithms for the analog controlled power supplies, and conversion algorithms for the beam diagnostics. On the other hand, for the instrumentation with serial communication, new algorithms were produce.

CONCLUSION

Standardization of the control systems of the accelerator complex at LNL is being addressed with the development of the new EPICS IOC.

It will be based on highly integrated Computer-on-Modules, installed on a custom tailored carrier board, equipped with all the necessary IO interfaces for satisfying the requirement of all the foreseen control systems. EPICS as a framework will bring a homogeneous software architecture with added benefits as total interoperability between the systems, and essential services as data archiving and logging.

Tests showed that the ADC inputs could reach high sample rates, around 4.4 KSample/s at the cost of high CPU usage. Nevertheless, good tradeoffs are available; a good choice for the LNL applications is the rate of 900 Sample/s using only 18% of CPU. Furthermore, sample rates of tens of Samples/s could be easily reached, with negligible use of CPU. Also, ENOB between 15.4 and 19bits were obtained on the ADC inputs.

In order to validate this hardware platform as suitable for developing the control systems at LNL, prototype IOCs were developed and implemented using commercial devices. These IOCs have been tested under real applications at LNL, with the implementation of four control systems: the beam diagnostic data acquisition, the Front-End beam extraction and focalization, the magnetic beam steerer and the ECR source systems. All the installed prototypes have shown that the hardware platform is suitable for the development of the LNL control systems using EPICS.

Although the performance is not optimal, the prototype IOCs have shown that they are suitable for controlling the selected systems, satisfying the operation requirements. However, much higher efficiency is expected from the custom IOC design.

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